NS2016 DataSheet V1.0

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2009,07

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General Description

The NS2016 is a 4-wire resistive touch screen controller, includes 12-bit resolution A / D converter. NS2016 through the implementation of the two A / D conversion has been identified by the location of the screen, in addition to measurable increase in pressure on the touch screen. Own internal 2.5V reference voltage, can be used as auxiliary input, temperature measurement and battery monitoring, battery monitoring, voltage range from 0V to 6V. NS2016 a chip temperature sensor. 2.7V typical work in the state, the closure of the reference voltage, power consumption can be less than 0.75mW.

Features

- Operating voltage range of 2.0V ~ 5.5V
- Built-2.5V reference voltage source (open when the need is greater than the supply voltage 2.6V)
- 1-way measuring input supply voltage (0V ~ 6V)
- 1 auxiliary inputs
- Built-junction temperature measurement function
- Touch-pressure measurement
- 2-wire I2C communication interface
- With automatic power down feature
- TSSOP-16 package
- -40 ~ 85 ℃ Operating Temperature Range

Applications

- Mobile phone (cell phone, etc.)
- Touch screen displays, personal digital assistant (PDA)
- Portable equipment, POS terminal machine equipment, etc.

Typical Application Circuit

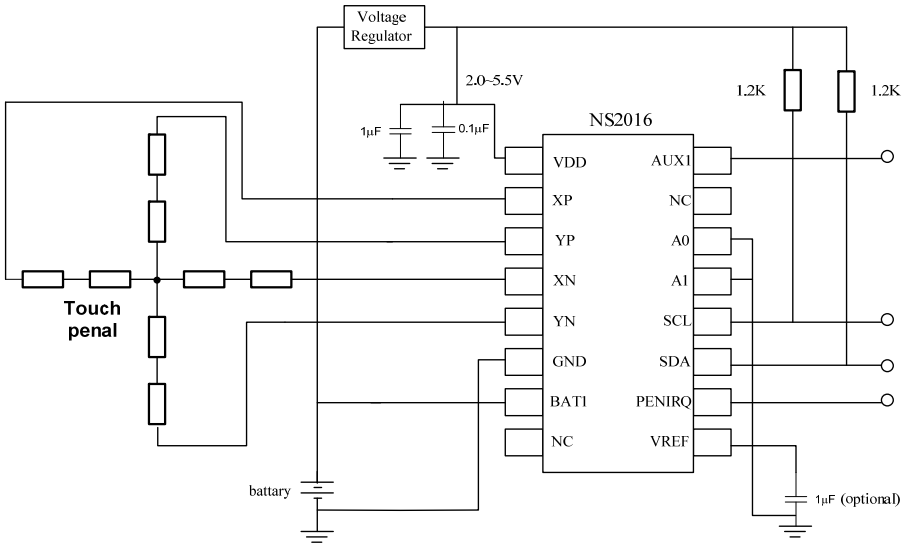


Figure 1 NS2016 Typical Application Circuit

Absolute Maximum Ratings

Table 1 Chip Limit Parameter Table

Name	Parameter
VDD Voltage	－0.3V To ＋5.5V
Analog Input Voltage	－0.3V To ＋VDD＋0.3V
Digital Input Voltage	－0.3V To＋VDD＋0.3V
Consumption	1W
Maximum Junction Temperature	＋150℃
Operating Temperature	－40℃～＋85℃
Storage Temperature	-65℃～＋150℃
Welding Temperature (less than 10 seconds)	＋260℃
ESD	+/- 8000V （HMD）
Latch Up	+/- 100mA

WARNING: In addition to limits or any other conditions, the chip may be damaged.

Electrical Characteristics

Qualification: VS = +2.5 V ~ +5.5 V, TA =- 40 ℃ ~ +85 ℃, VDD = +2.7 V, VREF = 2.5V internal voltage, 12bits standard mode (100K), or fast mode (400K), the digital input ground or VDD.

Table 2 NS2016 Electrical Characteristics Table

Parameter	Condition	NS2016			Unit
		Min	Typ	Max	
Analog Input：					
Differential Input	Cathode Input - Negative Input	0		V_{REF}	V
Single-ended Input	Cathode Input	-0.2		+VDD+0.2	V
	Negative Input	-0.2		+0.2	V
Input Capacitance			25		pF
Leakage current			0.1		μA
ADC System Performance：					
Resolution			12		Bits
No missing Code		10			Bits
Integral Linearity Error				±2	LSB[1]
Imbalance Error				±6	LSB
Gain Error	External Vref			±4	LSB
Noise Performance	Including Internal Vref		70		μV_{rms}
PSRR			70		dB
Switch Driver					
Switch On-Resistance					
YP、XP			5		Ω
YN、XN			5		Ω
Driver Current(2)	Duration 100ms			50	mA
Vref Output					
Internal Reference Voltage Accuracy		2.35	2.5	2.65	V
Internal Reference Voltage Drift			50		ppm/℃
Quiescent Current Reference Voltage			200		μA
External Vref					
Input Range		1.0		VCC	V
Input Impedance	Internal Reference Shutdown		1		GΩ
	Open The Internal Reference		250		Ω
Battery Monitor					
Input Volage Range		0.5		6.0	V
Input Impedance					
Sampling Battery			4		KΩ
Battery Monitor Off			1		GΩ
Accuracy	V_{BAT}=0.5V~5.5V,ExternalV_{REF}=2.5V	-2		+2	%
	V_{BAT}=0.5V~5.5V,InternalV_{REF}	-7		+7	%
Temperature Measurement					
Temperature Range		-40		+85	℃
Resolution	Differential mode [3]		2		℃

Accuracy	Differential mode [3]		±4		℃
Digital Input/Output					
Logic Type			CMOS		
Capacitance	All Digital Control Input Pins		5	15	pF
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	VDD*0.7		VDD+0.3	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	-0.3		0.3*VDD	V
V_{OH}	I_{OH}=-250μA	VDD*0.8			V
V_{OL}	I_{OL}=250μA			0.4	V
Data Format		Straight Binary			
Power Requirement					
VDD	Operating Range	2.0		5.5	V
Quiescent Current	Internal Vref Off		100	150	μA
	Internal Vref On		300		μA
	Power-Down State			3	μA
Temperature Range	—				
Feature		-40		+85	℃

Notes:
1. LSB that the least significant bit. When VREF = +2.5 V, for the 12bits ADC, the LSB is 610μV
2. In order to ensure reliable chip, X, Y can not be larger than the drive current 50mA
3. TEMP0 and TEMP1 test the difference, without correction

Pin Configuration

Pin Layout

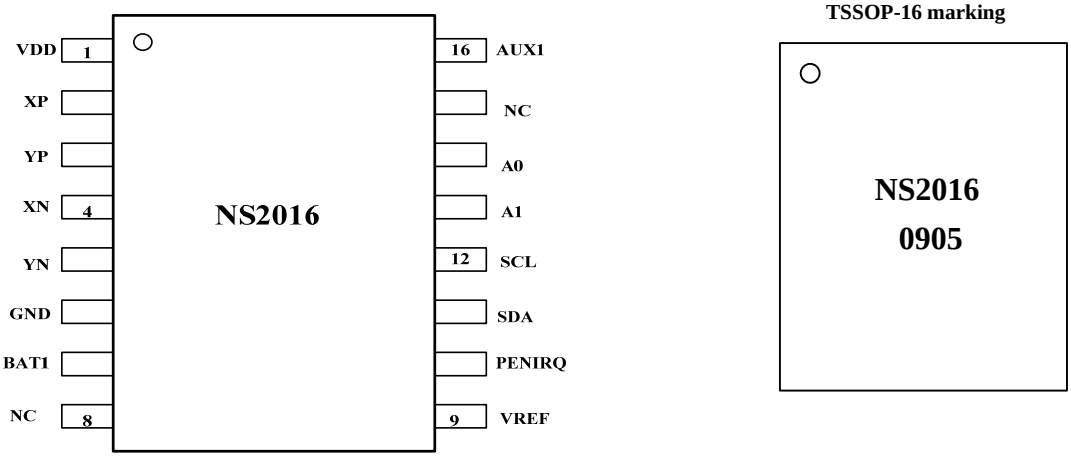


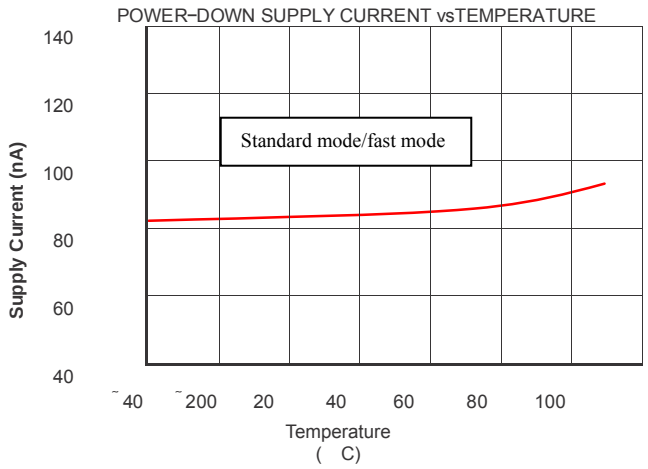
Figure 3 TSSOP-16 Package Pin Distribution

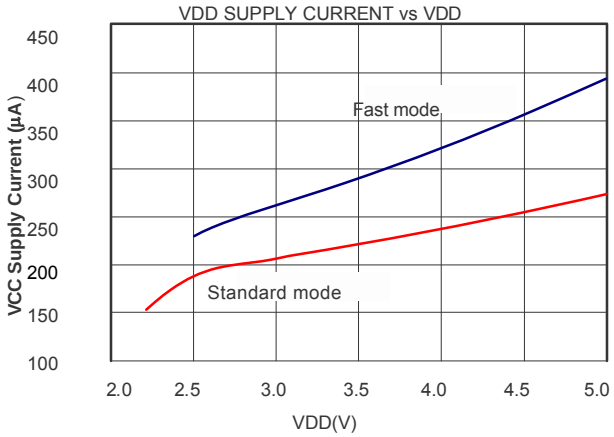
Pin Discription

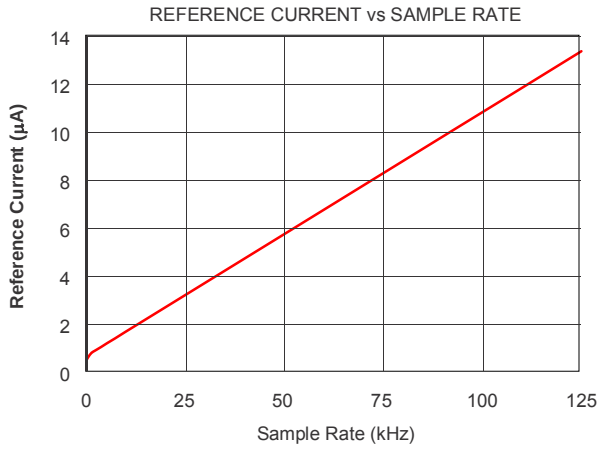
TSSOP PIN#	NAME	DISCRIPTION
1	VDD	Power Supply
2	XP	XP Position Input
3	YP	YP Position Input
4	XN	XN Position Input
5	YN	YN Postion Input
6	GND	Ground
7	BAT1	Battery Monitor Input1
8	NC	Noll
9	VREF	Reference Voltage Input/Output
10	PENIRQ	Pen Interrupt Pin
11	SDA	I2C Data Interface
12	SCL	I2C Clock Interface
13	A1	I2C Address Input1
14	A0	I2C Address Input0
15	NC	Noll
16	AUX1	Auxiliary Input to ADC1

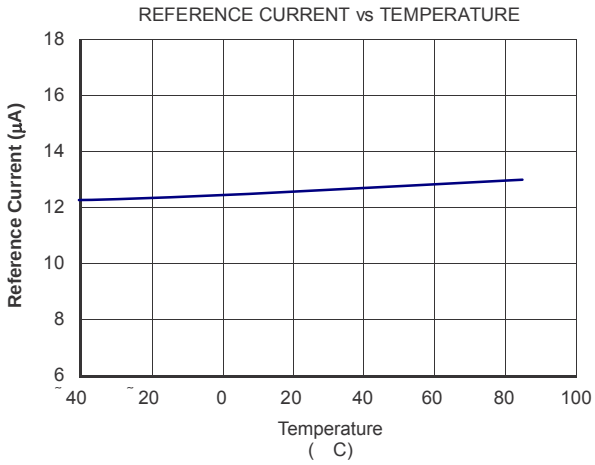
Typical Characteristics

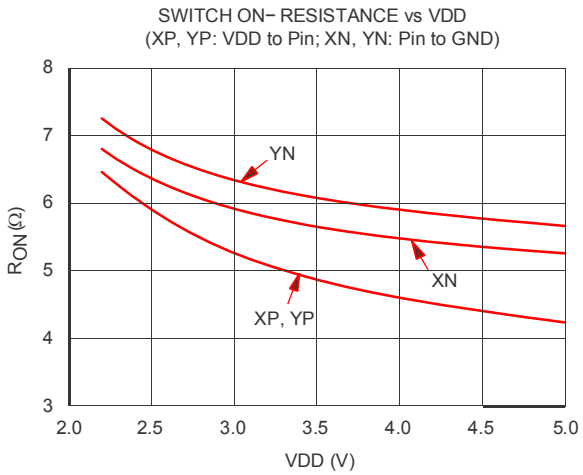
Conditions: TA = 25 ℃, VDD = +2.7 V; VREF = 2.5V external voltage, 12-bit mode; PD0 = 0

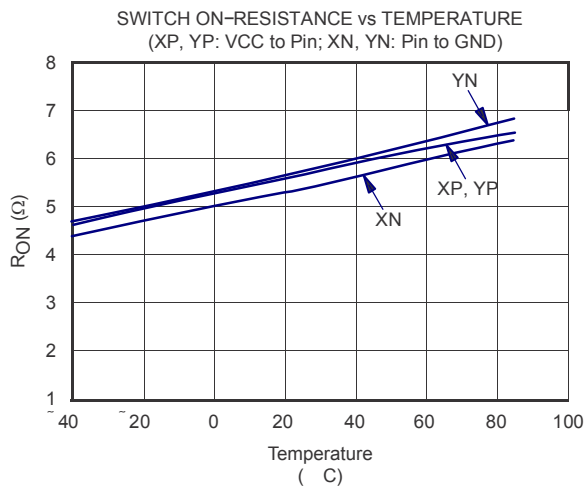


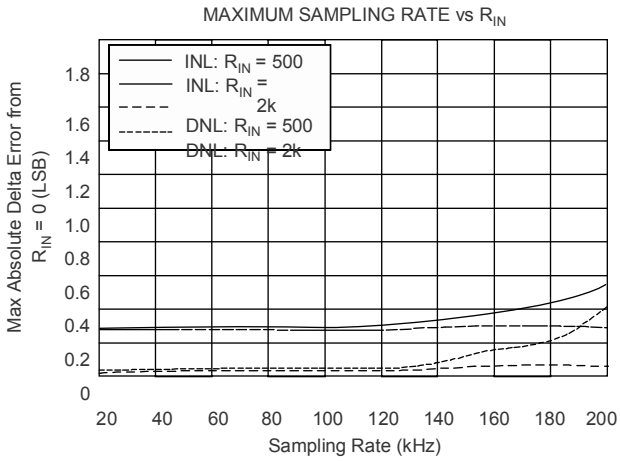


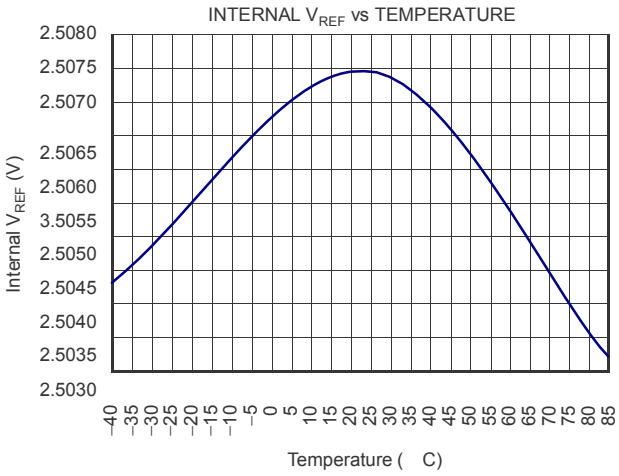


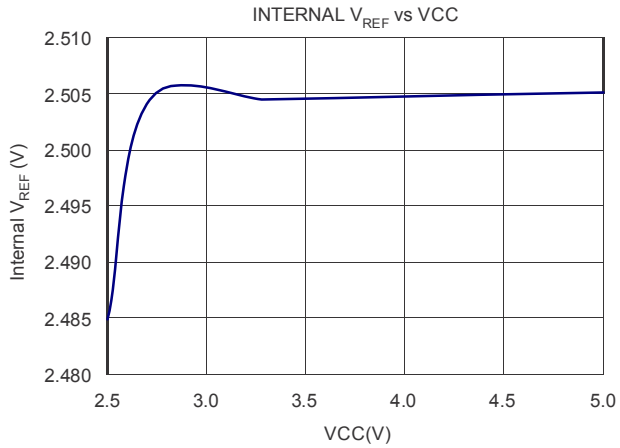


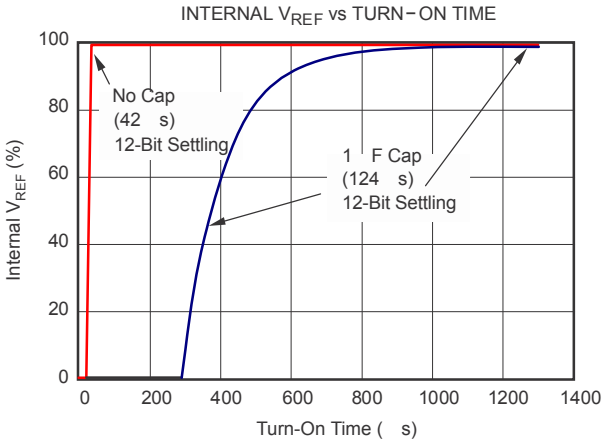





MAXIMUM SAMPLING RATE vs R_IN
INL: R_IN = 500
INL: R_IN = 2k
DNL: R_IN = 500
DNL: R_IN = 2k
Max Absolute Delta Error from R_IN = 0 (LSB)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
20 40 60 80 100 120 140 160 180 200
Sampling Rate (kHz)


INTERNAL V_REF vs TEMPERATURE
2.5080
2.5075
2.5070
2.5065
2.5060
3.5055
2.5050
2.5045
2.5040
2.5035
2.5030
Internal V_REF (V)
−40 −35 −30 −25 −20 −15 −10 −5 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85
Temperature (C)


INTERNAL V_REF vs VCC
2.510
2.505
2.500
2.495
2.490
2.485
2.480
Internal V_REF (V)
2.5 3.0 3.5 4.0 4.5 5.0
VCC(V)


INTERNAL V_REF vs TURN−ON TIME
100
80
60
40
20
0
Internal V_REF (%)
No Cap
(42 s)
12-Bit Settling
1 F Cap
(124 s)
12-Bit Settling
0 200 400 600 800 1000 1200 1400
Turn-On Time (s)

Theory of Operation

The Basic Principle

NS2016 is a typical type of successive approximation ADC (SAR ADC), contains a sample / hold, analog-to-digital conversion, serial data output functions. At the same time, there is a 2.5V internal reference voltage source, the temperature detection circuit, and using external clock. Single power supply, power supply voltage range of 2.0V ~ 5.5V. Vref directly determines the range of ADC input , the reference voltage can use the internal reference voltage, can also be directly imported from outside the range of 1V ~ VCC reference voltage (the requirements of external reference voltage source with low output impedance). The analog inputs (X, Y, Z, VBAT, Temp, and AUX) via control register enter the ADC, ADC can be configured as single-ended or differential mode. Selecting VBAT, Temp and AUX ,ADC should be configured for single-ended mode; as a touch screen application, it should be configured as a differential mode, which can effectively eliminate the parasitic resistance of the driver switch and external interference caused by measurement error and improvet he conversion accuracy.

Analog Input Characteristics

Figure 5 describes MUX, ADC's analog input, reference voltage reference as well as the I2C interface circuit. Table 3 shows the control byte order bit C3, C2, C1, C0 and the relationship of configuration between NS2016.

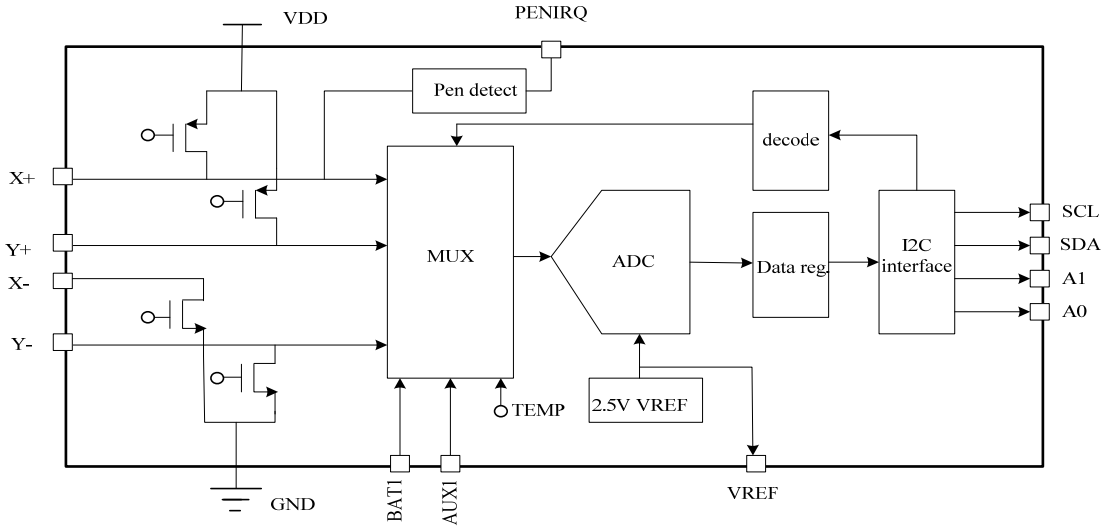


Figure 5 NS2016 Analog Input Schematic

Table 3 ADC Input Configuration

C3	C2	C1	C0	BAT1	AUX1	TEMP	YN	XP	YP	Y-Position	X-Position	Z_1-Position	Z_2-Position	X-Driver	Y-Driver
0	0	0	0			+IN (TEMP0)								Off	Off
0	0	0	1	+IN										Off	Off
0	0	1	0		+IN									Off	Off
0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—
0	1	0	0			+IN (TEMP1)								Off	Off
0	1	0	1	—	—	—	—	—	—	—	—	—	—	Off	Off
0	1	1	0	—	—	—	—	—	—	—	—	—	—	Off	Off

0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—
1	0	0	0	Long driver, Accelerate mode					+IN		meas			On	Off
1	0	0	1	Long driver, Accelerate mode				+IN		meas				Off	On
1	0	1	0	Long driver, Accelerate mode				+IN				meas		XN On	YP On
1	0	1	1	Long driver, Accelerate mode			+IN						meas	XN On	YP On
1	1	0	0	Short driver, auto power down,low power mode					+IN		meas			On	Off
1	1	0	1	Short driver, auto power down,low power mode				+IN		meas				Off	On
1	1	1	0	Short driver, auto power down,low power mode				+IN				meas		XN On	YP On
1	1	1	1	Short driver, auto power down,low power mode			+IN						meas	XN On	YP On

Internal Vref

NS2016 internal 2.5V reference voltage source can be off or on through the control-bit PD1 (see Table 6 and Figure 6).In general, the internal reference voltage is only used to measure VBAT, Temp and AUX input. If the request for higher measurement accuracy, you should use an external reference voltage source. An external reference input directly from the VREF pin,which is in use,be sure to close the internal reference voltage source.

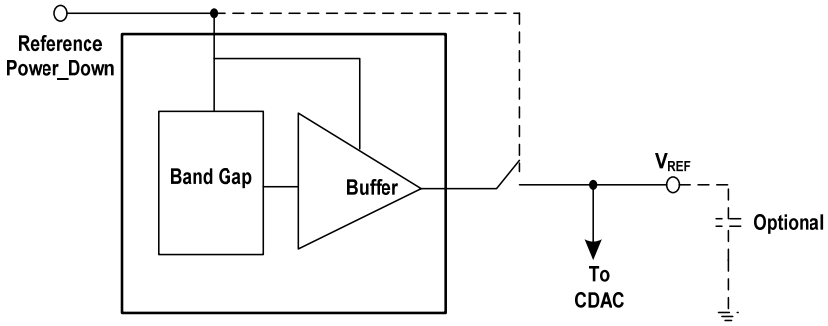


Figure 6 Internal Vref Schematic

Single-ended Mode

When the command control bit C3 is low, NS2016 is in the measurement mode of BAT, AUX or Temp, the internal ADC reference voltage source is the single-ended mode, using the internal 2.5V reference source (can also use the external input voltage source) as the ADC reference voltage, application of the principle of single-ended mode shown in Figure 7.

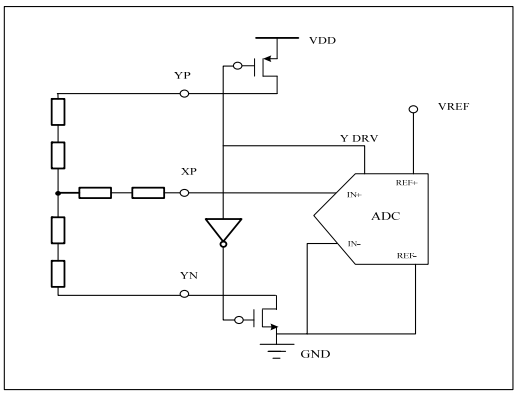


Figure 7 Schematic diagram of single-ended mode (C3 = 0, Y direction drive switch closure, XP as an analog input)

Differential Mode

When the command control bit C3 is high, NS2016 is in the measurement mode of X, Y, Z, the internal ADC reference voltage source is the differential mode, shown in Figure 8. The advantage of differential mode: + REF and-REF input directly to the YP, YN, Which can eliminate measurement error because of the switch on-resistance. The disadvantage is that: both the ample or conversion process, the driver will need to be on, relative to single-ended mode, the power consumption increased.

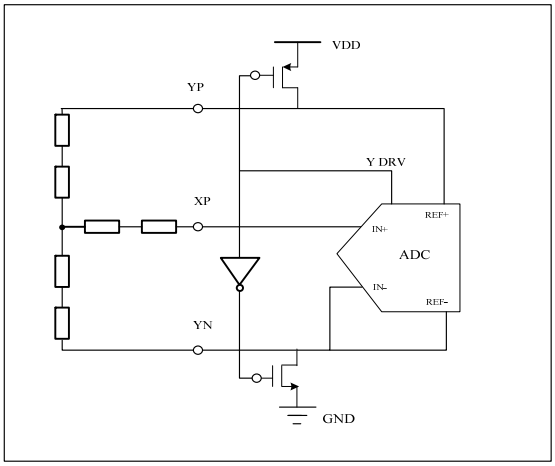


Figure 8 Differential reference mode diagram (C3 = 1, Y direction drive switch closure, XP as an analog input)

Application Recommendations of Touch Screen

In the application, it is recommended to add some external capacitor across the touch screen in order to filter the noise from touch-screen (such as: the noise from backlight and LCD circuit). Capacitors and resistors form a low-pass filter to suppress noise. Too large capacitance value may lead to an increase in set-up time, there gain error. So capacitance should be taken into consideration to choose the input signal bandwidth requirements.

Temperature Measurement

Integrated temperature detection for the detection of temperature. There are two methods oft emperature measurement.

Method I: direct measurement

The use of the PN junction diode temperature coefficient characteristics of a relatively stable through measuring the PN junction diode voltage to measure the temperature, can be pre-tested and stored the PN junction voltage (600mV typical value of about) at room temperature, PN junction temperature coefficient is about -- 2mV / ℃, measure the PN junction voltage at other temperature ,then the temperature can be got. This method would change with the process, andt he need for correction

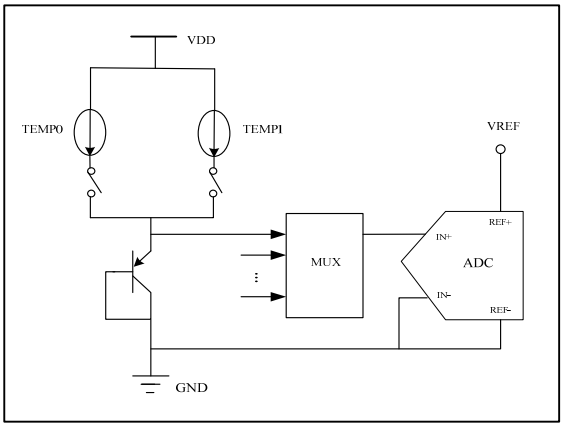


Figure 9 Schematic diagram of temperature measurement function

Method 2: indirect measurement
This method does not require the test temperature specified benchmarks, the accuracy can achieve 2 ℃. This method requires a second conversion:The first time, set up "A2A1A0" = "000", test temp0 the PN junction current-voltage V0 Second, set up "A2A1A0" = "111", to achieve 91 times the current temp0 big test at this time of the PN junction voltage V1.Second and the first conversion of the voltage difference by the equation (1), said:

$$\triangle V = \frac{kT}{q} \bullet \ln(N) \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (1)$$

where:
N - Current ratio coefficient, equal to 91;
k -Boltzmann's constant, equal to 1.38054 × 10-23 volts per opening (V • K-1);
q - charge, equal to 1.602189 • 10-19C
T - temperature (Kelvin)
Second, more than one way to provide a more accurate method of measuring accuracy can be achieved 2 ℃. Absolute temperature conversion formula is:

$$^{\circ}K = q \bullet \frac{\Delta V}{(k \bullet \ln(N))} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2)$$

where:
△ V = V (I91) - V (I1) (in mV)
° K = 2.573 K / mV • △ V
℃ = 2.573 • △ V (mV) - 273K
Note: Since each diode bias current is only the work of the three sampling clock cycle (only during the sampling), so the increase in power consumption is obvious, especially in temperature measurement is only occasional at this time of internal NS2016 on behalf of the junctiont emperature can be ambient temperature.

Battery Measurement

Shown in figure 10, the battery voltage from 0V to 6V ,input voltage (VBAT) through sub-pressure (1 / 4) enter to the ADC, so the battery voltage of 5.5V was divided into 1.375V then enter the ADC.

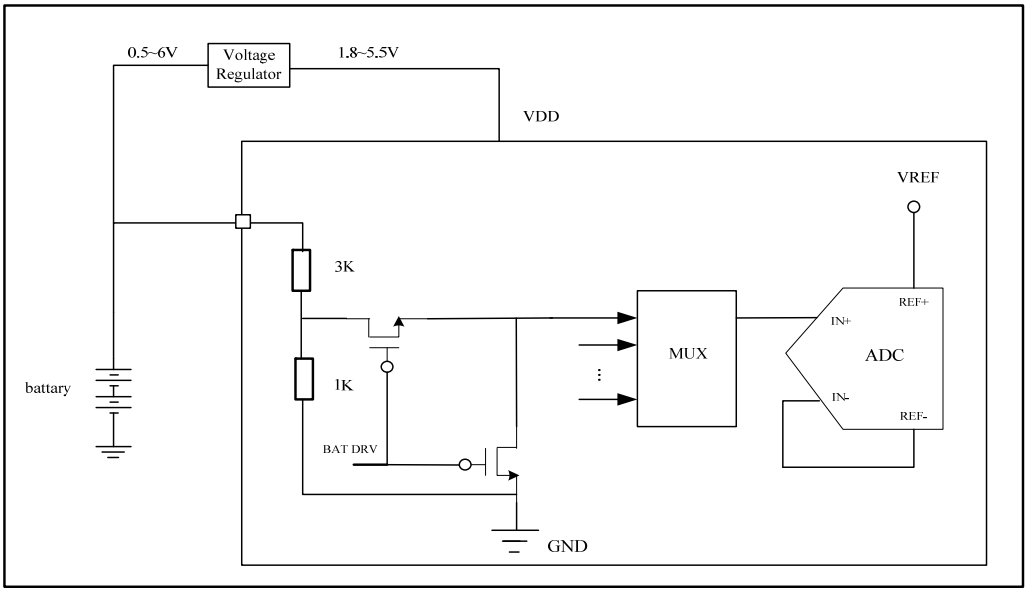


Figure 10 the battery voltage measurement function module map

Pressure Measurement

NS2016 can also measure the pressure of touch, that is written in Table 3 Measurement of Z direction. In general, the performance of such measurements do not ask for much, so the use of 8-bit resolution mode (however, the calculation is the following 12-bit resolution mode) can be. There are several different ways to achieve the pressure measurements. The first method needs to know X panel of the resistance, X the location of the measurement, touch screen panel attached between the two measured values (Z1 and Z2), as shown i n Figure 11. Formula can be used (3) calculate the touch resistance:

$$R_{touch} = R_{X\text{-}Plate} \bullet \frac{XPosition}{4096}\left(\frac{Z2}{Z1} - 1\right) \cdots\cdots\cdots\cdots\cdots\cdots (3)$$

The second approach requires the detection of X and Y panels panel resistance, X and Y position, and the Z1 position. Formula can be (4) Calculation of touch resistance:

$$Rtouch = \frac{R_{X\text{-}Plate} \bullet X\text{-}Position}{4096}\left(\frac{4096}{Z_1} - 1\right) - R_{Y\ -\ Plate}\left(1 - \frac{Y\text{-}Position}{4096}\right) \cdots\cdots (4)$$

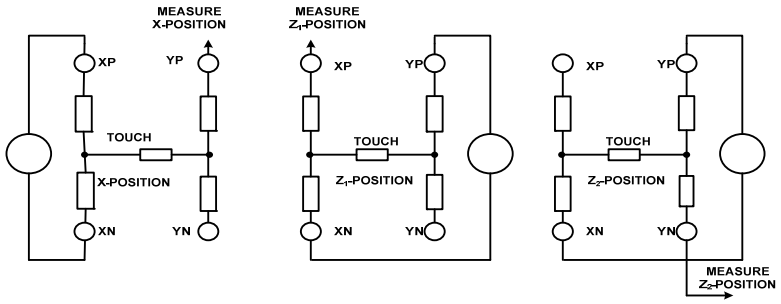


Figure 11 Pressure Measurement Block Diagram

Digital Interface

NS2016 data interface is I2C serial interface, I2C interface to meet the agreement, can realize the standard mode (100K), fast mode (400K) or high-speed mode (3.4M), divided into the control of NS2016 writing, reading two command format, write command is used to enter an address and command bytes, so that work in the designated NS2016 configuration and mode, NS2016 read command is used to output data of ADC conversion in order to obtain information related to measurement.

Write Command

Command timing, as shown in Figure 12.

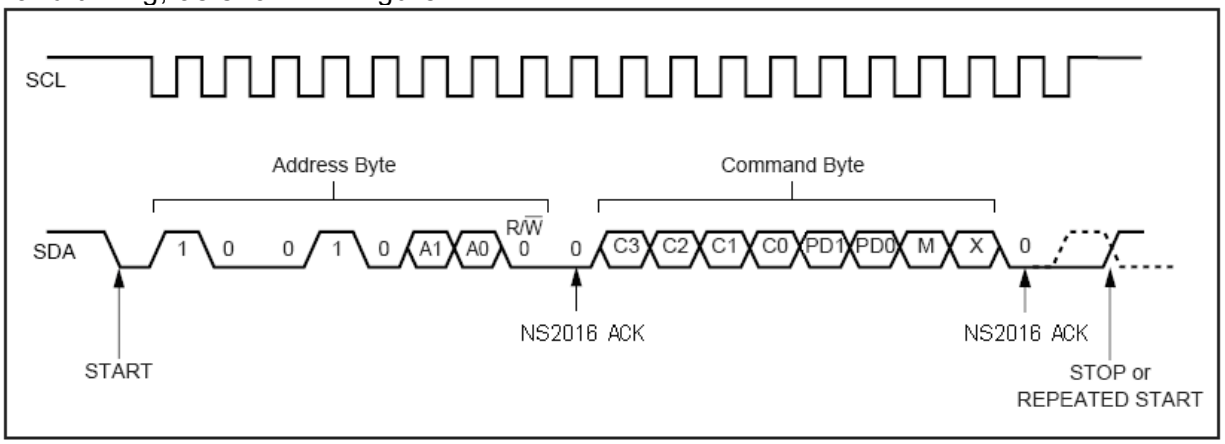


Figure 12 I2C interface write command timing diagram

First byte for address byte：

Table 4 address byte

Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0(LSB)
1	0	0	1	0	A1	A0	R/W

The lowest R / W (bit0), 0 means write command, 1 means read command A0 (Bit1), A1 (b i t 2) control bit for the hardware address, which must be in line-level with 13 pin, 14 pin to the correspon ding NS2016. The highest 5-bit address for the software, you must enter a fixed code "10010", as shown in Figure 7. After the first byte has been received , NS2016 issue response signal ACK (0-level) at the 9th clock cycle,indicating that the data hasbeen received.
Second byte for command byte:

Table 5 Command Byte

Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0(LSB)
C3	C2	C1	C0	PD1	PD0	M	X

C3, C2, C1, C0 - decided NS2016 configuration of the input signal and the corresponding measurement function, specifically as shown in table 3.
PD1, PD0 - used to control the internal reference voltage source and the pen interrupt signal, as shown in table 6:

Table 6 PD1、PD0 Control Bit

PD1	PD0	PENIRQ	Function Discprition
0	0	Enable	Saving mode, only after the second byte of write command, the internal ADC circuit starts work, until the ADC data conversion is completed, the chip automatically enter the power down state, ADC data saves in internal registers of the data to wait to be read. Internal reference source at the closed
0	1	Disable	ADC always on. Internal reference source at the closed
1	0	Enable	The difference from "00" is that this configuration of the internal reference source is turned on
1	1	Disable	The internal ADC and reference sources are always on, at this time as long as the chip is power-on, the driver switch lines to open.

M - Mode Selection, and to set the resolution of ADC. MODE = 0, ADC is a 12-bit mode; MODE = 1, ADC is an 8-bit mode. The lowest bit (bit0) is set aside, and can be set up, the general set to 0
After the second byte has been received , NS2016 will issue the response signal ACK(0-level) at the 18th clock cycle, indicating that the data has been received.

Read Command

Command Timing，Shown in Figure 13：

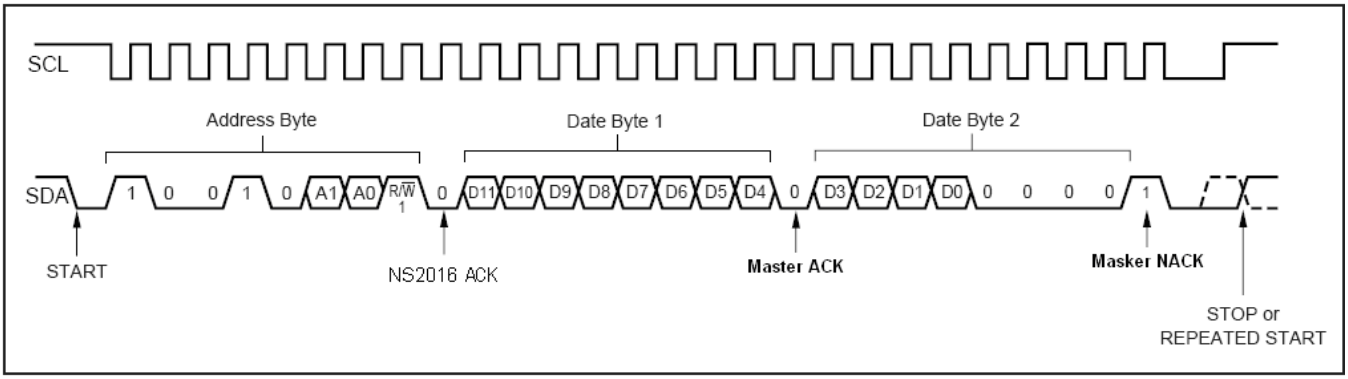


Figure 13 I2C Interface Read Command Timing Schamatic

Reading command contains 3-byte , the first byte is address , similar to the write command only for bit0 is high; the next 2 bytes is the 12bit from NS2016 (if 8bits mode, it is only 1 bytes of data), redundant 4bits zero. After NS2016 received the first byte of the address data, then issue response signal ACK (0-level) at the 9th clock cycle, then started to output the first byte of data,after the host received the first byte of data then should issue response master ACK (0-level), After NS2016 received masker ACK then started to send second byte of data,after the host received the second byte of data, do not answer ,at this time ,SDA will be pulled high , which is shown on the masker Not ACK signal.

High-Speed Mode

When the host send data "00001XXX", which was received by NS2016 then the host doesn't need wait for the response, NS2016 will enter the high-speed mode (serial rate can 3.4Mhz), until the host issued a STOP signal. High-speed mode, the read/write command format is the same as the standard mode and speed mode. But STOP signal can not be made, otherwise high-speed mode will be ended.

Digital Timing

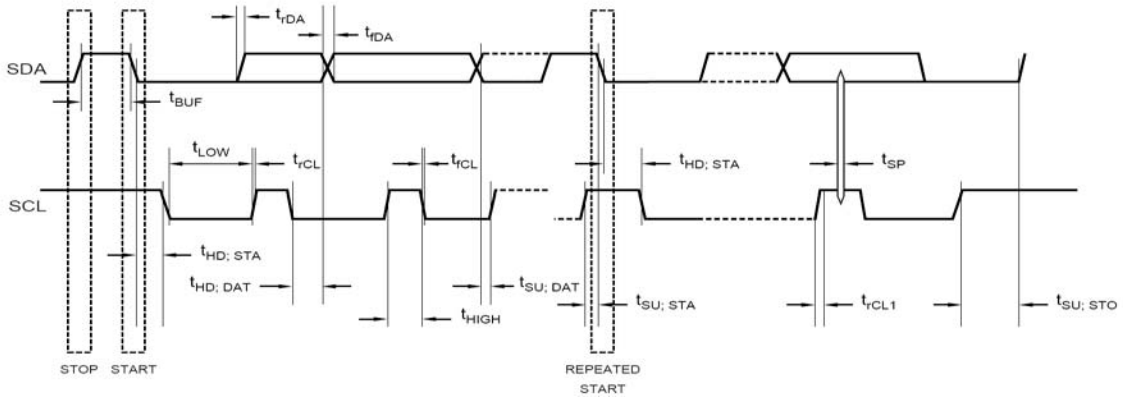


Figure 14 NS2016 Digital Interface

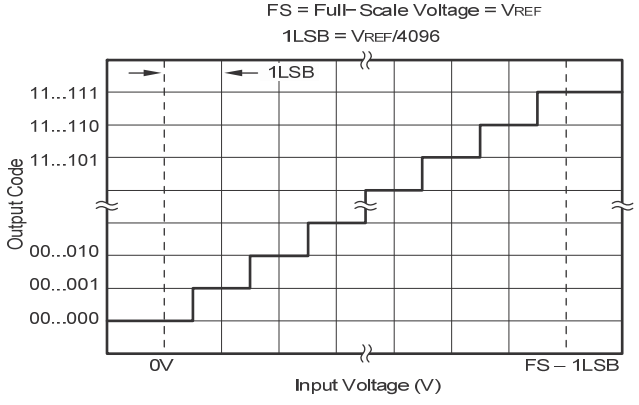
Table 7 timing specification

Serial Number	Instruction	Test Condition	+VDD = 2.7V, C_{LOAD} = 50pF		Unit
			Min	Max	
fSCL	SCL Clock Frequency	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	0 0 0 0	100 400 3.4 1.7	kHz kHz MHz MHz
tBUF	Bus Free Time Between a STOP and Start Condition	Standard Mode Fast Mode	4.7 1.3		μs μs
tHD; STA	Hold Time (Repeated) START Condition	Standard Mode Fast Mode High-Speed Mode	4.0 600 160		μs ns ns
tLOW	LOW Period of the SCL Clock	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	4.7 1.3 160 320		μs μs ns ns
tHIGH	HIGH Period of the SCL Clock	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	4.0 600 60 120		μs ns ns ns
tSU; STA	Setup Time for a Repeated START Condition	Standard Mode Fast Mode High-Speed Mode	4.7 600 160		μs ns ns
tSU; DAT	Data Setup Time	Standard Mode Fast Mode	250 100		ns ns

		High-Speed Mode	10		ns
tHD; DAT	Data Hold Time	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	0 0 0 0	3.45 0.9 70 150	µs µs ns ns
trCL	Rise Time of SCL Signal	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	 20 + 0.1Cb 10 20	1000 300 40 80	ns ns ns ns
trCL1	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	 20 + 0.1Cb 10 20	1000 300 80 160	ns ns ns ns
tfCL	Fall Time of SCL Signal	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	 20 + 0.1Cb 10 20	300 300 40 80	ns ns ns ns
trDA	Rise Time of SDA Signal	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	 20 + 0.1Cb 10 20	1000 300 80 160	ns ns ns ns
tfDA	Fall Time of SDA Signal	Standard Mode Fast Mode High-Speed Mode, Cb = 100pF max High-Speed Mode, Cb = 400pF max	 20 + 0.1Cb 10 20	300 300 80 160	ns ns ns ns
tSU; STO	Setup Time for STOP Condition	Standard Mode Fast Mode High-Speed Mode	4.0 600 160		µs ns ns
Cb	Capacitive Load for SDA or SCL Line	Standard Mode Fast Mode High-Speed Mode, SCL = 1.7MHz High-Speed Mode, SCL = 3.4MHz		400 400 400 100	pF pF pF pF
tSP	Pulse Width of Spike Suppressed	Fast Mode High-Speed Mode	0 0	50 10	ns ns
VnH	Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	Standard Mode Fast Mode High-Speed Mode	0.2VDD		V
VnL	Noise Margin at LOW Level for Each Connected Device (Including Hysteresis)	Standard Mode Fast Mode High-Speed Mode	0.1VDD		V

Data Format

NS2016 output data format is a standard binary format. The following figure gives a different output voltage corresponding to the ideal encoding.



PENIRQ Output

The PENIRQ can be set through PD0 (see table 6),pen interrupt output function shown in Figure 9. when PD0 = 0 , YN-driven open, the Y-touch screen panel to be connected to GND. PENIRQ output is connected to XP through two switches . In the standby mode, when there is a touch-screen action, XP input drop-down to ground through the touch-screen ,PENIRQ output low . when there is no movement touch screen disconnect to GND , PENIRQ high output. Through the disruption of the functional pen set PD0 (see Table 6), pen interrupt output function shown in Figure 9.

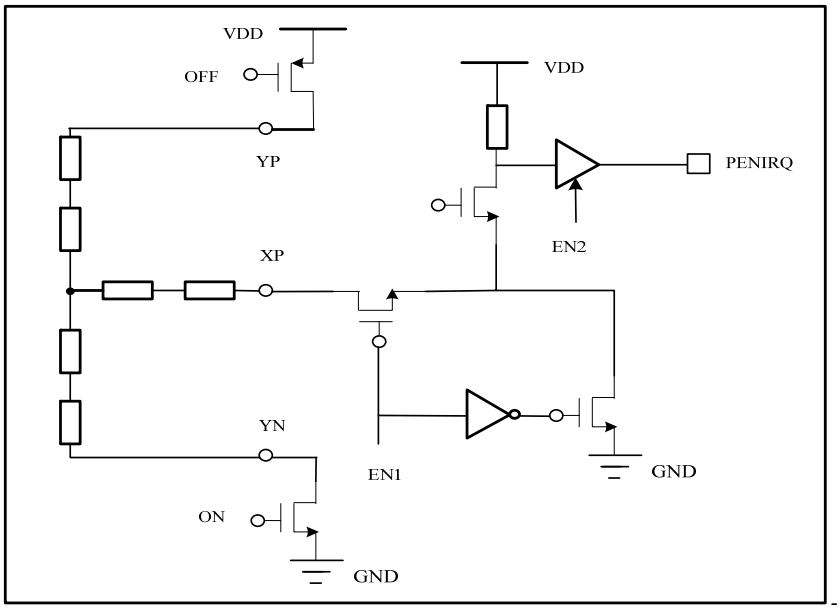


Figure 15 PENIRQ Function Schematic

In the measurement process of X, Y and Z, PENIRQ output low; in the measurement process of VBAT, AUX and temp , PENIRQ high output. PD0 = 1, the pen interrupt function have been banned, can not monitor the touch movement on the touch screen. If you want to re-enablei nterrupt function pen,need to control PD0 = 0 to write to NS2016, if the last control word contains PD0 = 0, pen interrupt output will be enable after the completion of the command.In order to avoid false triggering, it is proposed, when the processor is sending command to NS2016, maski nterrupt PENIRQ.

Application Note

Follow the following rules then the NS2016 can be brought into full play the advantages. There are many contradictions about power, cost, size and weight in the most design of portable system. Generally , the vast majority of chips for portable systems need to have considerable clean power and ground, this is because most of its internal very low power consumption devices. This will mean that fewer and fewer total bypass and ground. Moreover, the circumstances vary, so should pay attention to the following recommendations and requirements.

To enable the chip to optimum performance,do take extra care to deal with the physical connection of NS 2016 circuit. SAR basic structure is very sensitive to the pulse interference, and the mutation of power supply voltage, reference voltage, ground connection, and the digital input which only occurred before the analog comparator output latch. Thus, in n-bit SAR converter conversion at any one time, there will have n "window" that external transient voltage formed affect the outcome of the conversion. Similar pulse interference may come from switching power supplies, digital logic circuits, and high-power devices. These disturbances on digital logic output error depends on the reference voltage, layout wiring and external timing. The changes of input clock timing affect the error of the digital logic output too.

For the interference effects of the above considerations, NS2016 power supply must be clean, and there is a good bypass. As far as possible close to the chip , plus a 0.1μF ceramic capacitor. If the impedance is highbetween VDD and power supply, it should also add a 1μF ~ 10μF capacitance. Leakage current of allcapacitors must be small enough to avoid consume additional power when the NS2016 down to the system. In general, VREF pin does not require additional bypass capacitor, because the internal reference voltage has been output through internal operational amplifier buffer. However, if you use an external reference voltagesource, need to add bypass capacitor, and to ensure that does not cause oscillation. NS2016 has no the repress ability for external reference voltage input, if the input reference voltage sourcedirectly connected with the power supply, power supply noise and ripple will directly affect the accuracy of the conversion. Despite the high-frequency noise can be filtered, but it is very difficult to filter interference ofpower frequency, which should be regarded in the design.

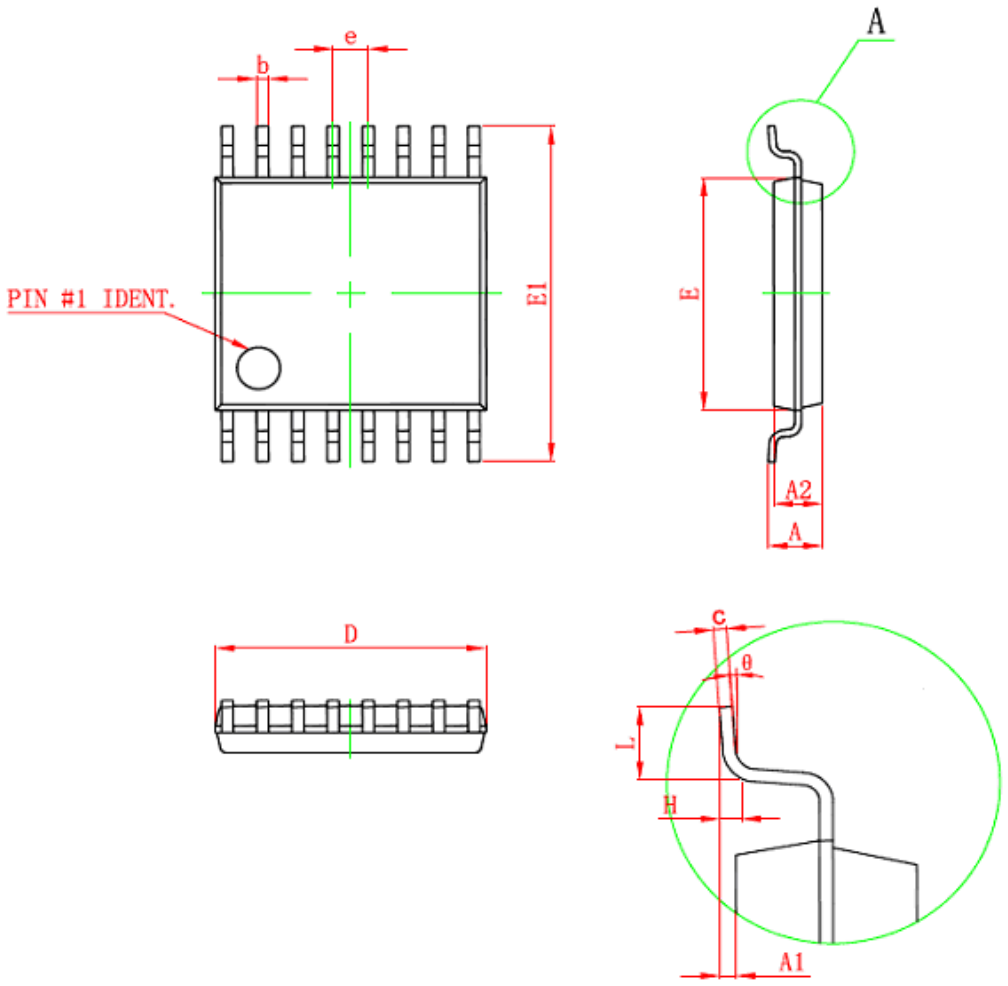
GND of NS2016 is simulate, the pin must be connected to a very clean GND, to avoid to near the ground of micro-controller or digital signal processor . If possible, it would be preferable to connect the converterground to the power supply internal ground (or batteries) . The will be the best to place converter and other analog circuits in the same plane.

In particular, when using resistive touch screen, pay attention to the connection between touch screen and NS2016. Because the resistance of resistive touch screen is relatively small, so the connection betweenNS2016 the screen is as small as possible. Long connection will bring more of the error, which, as the switch on-resistance. In addition, the welding point relaxation, as well as a not solid point will bring the error to theapplication.

In addition to the above, the noise will cause error in other touch screen applications (for example, used theLCD panel backlight) too. EMI noise coupled the noised to touch screen through the LCD panel , causedinstability in output, there are "glitches", and so can not be calibrated. Minimize these errors, there are several possible ways: increasea metal shield at the bottom of the touch screen, shield to ground; respectively, place the filter capacitor between XP,YP,XN,YN and ground; but it must be noted These settings will impactthe touch screen response time , especially in single-ended mode at the same time datat ransmission andrelatively high speed applications.

Physical Size of Chip Package

TSSOP-16 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

Figure 17 TSSOP-16 Pagckage Size

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