NS4168 2.5W-I2S digital input mono class D audio power amplifier

1 NS4168 Features

- Output Power Po:2.5W(VDD=5V, RL=4Ω)
- Operating Voltage:3.0V～5.5V
- 0.2%THD+N（VDD=5V, RL=4Ω, Po=1W）
- 80% efficiency (VDD=5V, RL=4Ω, Po=2.5W)
- Default 12S serial digital audio input interface
- Supports wide range sampling rate: 8kHz~96kHz.
- Left or right channel is available by setting the level of CTRL pin.
- Output NCN function.
- Filterless Class D amplifier.
- Excellent “power on, power off” noise suppression.
- Overcurrent protection, overheat protection and undervoltage protection.
- Available in ESOP-8L and DFN3X3-8L packages.

2 NS4168 Application

- Smart speakers.
- Mini speakers.
- Digital Frames.

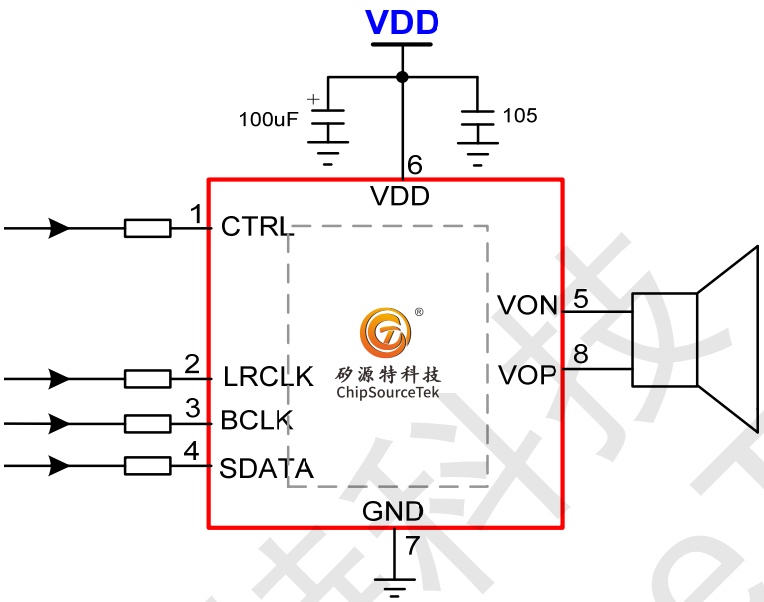
3 NS4168 Description

NS4168 is a mono class D audio power amplifier with I2S serial digital audio input and NCN output. It has built-in digital-to-analog converter (DAC) and multistage Class D modulator for excellent audio performance. Using the NS4168's I2S digital audio serial interface to transmit to the amplifier, the impact of the noise source on the transmitted audio can be significantly reduced. In addition, it also avoids the noise caused by the built-in audio decoding DAC of the MCU master chip, and finally obtains a higher signal-to-noise ratio and a smaller distortion degree. Its closed-loop digital input design retains the advantages of a digital amplifier while providing excellent PSRR and audio performance. Compared to other Class D architectures, the use of spread spectrum pulse density modulation enables lower EMI interference and the highest audio efficiency.

The NS4168 uses a unique NCN function to effectively prevent output signal distortion caused by input signal overload and battery voltage drop, and can effectively protect the speaker from being damaged during high-power output.

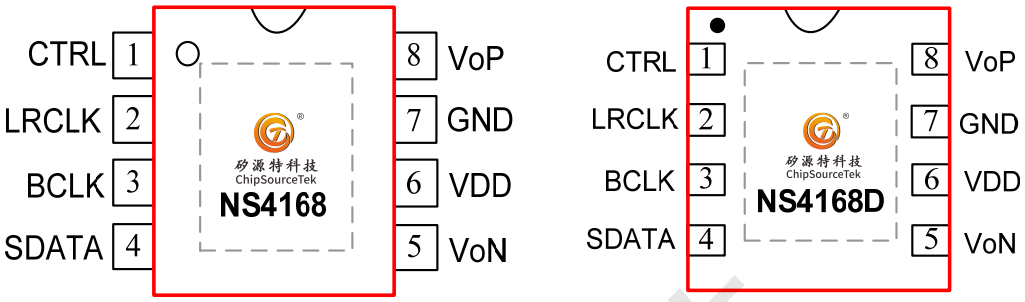
The NS4168 is a mono audio amplifier. The left and right channel selection can be set by CTRL pin level. Stereo products can flexibly choose two chips. The NS4168 has built-in overcurrent protection, overheat protection and undervoltage protection functions, effectively protects the chip from being damaged under abnormal working conditions.

4 NS4168 Typical application



5 NS4168 Pin configuration

The pin diagrams of ESOP-8L and DFN3X3-8L are shown below.



Pin name	No.	Description
1	CTRL	Left and right channel switching control and chip on/off control pin.
2	LRCLK	I2S left and right channel frame clock pin.
3	BCLK	I2S bit clock pin.
4	SDATA	I2S serial data input pin.
5	VoN	Audio amplifier negative output pin.
6	VDD	Power input.
7	GND	Power ground.
8	VoP	Audio amplifier positive output pin.

5.1 Silk screen instruction

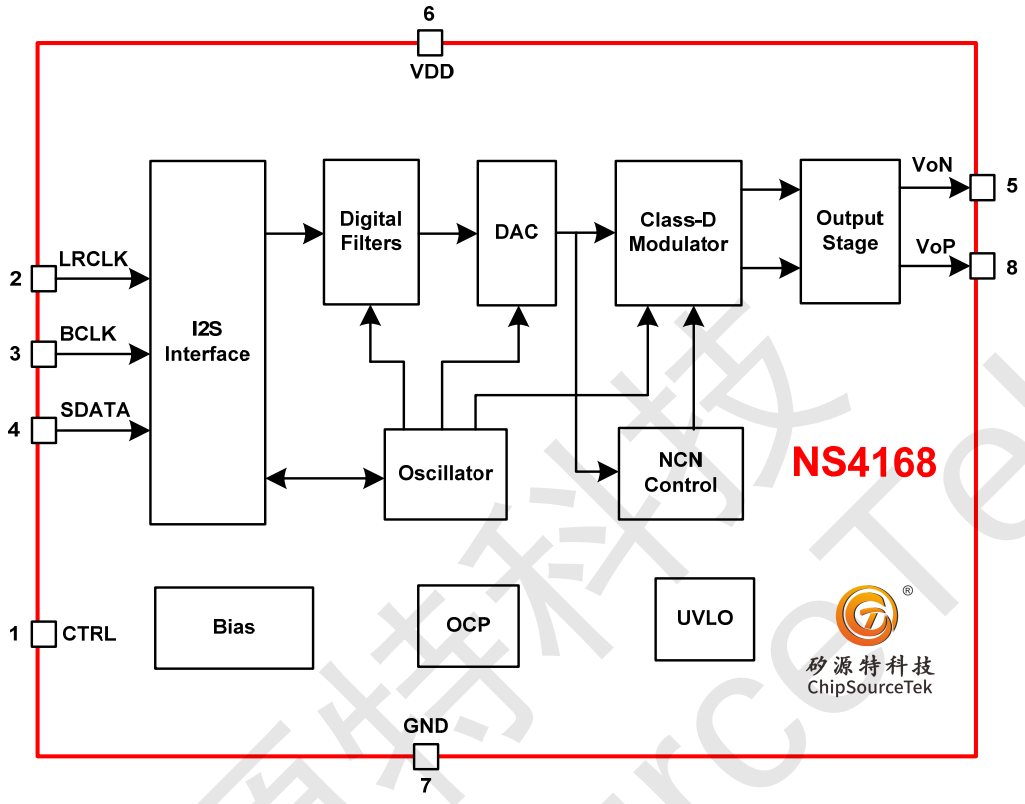
NS4168x
xxxx

The x in NS4168x stands for different package forms.

NS4168D	NS4168
DFN3x3-8L	ESOP-8L

The second line XXXX represents the production cycle. For example, 2206 indicates the packaging test time in Week 6, 2022.

6 NS4168 Structure diagram



7 NS4168 Limit operating parameters

- Power voltage:2.8V ~ 5.0V
- CTRL/LRCLK/BCLK/SDATA -0.3V ~ VDD
- ESD voltage (HBM/MM)4000V/200V
- Operation Temperature: -40℃ ~ +85℃
- Storage temperature: -65℃ ~ +150℃
- TJMAX:+150℃
- Soldering temperature(in 10s): +220℃
- θ_{JC}/θ_{JA}（ESOP8）20/80°C/W

Notes:Over these operating parameters above may result in permanent damages to the chip. Exposure over time at any limit operating conditions may decrease the reliability and lifetime of the chip.

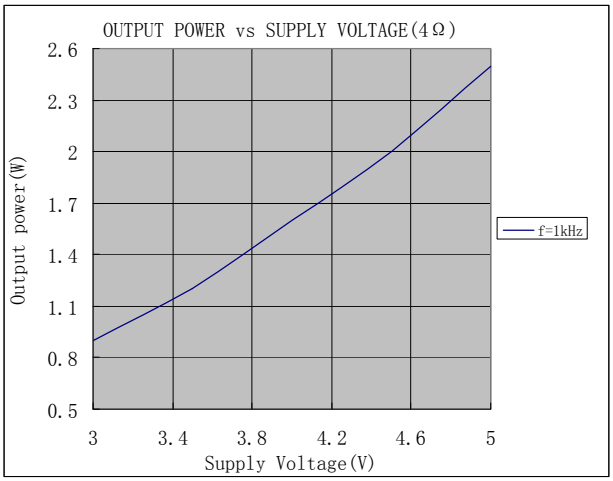
8 NS4168 Electrical characteristics

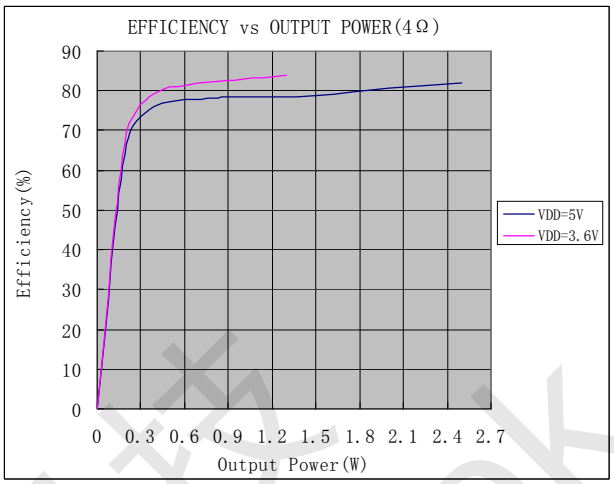
Operating conditions(unless specified)：T=25℃, VDD=5V,f_S=48KHz,I2S default format.

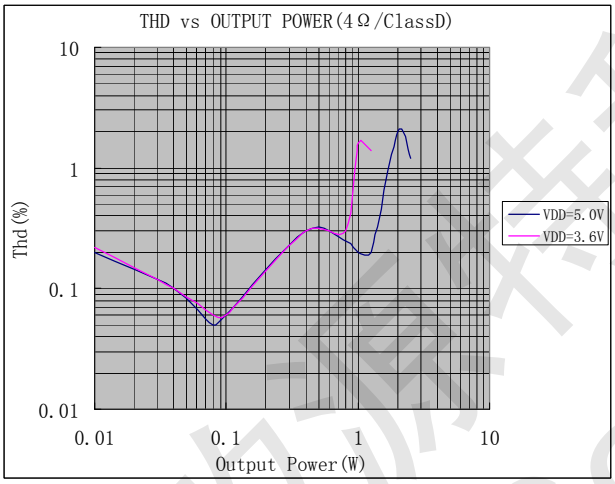
Symbol	Parameter	Test condition	Min.	Stand.	Max	Unit
V_{DD}	power voltage		3		5. 5	V
I_{DD}	power quiescent current	V_{DD} =5.0V, V_{IN}＝0V, No load		13		mA
I_{SD}	shutdown leakage current	V_{CTRL} =0V		1		μA
V_{OS}	output offset voltage			10	40	mV
PSRR	power supply rejection ratio	217Hz			-80	dB
		20KHz			-72	dB
CMRR	common mode rejection ratio			-70		dB
f_{SW}	modulation frequency	V_{DD} =3V to 5.25V		430		kHz
η	efficiency	Po=2.5W,R_L=4Ω, V_{DD}=5V		80		%
V_{CTRL}	CTRL voltage threshold	Right Channel（右声道）	1.5		VDD	V
		Left Channel（左声道）	0.9		1.15	
		Shut-down 低功耗关断	0		0.4	
T_{OFF}	CTRL shutdown time	V_{CTRL}=0V		100		us
t_{AT}	NCN attack time	V_{DD} =3.6V		10		ms
t_{RL}	NCN release time	V_{DD} =3.6V		1.1		s
P_O	Output power	V_{DD} =3.6V, f=1KHz, RL=4Ω, THD+N=10%		1.2		W
		V_{DD} =5.0V, f=1KHz, RL=4Ω, THD+N=10%		2.5		W
THD+N	total distortion + noise	f=1kHz, R_L=4Ω, P_O=1.0W		0.2		%
SNR	Signal to Noise Ratio	RL＝4Ω,Po＝2.0W		85		dB
AMAX	Max. attenuation gain			-10		dB
Digital input/output						
VIH	High input voltage	BCLK/LRCLK/SDATA/CTRL	0.7xV_{DD}		V_{DD}	V
VIL	Low input voltage	BCLK/LRCLK/SDATA/CTRL	-0.3		0.3V_{DD}	V

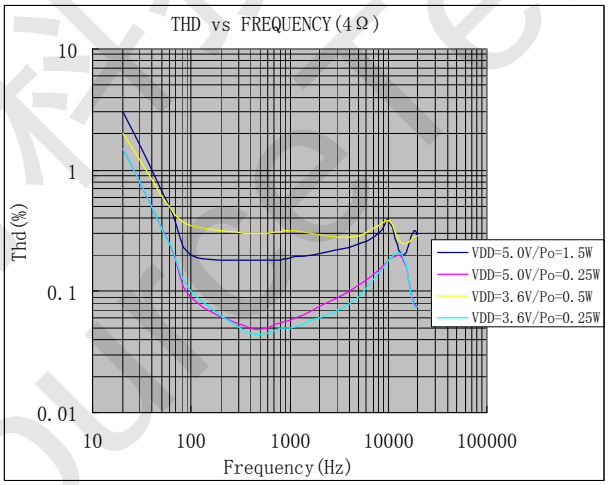
9 NS4168 Typical characteristic curves

In the following characteristic curves, T=25℃(unless specified).









10 NS4168 Application specifications

10.1 Basic structure description

The NS4168 is a digital audio signal input that supports I2S format (BCLK delay one clock) and utilizes an internal bridge power stage to generate PDM differential switching output. The chip has built-in multiple protection functions , and it is a fully integrated digital switching audio amplifier.

10.2 I2S digital input serial audio interface

10.2.1 I2S digital audio format

The NS4168 supports I2S standard digital audio signal input. The standard I2S has 3 main signals: serial clock BCLK, frame clock LRCLK, serial data SDATA. The I2S digital audio format as shown below:

The serial clock BCLK is also called the bit clock, that is, each bit of data corresponding to the digital audio.

The frame clock LRCLK is used to switch the data of the left channel and right channel. A "1" LRCLK indicates that data is being transmitted in the right channel, and a "0" indicates that data is being transmitted in the left channel. The frequency of LRCLK is usually set to the audio signal sampling frequency.

SDATA is serial data that is transmitted over the data line in the form of binary complement in I2S. Transmit the highest bit MSB first. The MSB is transmitted first because the word length of the sending device and the receiving device may be different. When the system word length is longer than the data sending end word length, the data transmission will be truncated, that is, if the data bit received by the data receiving end is longer than its specified word length, all bits after the lowest LSB of the specified word length will be ignored. If the received word length is shorter than the specified word length, then the free bits will be filled with 0. In this way, the highest

significant bit of the audio signal can be transmitted, thus ensuring the best hearing effect.

10.2.2 All timing specifications in I2S digital audio format

The NS4168 is always used as a slave, and it is necessary to pay attention to the send delay and the allowance for the setup time of the receiving device, all timing requirements are related to the clock cycle or the minimum clock cycle allowed by the device.

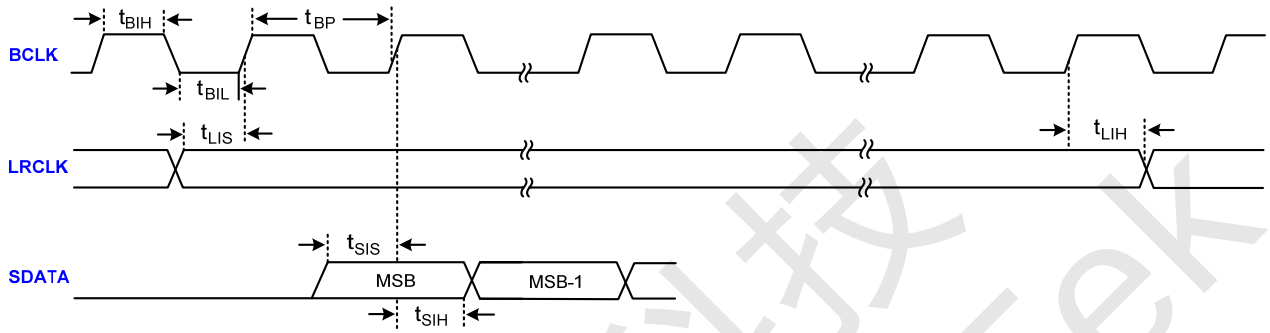


图 2 I²S Serial Audio Interface

Tab.1 Timing parameter table

Parameter	Min.	Unit	Description
t_{BIL}	40	ns	BCLK low level pulse width
t_{BIH}	40	ns	BCLK high level pulse width
t_{LIS}	10	ns	Setting time from LRCLK or SDATA edge to BCLK rising edge
t_{LIH}	10	ns	Holding time from BCLK rising edge to LRCLK or SDATA edge
t_{SIS}	10	ns	Setting time from SDATA to BCLK rising edge
t_{SIH}	10	ns	Holding time from BCLK rising edge to SDATA

10.2.3 Left channel and right channel LRCLK settings

The NS4168 is a mono amplifier, while the standard I2S protocol can transmit left channel signal and right channel signal. The NS4168 selects left channel signal or right channel signal by setting the level of the pin1 (CTRL) pin. The frequency of LRCLK is usually set to the audio signal sampling frequency, but different sampling rates support different BCLK rates (generally MCLK is set to 256fs). The application range of the internal LRCLK clock in the NS4168 chip is 128kHz-6.144MHz (the MCLK clock range is 2.048MHz-24.576MHz). All available options are shown in Table 2.

Tab.2 BCLK rates supported by different sampling frequencies

Sampling frequency Fs	Supported BCLK rates for				
	16Fs	24Fs	32Fs	48Fs	64Fs

8kHz	128kHz	192kHz	256kHz	384kHz	512kHz
16kHz	256KHz	384kHz	512kHz	768kHz	1.024MHz
32kHz	512KHz	768kHz	1.024MHz	1.536MHz	2.048MHz
44.1kHz	705.6KHz	1.058MHz	1.422MHz	2.117MHz	2.822MHz
48kHz	768KHz	1.152MHz	1.536MHz	2.304MHz	3.072MHz
96kHz	1.536MHz	2.304MHz	3.072MHz	4.608MHz	6.144MHz

10.2.4 Input channel selection

The input channel of NS4168 is selected by setting the level of the CTRL pin. Select the left channel when the CTRL pin voltage is 0.9V-1.15V; select the right channel when the CTRL pin voltage is 1.5V-VDD. As shown in the following table.

Tab.3 selection of CTRL voltage and channel

CTRL pin voltage	Channel selection
1.5V-VDD	Right channel
0.9V-1.15V	Left channel
0-0.4V	Shutdown

10.3 NCN function

The NS4168 has NCN function. The NCN function can effectively prevent the output signal distortion caused by the input signal overload or the battery voltage drop, and can effectively protect the speaker from being damaged when the high power output. The principle is that the amplifier automatically detects the output cutting distortion and automatically adjusts the gain of the amplifier to achieve the effect of NCN. As shown in the picture below.

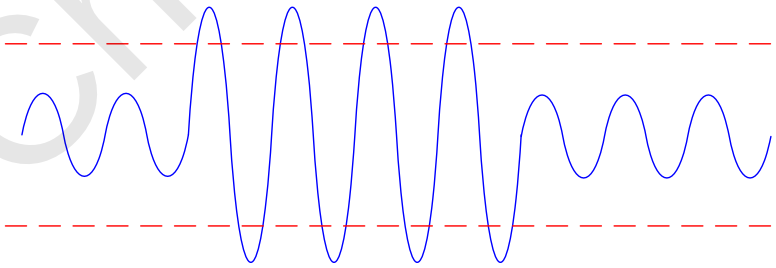


Figure1 The audio output signal is not limited by the supply voltage

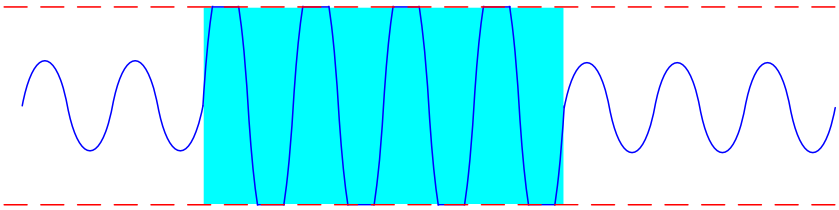


Figure2 The audio output signal is normal mode

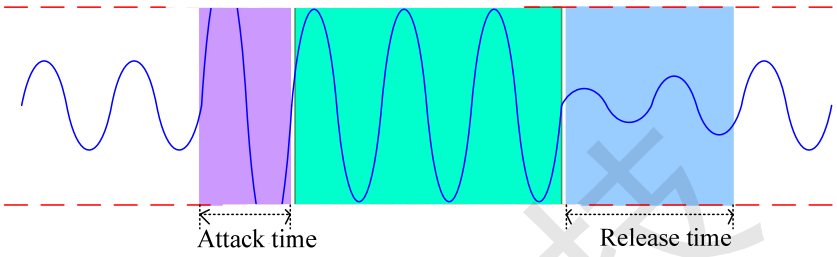


Figure3 The audio output signal is NCNl mode

10.4 Power supply filter capacitor selection

In the application of amplifier, the bypass design of the power supply is very important, especially for the noise performance and the power supply voltage suppression performance in application. In the design, the filter capacitor is required to be as close as possible to the chip power pin. The typical capacitor is a 100uF capacitor in parallel with a 1uF ceramic capacitor.

10.5 Protection circuit

When the chip has a short circuit between the output pin and the power or ground, or a short circuit fault between the outputs, the overcurrent protection circuit will turn off the chip to prevent the chip from being damaged. After the short circuit fault is eliminated, the NS4168 automatically recovers.

10.6 Layout suggesting

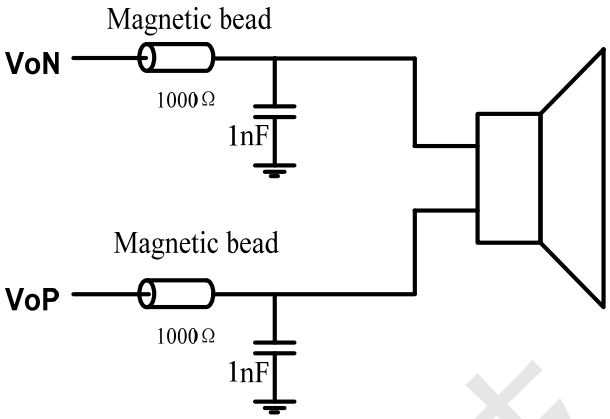
The NS4168 is a Class D amplifier, and EMI interference should be considered when layout. EMI interference can be minimized in the following aspects:

1. The wiring of the power amplifier output to the speaker should be as short and wide as possible, and the output wiring should be as far away from the sensitive signal lines and circuits as possible..

2. The decoupling capacitor of the power amplifier power pin is as close as possible to the chip pin. Power cable, ground wire is best to use the star connection.

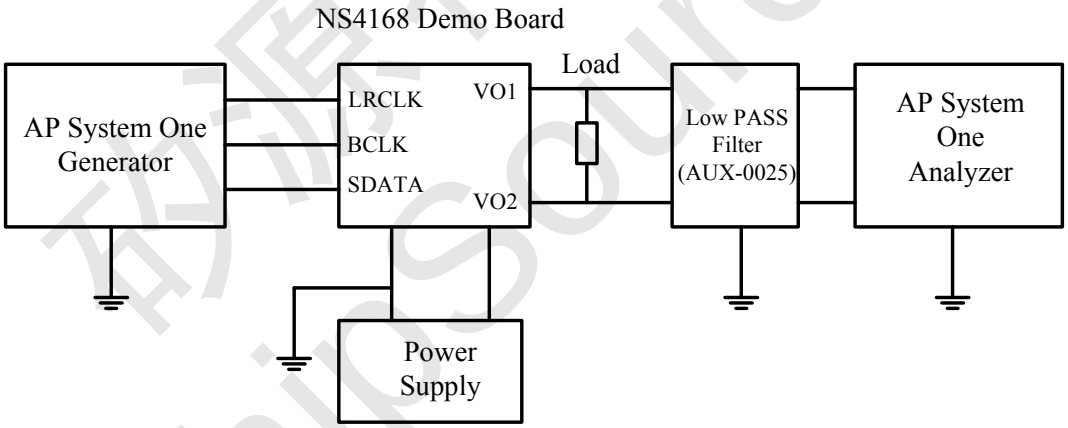
3. Due to space limitations and other reasons, when the application environment is relatively harsh, adding magnetic beads and capacitors at the output end can effectively suppress EMI interference. Use the bead and capacitor as close to the chip pin as possible. The following design reference circuit application is with magnetic

beads and capacitors to the NS4168 output.



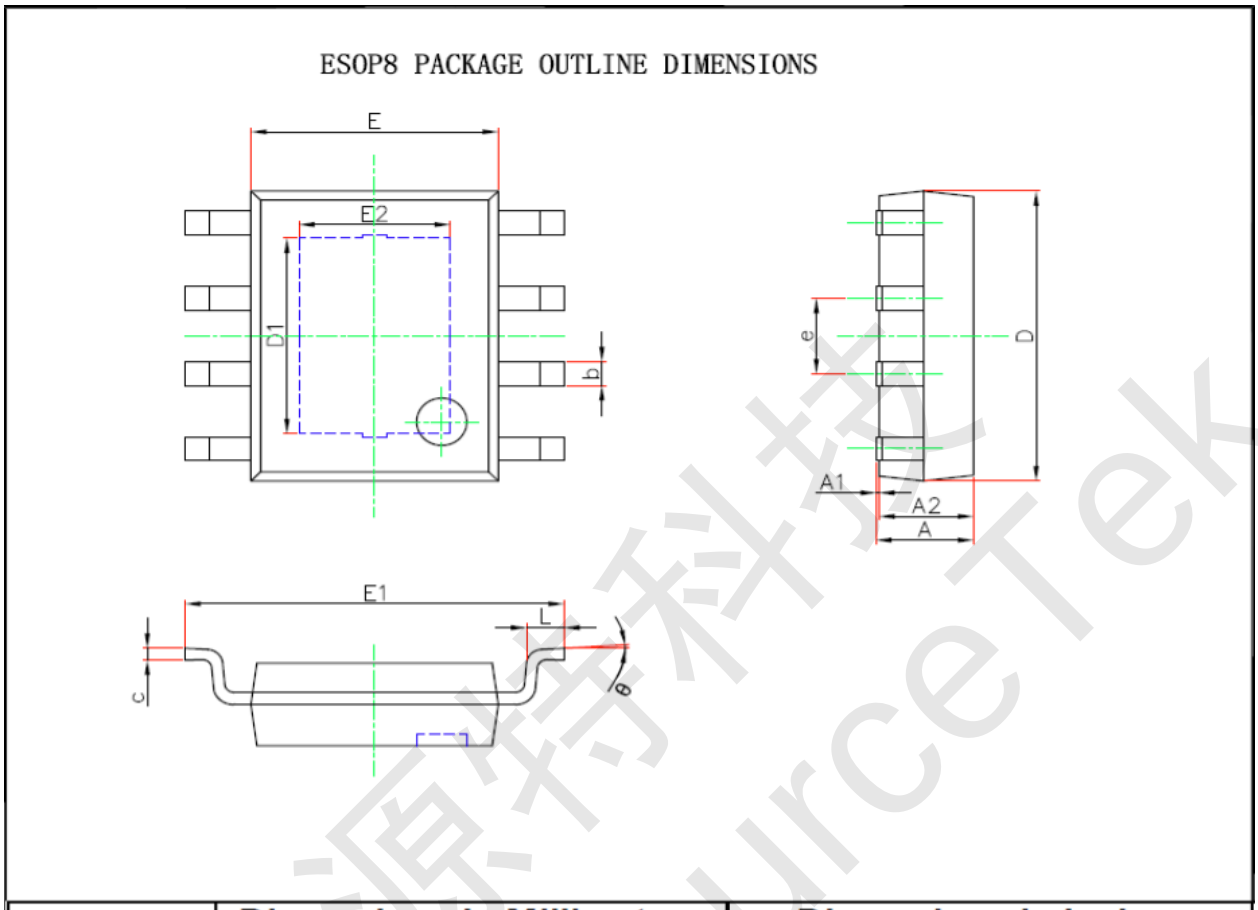
10.7 Test circuit

The NS4168 test circuit is shown below. When measuring a Class D mode power amplifier, a Low PASS Filter is necessary. Two 33uH inductors can be used in series at both ends of the load resistance to be equivalent a speaker. If only pure resistance is used to replace the loudspeaker load, the measured results will be worse than the results when the loudspeaker is loaded, including power, efficiency, distortion and other indicators.



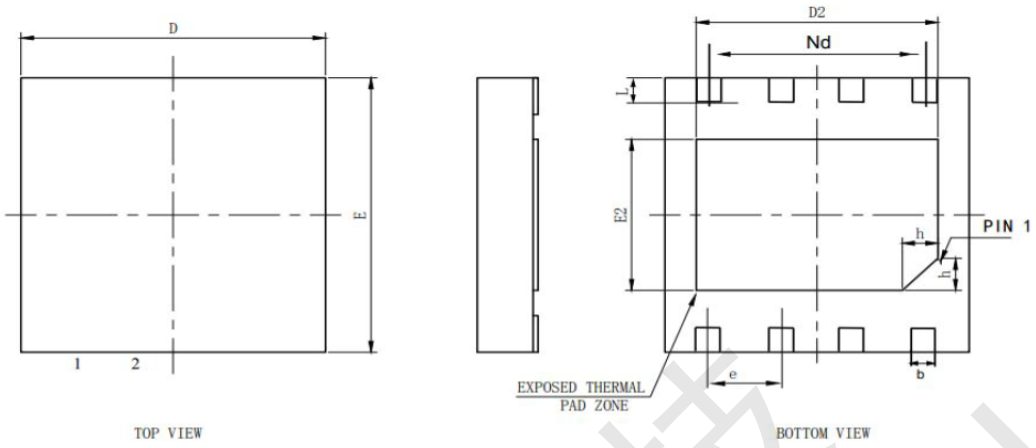
11 NS4168 Packaging information

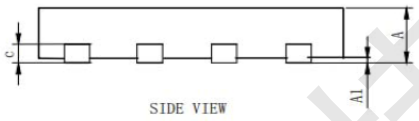
11.1 Dimensional drawing of ESOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.150	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

11.1 Dimensional drawing of DFN3X3X0.75-8L





SYMBOL	MILLIMETER		
	MIN	MID	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 20	0.25	0. 30
c	0. 18	0.20	0. 25
D	2. 90	3. 00	3. 10
D2	2. 20	2. 30	2. 40
e	0. 65BSC		
E	2. 90	3. 00	3. 10
E2	1. 40	1. 50	1. 60
L	0. 20	0.25	0. 30
h	0. 30	0. 35	0. 40
Nd	1. 95BSC		
L/F载体尺寸	2. 70*2. 10		

12 Revision history

Declaration: Shenzhen Zhiyuan Technology Co., Ltd. has the right to modify the product Information and specifications are updated at any time without prior notice. The interpretation right of this manual belongs to our company, and we are responsible for the final interpretation