NSA2302

General Sensor Conditioner with Digital Temperature Calibration

Datasheet (EN) 1.2

Product Overview

The NSA2302 is a highly integrated, low power high precision sensor conditioner for general resistive bridge sensors, which features a low noise instrument amplifier, a low power 24-bit Σ-Δ ADC, a digital sensor calibration DSP and a 12-bit DAC. The NSA2302 can provide an on-chip digital compensation of sensor offset, gain, temperature drift and non-linearity based on the internal EEPROM. Multiple temperature sensing methods are supported by NSA2302 for sensor's temperature calibrating. Once calibrated, the pin VOUT can provide a absolute or ratiometric analog output, and I²C, SPI and one wire (OWI) interfaces are supported for chip configuration, sensor calibrating and digital output.

Key Features

- Ultra-low power down current (< 0.2μA @ 25℃)
- Instrumental amplifier with variable gain from 1X to 256X
- 24-bit ADC for primary signal measurement
- Internal and external temperature sensor supported
- 12-bit DAC
- Multiple OSR settings
- Sensor calibration logic
- 32 bytes EEPROM
- Ratiometric or absolute voltage output
- Frequency output
- Special OWI communication
- SPI/I²C
- Sensor diagnostic logic
- High voltage regulator with external JFET
- RoHS & REACH compliance

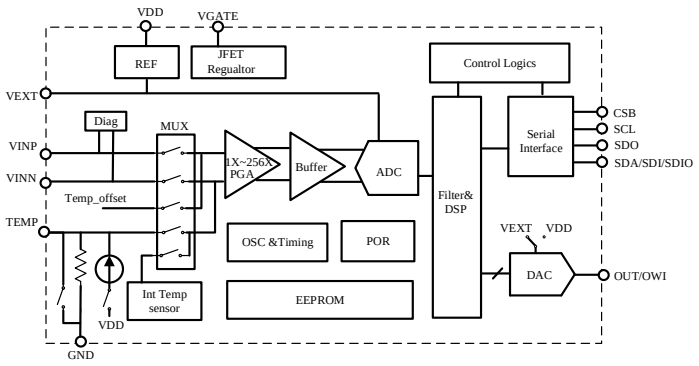
Applications

- Pressure sensor conditioner
- Strain gauge interface
- Industry process control

Device Information

Part Number	*Package*	*Body Size*
NSA2302-W	Bare die	1270μm×1437μm
NSA2302_QMOR	MSOP10 package	3.1mm×5.05mm

Functional Block Diagrams



1. Pin Configuration and Functions

The NSA2302 is offered either via bare die or MSOP-10 Package. The pad location of bare dies is shown in Figure 1.1 and Table1.1.

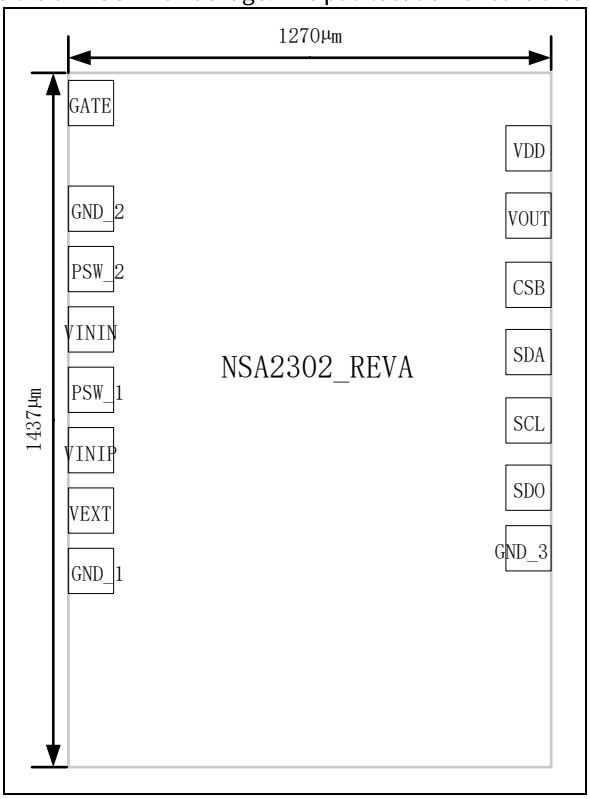


Figure1.1 NSA2302 Pad Location

Table1.1 NSA2302 Pin Location

Pin Number	*X Coordinate(um)*	*Y Coordinate(um)*	*PAD Name*
1	58.95	416.885	GND_1
2	58.95	516.885	VEXT
3	58.95	616.885	VINIP
4	58.95	716.885	PSW_1
5	58.95	816.885	VININ
6	58.95	916.885	PSW_2
7	58.95	1016.885	GND_2
8	58.95	1309.675	GATE
9	1220.92	1306.725	VDD
10	1220.92	1166.725	VOUT
11	1220.92	1036.725	CSB
12	1220.92	906.725	SDI

13	1220.92	776.725	SCL
14	1220.92	646.725	SDO
15	1220.92	516.725	GND_3

The die information is shown in Table1.2.

Table 1.2 Die Information

Die Size (without scribe line)	1270μm*1437μm
PAD Opening	65μm*65μm

The NSA2302 PAD description is shown in Table1.3.

Table 1.3 NSA2302 PAD Description

Bare Die Pin No.	***Symbol***	***Type***	***Function***
1	GND_1	Analog input	Ground supply
2	VEXT	Analog output	Excitation voltage for Mass sensor
3	VINIP	Analog input	Positive analog Input Pins
4	PSW_1	Analog output	Low-side power switch connection for pressure sensor
5	VININ	Analog input	Negative analog Input Pins
6	PSW_2	Analog output	Low-side power switch connection for pressure sensor
7	GND_2	Analog input	Ground supply
8	GATE	Analog input	JFET regulator control signal
9	VDD	Power supply	Power supply for both core
10	VOUT	Analog output / Digital Input	DAC output / One Wire Interface/Frequency output
11	CSB	Digital input	Chip select
12	SDI	Digital input	Serial data input/output in I2C mode (SDA) Serial data input in 4-wire SPI mode (SDI) Serial data input/output in 3-wire SPI mode (SDIO)
13	SCL	Digital input	Serial clock
14	SDO	Digital output	Serial data output in 4-wire SPI mode Address select in I^2C mode
15	GND_3	Analog input	Ground supply
16	VDDIO	Power supply	Power supply for I/O circuits

The NSA2302 is also offered MSOP-10 Package.NSA2302 Pin Configuration and Description is shown in Table1.4

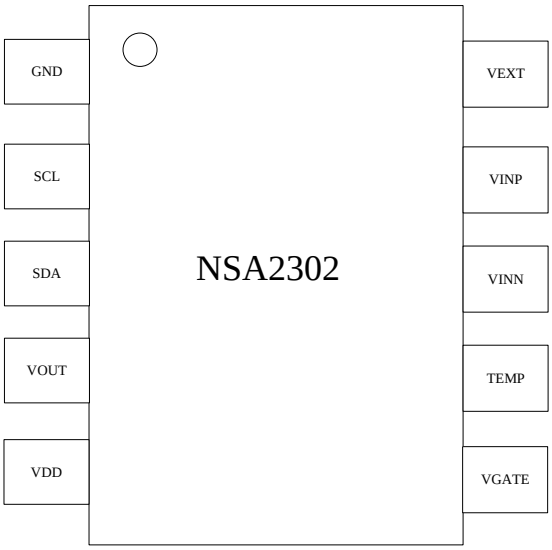


Figure 1.2 NSA2302 MSOP10 Package

Table 1.4 NSA2302 Pin Configuration and Description

Pin Name	*MSOP-10 Pin*	*Type*	*Description*
GND	1	Analog input	Ground supply
SDO/ADDR	N/A	Digital output	Serial data output in 4-wire SPI mode Address select in I^2C mode
SCL	2	Digital input	Serial clock
SDA	3	Digital input	Serial data input/output in I^2C mode (SDA) Serial data input in 4-wire SPI mode (SDI) Serial data input/output in 3-wire SPI mode (SDIO)
CSB	N/A	Digital input	Chip select
OUT/OWI	4	Analog output / Digital Input	DAC output / One Wire Interface/Frequency output
VDD	5	Power supply	Power supply for both core and IO circuits;
VGATE	6	Analog input	JFET regulator control signal
TEMP	7	Analog input	External temperature input pin with bridge switch
VINN	8	Analog input	Negative analog Input Pins
VINP	9	Analog input	Positive analog Input Pins
VEXT	10	Analog output	Excitation voltage for Mass sensor

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	VDDmax	-0.3		6.5	V	
VGATE Voltage	VGATEmax	-0.3		7.5	V	
Analog pin voltage		-0.3		VDD+0.3	V	
Analog pin current				25	mA	
Digital pin voltage		-0.3		VDD+0.3	V	25°C
Storage temperature		-60		150	°C	

3. ESD Rating

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 Rev E ● All other pins to VDD ● All other pins to GND ● IO pins to IO pins	±2	kV
	Charged device model (CDM), per AEC-Q100-011 Rev D ● All pins	±500	V

4. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Supply/Regulation						
Supply Voltage	VDD	3	5	5.5	V	Power supply on VDD pin
JFET output voltage	VDD_JFET		5.5		V	High voltage power supply through JFET
Power on Reset	V_{POR_VDD}		2		V	POR threshold as power up
Supply Current (Sensor not included)	I_{DD1}		1.8		mA	0~5V voltage output DAC on
	I_{DD2}		1.6		mA	Digital output, DAC off
	Icmd			200	nA	standby current
Reference Voltage						
Reference output	VEXT		3.6 or 2.4		V	'Regulator_sel' = 0 or 1
Load on VREF	R_{VREF}	0.5			kohm	
VREF Current Limit	I_{VREF_limit}		20		mA	Short to Ground
Primary Signal Measurement Channel						
PGA Gain	GAIN	1		256		

PGA Gain Error	GAINP_ERR			3%		
Zero Offset	Offset			300	μV	
PADC Resolution	RES_P		24		Bits	
Effective Resolution	ENOB_P	refer to Table 6.1			Bits	Depends on Gain & OSR
Input Common Mode Rejection	CMRR		120		dB	
Power Supply Rejection	PSRR	90	120		dB	
Temperature Measurement Channel (Internal and External Temperature Sensor)						
TADC Resolution	RES_T		24		Bit	
TADC Gain	GAIN_T	1		256		External temperature sensor
Effective Resolution	ENOB_T	refer to Table 6.2			Bits	
Error of Internal Temperature Sensor				±3	℃	-40 to 125℃
Internal Resistance for temperature sensor	R_{T-RES}		6		kohm	
Analog Pins						
Absolute Voltage of Input Pins	VINP, VINN	GND+0.4		VDD-1.2	V	PGA on (Gain >2)
		GND+0.1		VDD-0.1		PGA off, Buffer on
		GND-0.1		VDD+0.1	V	PGA off, Buffer off
Differential Input Ranges (V_{offset}+V_{sp})	V_{range}		±VREF /GAIN		V	
Input Pin Leakage	$I_{leakage}$			±1	nA	
DAC						
Resolution			12		Bit	
DAC Full Scale	V_{FS}	0-VDD or 0-1.5*VEXT				Vout_sel = 0 or 1
DNL				0.5	LSB	
INL				1	LSB	
DAC Output RMS noise	V_{rms}		0.5		mV	
Rload of DAC buffer	R_{load}	1			kohm	Voltage output mode
Cload of DAC	C_{load}			15	nF	Voltage output mode
Short Current Limit			20		mA	Short to VDD or GND
Upper output limit		3/4		1	VFS	Set by DAC_LIMIT_H<5:0>
Lower output limit		0		1/4	VFS	Set by DAC_LIMIT_L<5:0>

Diagnosis						
Burnout Current	I_{diag}		100		nA	
OSC						
ADC Clock	FOSC_MOD		1000		kHz	
Clock Rate Error	FOSC_ERR	-15%		15%		-40~125℃
Frequency Output						
Frequency Output	Freq	0		250	kHz	Depends on Freq_FS<1:0>
EEPROM						
Programming Temperature	T_{EEP}	-40		105	℃	
Programming Supply Voltage	V_{EE}	3		5.5	V	
Time for EEPROM programming	t_{EEP}		0.8		s	
Endurance			10		k	
Date Retention		10			A	@125℃
Serial Interface						
Serial Clock Frequency	F_{sclk}			10	MHz	SPI Interface
				400	kHz	I^2C Interface
				50	kHz	OWI Interface

5. Registers

All the NSA2302 registers can be departed into normal registers and EEPROM registers. The normal registers are used to send a conversion command to the NSA2302, read back the conversion data and perform the EEPROM blowing. The EEPROM registers are used to store the configurations and calibration coefficients for the NSA2302, whose default values can be programmed by the inside EEPROM banks.

5.1. Normal Registers

IF_CTRL(R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x00	7, 0	SDO_ACTIVE	1'b1 1'b1	Set either of these two bits to 1 for SPI-wire: 0: SPI3-wire 1: SPI4-wire (SDO as serial output)
	6, 1	LSB_FIRST	1'b0 1'b0	Set either of these two bits to 1 for SPI LSB first: 0: SPI MSB first 1: SPI LSB first

	5, 2	SOFTRESET	1'b0 1'b0	Set either of these two bits to 1 to reset the chip. Return to 0 after reset.

Part ID (Read only)

Address	Bit	Register Name	Default	Description
0x01	7, 0	Part_ID<7:0>	0x00	Chip ID, configured by EEPROM register 0xA0

Data-Ready (Read only)

Address	Bit	Register Name	Default	Description
0x02	7 – 2	ERROR_CODE<5:0>	6'b00000	Bit7 = 1: VINP open or short to VDD Bit6 = 1: VINP short to GND Bit5 = 1: VINN open or short to VDD Bit4 = 1: VINN short to GND Bit3 = 1: Positive signal out of range Bit2 = 1: Negative signal out of range
	0	DRDY	1'b0	1: Set after a new data updated and automatically cleared after a register reading to PDATA/TDATA or before the next data's coming.

PDATA (Read only)

Address	Bit	Register Name	Default	Description
0x06	7 – 0	Data_out<23:16>	0x00	Signed, 2's complement: When 'RAW_P' = 1, stores the ADC output of primary channel or temperature channel, When 'RAW_P' = 0, stores the calibrated primary channel data.
0x07	7 – 0	Data_out<15:8>	0x00	
0x08	7 – 0	Data_out<7:0>	0x00	

TDATA (Read only)

Address	Bit	Register Name	Default	Description
0x09	7 – 0	Temp_out<15:8>	0x00	Signed, 2's complement: When 'RAW_T' = 1, data is meaningless. When 'RAW_T' = 0, stores the calibrated temperature data, LSB = 1/2^16 ℃.
0x0a	7 – 0	Temp_out<7:0>	0x00	

COMMAND (R/W, command register)

Address	Bit	Register Name	Default	Description
0x30	7 – 4	Sleep_time<3:0>	4'b0000	4'b0000: 62.5ms, 4'b0001: 125ms, ... 4'b1111: 1s. only active during sleep mode conversion
	3	Sco	1'b0	1: Start of conversion, automatically come back to 0 after conversion ends (except sleep mode conversion).
	2 – 0	CMD<3:0>	3'b000	3'b000: Single temperature signal conversion. 3'b001: Single sensor signal conversion. 3'b010: Combined conversion (once temperature conversion immediately followed by once sensor signal conversion).

				3'b011: Sleep mode conversion (periodically perform once combined conversion with an interval time of 'sleep_time').

QUIT_OWI (Write only)

Address	Bit	Register Name	Default	Description
0x61	7 – 0	QUIT_OWI <7:0>	0x00	Write '0x5D' to this register to quit OWI communication and enter voltage output mode; Write '0x89' to this register to quit OWI communication and enter vout high-Z mode;

QUIT_OWI_CNT (R/W)

Address	Bit	Register Name	Default	Description
0x62	7 – 0	QUIT_OWI_CNT<7:0>	0x00	Time for temporary quit OWI communication Mode. 0x00: Quit forever, 0x01: 50ms, 0x02: 100ms … 0xFF: 12.8s

EE_Address (R/W)

Address	Bit	Register Name	Default	Description
0x6a	7 – 5	EE_pwr_on<2:0>	3'b000	Write 3b'010 to these bits to before EEPROM Programming.
	4 – 0	EE_prog_address	5'b00000	EEPROM register address to be programmed in manual mode

Blow_Data (R/W)

Address	Bit	Register Name	Default	Description
0x6b	7 – 0	Programmed data<7:0>	0x00	EEPROM register data to be programmed in manual mode

Blow_Start (R/W)

Address	Bit	Register Name	Default	Description
0x6c	7 – 2	Blow_start<5:0>	0x00	Write '6b'011010' to these bits to start EEPROM Programming.
	1	Blow_mode	1b'0	EEPROM programming mode 1: auto mode 0: manual mode

5.2. EEPROM Registers

ID0 (R/W)

Address	Bit	Register Name	Default	Description
0xa0	7 – 0	ID0<7:0>	0x00	ID0 register

ID1 (R/W)

Address	Bit	Register Name	Default	Description
0xa1	7 – 0	ID1<7:0>	0x00	ID1 register

Coarse_Coeff (R/W)

Address	Bit	Register Name	Default	Description
0xa2	7 – 3	Coarse_off<7:3>	5'b00000	LSB = 1/16. Range (-1, +1)
	2 – 0	Coarse_gain<2:0>	3'b000	3'b000: 1X, 3'b001: 1.5X, 3'b010: 2X, 3'b011: 3X, 3'b100: 4X, 3'b101: 6X, 3'b110: 8X, 3'b111: 12X

Chip_Address (R/W)

Address	Bit	Register Name	Default	Description
0xa3	7	Ex_addr_en	1'b0	When Ex_addr_en = 1, and INT_en = 0, I2C address is decided by Chip_address<6:1> and SDO pin; In other cases, I²C address is decided by Chip_address<6:0>.
	6 – 0	Chip_address<6:0>	6'b000000	

SYS_Config1 (R/W)

Address	Bit	Register Name	Default	Description
0xa4	5	OWI_PP	1'b0	1: Set OWI as Push-Pull style 1: Set OWI as Open-Drain style.
	4	Serial_filter_en	1'b0	1. Enable de-glitch filter inside SCL/SDA pins
	3	INT_en	1'b0	1. Enable Data ready interruption (through SDO pin, active low)
	2	Freq_out_en	1'b0	1: Enable frequency output mode
	1 – 0	Freq_FS<1:0>	2'b00	2'b00: Freq_FS = Fclk/4 (250kHz) 2'b01: Freq_FS = Fclk/8 (125kHz) 2'b10: Freq_FS = Fclk/16 (62.5kHz) 2'b11: Freq_FS = Fclk/32 (31.25kHz)

SYS_Config2 (R/W)

Address	Bit	Register Name	Default	Description
0xa5	7	DAC_on	1'b0	1: Enable voltage output mode
	6	Thermopile_mode	1'b0	1: Enable thermopile mode, VIN is connected to VEXT*9/16.
	5	Reserved	1'b0	Reserved
	4	Vout_sel	1'b0	1: Absolute voltage output mode, output range 0~1.5*VEXT 0: Ratiometric voltage output mode, output range 0~VDD
	3	Regulator_sel	1'b0	1: VEXT = 2.4V 2: VEXT = 3.6V
	2	Input_swap	1'b0	1: Swap the polarity of inputs of PADC
	1	Raw_data_on	1'b0	1: Update raw ADC data into 'PDATA' register. Only active in Single sensor signal conversion and Single temperature signal conversion. 0: Update calibrated sensor data into 'PDATA' register.
	0	Diag_on	1'b0	1: Enable sensor diagnostic function.

PCH_Config (R/W)

Address	Bit	Register Name	Default	Description
0xa6	7	Reserved	1'b0	Reserved
	6 – 3	GAIN_P<3:0>	4'b0000	Primary Channel Gain 4'b0000:1X, 4'b0001:2X, 4'b0010:4X, 4'b0011:6X, 4'b0100:8X, 4'b0101:12X, 4'b0110:16X, 4'b0111:24X, 4'b1000:32X, 4'b1001:48X, 4'b1010:64X, 4'b1011:96X, 4'b1100:128X, 4'b1101:192X, 4'b1110:256X, 4'b1111:1X and disable buffer.
	2 – 0	OSR_P<3:0>	4'b0000	PADC OSR setting 3'b000:256X, 3'b001:512X, 3'b010:1024X, 3'b011:2048X, 3'b100:4096X, 3'b101:8192X, 3'b110:16384X, 3'b111:32768X

TCH_Config (R/W)

Address	Bit	Register Name	Default	Description
0xa7	7	Temp_sel	1'b0	1: internal temperature sensor selected 2: external temperature sensor selected (TEMP pin incorporates a 6 kΩ pull down resister)
	6 – 3	GAIN_T<3:0>	4'b0000	TADC output gain 4'b0000:1X, 4'b0001:2X, 4'b0010:4X, 4'b0011:6X, 4'b0100:8X, 4'b0101:12X, 4'b0110:16X, 4'b0111:24X, 4'b1000:32X, 4'b1001:48X, 4'b1010:64X, 4'b1011:96X, 4'b1100:128X, 4'b1101:192X, 4'b1110:256X, 4'b1111:1X and Buffer disabled.
	2 – 0	OSR_T<2:0>	3'b000	TADC OSR setting 3'b000:256X, 3'b001:512X, 3'b010:1024X, 3'b011:2048X, 3'b100:4096X, 3'b101:8192X, 3'b110:16384X, 3'b111:32768X

CLAMPH (R/W)

Address	Bit	Register Name	Default	Description
0xa8	7 – 6	DAC_limit_h<1:0>	2'b00	Set clamping high level.
	5 – 4	DAC_limit_l<1:0>	2'b00	Set clamping low level.
	3 – 0	T_ref_trim<3:0>	4'b0000	Set the reference voltage of external temperature sensor 4'b0000: 8/15*VEXT, 4'b0001: 9/15*VEXT, 4'b0010: 10/15*VEXT, 4'b0011: 11/15*VEXT, 4'b0100: 12/15*VEXT, 4'b0101: 13/15*VEXT, 4'b0110: 14/15*VEXT, 4'b0111: VEXT, 4'b1000: 0V, 4'b1001: 1/15*VEXT, 4'b1010: 2/15*VEXT, 4'b1011: 3/15*VEXT, 4'b1100: 4/15*VEXT, 4'b1101: 5/15*VEXT, 4'b1110: 6/15*VEXT, 4'b1111: 7/15*VEXT

CLAMPL (R/W)

Address	Bit	Register Name	Default	Description
0xa9	7 – 4	DAC_limit_h<5:2>	2'b00	Set clamping high level.
	3 – 0	DAC_limit_h<5:2>	2'b00	Set clamping low level.

MT0 (R/W)

Address	Bit	Register Name	Default	Description
0xaa	7 – 0	MT0<15:8>	0x00	Sensor calibration coefficient, offset coefficient of external temperature sensor , LSB = 1/2^15, Range (-1, +1)
0xab	7 – 0	MT0<7:0>	0x00	

KT (R/W)

Address	Bit	Register Name	Default	Description
0xac	7 – 0	KT<15:8>	0x00	Sensor calibration coefficient: sensitivity coefficient of external temperature sensor, KT: LSB = 1/2^10, Range (-32, +32)
0xad	7 – 0	KT<7:0>	0x00	

OFFSET0 (R/W)

Address	Bit	Register Name	Default	Description
0xae	7 – 0	CNT_OFF<15:8>	0x00	Sensor Calibration coefficient, offset at T0. LSB = 1/2^15. Range (-1, +1)
0xaf	7 – 0	CNT_OFF<7:0>	0x00	

CTC1 (R/W)

Address	Bit	Register Name	Default	Description
0xb0	7 – 0	CTC1<15:8>	0x00	Sensor Calibration coefficient, the 1st order temperature coefficient of offset. LSB = 1/2^22. Range (-0.00781, +0.00781)
0xb1	7 – 0	CTC1<7:0>	0x00	

CTC2 (R/W)

Address	Bit	Register Name	Default	Description
0xb2	7 – 0	CTC2<11:4>	0x00	Sensor Calibration coefficient, the 2nd order temperature coefficient of offset. LSB = 1/2^27, Range (-6.1e-5, 6.1e-5)
0xb3	7 – 4	CTC2<3:0>	4'b0000	

S0 (R/W)

Address	Bit	Register Name	Default	Description
0xb3	3 – 0	S0<13:10>	4'b0000	Sensor calibration coefficient, sensitivity at T0. LSB = 1/2^13 (unsigned), Range (0, 2)
0xb4	7 – 0	S0<9:2>	0x00	
0xb5	7 – 6	S0<1:0>	2'b00	

STC1 (R/W)

Address	Bit	Register Name	Default	Description
0xb5	5 – 0	STC1<13:8>	0x00	Sensor Calibration coefficient, the 1st order temperature coefficient of sensitivity. LSB = 1/2^20. Range (-0.00781, +0.00781)
0xb6	7 – 0	STC1<7:0>	0x00	

STC2 (R/W)

Address	Bit	Register Name	Default	Description
0xb7	7 – 0	STC2<9:2>	0x00	Sensor Calibration coefficient. the 2nd order temperature coefficient of sensitivity. LSB = 1/2^25, Range (-1.5e-5, 1.5e-5)
0xb8	7 – 6	STC2<1:0>	2'b00	

KS (R/W)

Address	Bit	Register Name	Default	Description
0xb8	5 – 0	KS<9:4>	6'b000000	Sensor calibration coefficient, the 2nd order nonlinearity coefficient, LSB = 1/2^11, Range (-0.25, +0.25)
0xb9	7 – 4	KS<3:0>	4'b0000	

KSS (R/W)

Address	Bit	Register Name	Default	Description
0xb9	3 – 0	KSS<9:6>	4'b0000	Sensor calibration coefficient, the 3rd order nonlinearity coefficient, LSB = 1/2^11, Range (-0.25, +0.25)
0xba	7 – 2	6'b000000	6'b000000	

KS_Scale (R/W)

Address	Bit	Register Name	Default	Description
0xba	1	KS_scale	1'b0	Multiply the 2nd order nonlinearity coefficient by 4, LSB = 1/2^9, Range (-1, +1)

KSS_Scale (R/W)

Address	Bit	Register Name	Default	Description
0xba	0	KSS_scale	1'b0	Multiply the 3rd order nonlinearity coefficient by 4, LSB = 1/2^9, Range (-1, +1)

B0 (R/W)

Address	Bit	Register Name	Default	Description
0xbb	7 – 0	B0 <15:8>	0x00	Sensor calibration coefficient: reference pressure point for nonlinearity calibration, LSB = 1/2^15, Range (-1, 1)
0xbc	7 – 0	B0 <7:0>	0x00	

6. Functional Description

The NSA2302 is a highly integrated sensor conditioner for voltage output sensors like Wheatstone bridge pressure sensor, thermocouple and strain gauge. The chip incorporates five parts: analog front-end module, digital module, analog output module, power supply module and serial interfaces. The block diagram of the NSA2302 is shown in Figure 6.1.

The analog front-end module includes a primary signal measurement channel with an instrumental amplifier followed by a 24-bit ∑Δ ADC, an internal temperature sensor and a digital filter, for precision sensor signal measurement.

The digital module is composed of registers, EEPROM, control logic, and a built-in DSP. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2nd order temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3rd order. The configuration parameters and coefficients for calibration are stored at in the EERPOM of 32 bytes.

The analog output module includes a 12-bit DAC and a flexible configurable output driver which can be configured to support voltage output modes and frequency output.

The power supply module includes a sensor voltage driver and a high voltage JFET regulator.

The NSA2302 supports three serial interfaces: SPI, I²C and OWI, writing and reading registers of configuration, calibration coefficients and data.

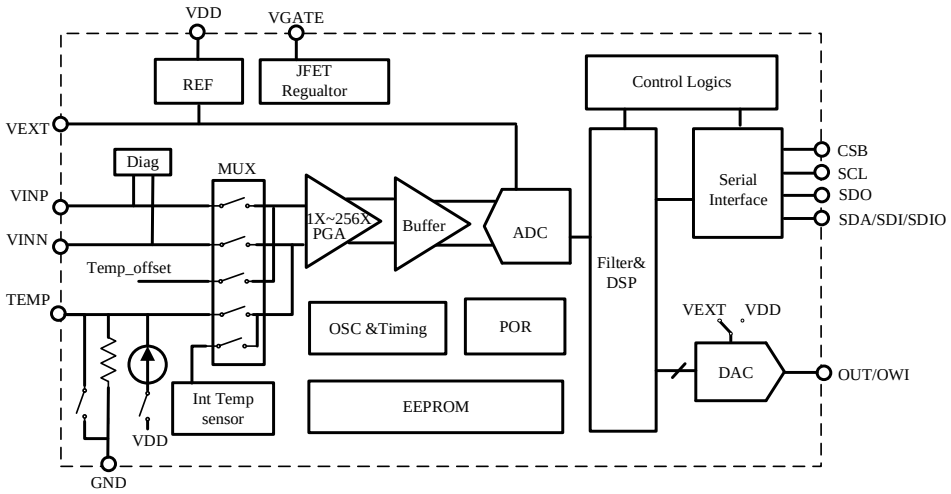


Figure 6.1 NSA2302 Block Diagram

6.1. Analog Front-end Module 1: Primary Signal Channel

The primary signal measurement channel includes an instrumental PGA, 24-bit sigma-delta ADC (PADC) followed by digital filters.

6.1.1. PGA+ADC

The PGA is a gain programmable instrumental amplifier, with its gain configurable to 1X, 2X, 4X, 6X, 8X, 16X, 24X, 32X, 48X, 64X, 96X, 128X, 192X, 256X. The PADC performs the analog to digital conversion. The output of the ADC is digital filtered with 24-bit resolution. The reference voltage of the ADC is VEXT, and the allowable differential input range is ±VEXT/GAIN_P. The PADC output can be expressed by the following equation:

$$PDATA_{RAW} = \frac{VINP - VINN}{VEXT} * GAIN\_P * 2^{23}$$

PDATARAW can be read out from 'PDATA' registers (Reg0x06-Reg0x08) only when 'RAW_P' is set to 1; otherwise, the built-in DSP calibrates the sensor using the calibration coefficients and temperature data stored in 'TDATA' and put the calibrated digital output of the primary channel onto the 'PDATA' registers.

6.1.2. The Input Common-mode Voltage of PGA

The PGA is of differential input and differential output. The output voltages of the PGA can be express as:

$$VP\_PGA = VCMin + GAIN\_P * VDin/2$$

$$VN\_PGA = VCMin - GAIN\_P * VDin/2$$

VCMin and VDin in above formula are the common-mode voltage and differential voltage of the PGA input voltage. To avoid the saturation of the amplifiers, both VP_PGA and VN_PGA should meet the follow limitation:

$$\mathrm{AGND} + 0.1\mathrm{V} < \mathrm{VP(N)\_PGA} < \mathrm{VDD} - 0.1\mathrm{V}$$

From above, the input common-mode voltage should satisfy following limitation:

$$\mathrm{AGND} + 0.1\mathrm{V} + \mathrm{GAIN\_P} * \mathrm{VDin(max)}/2 \ < \ \mathrm{VCMin} \ < \ \mathrm{VDD} - 0.1\mathrm{V} - \mathrm{GAIN\_P} * \mathrm{VDin(max)}/2$$

Besides, the input of the PGA amplifiers is PMOS transistor so the PGA input should meet:

$$\mathrm{VINP(N)} \ < \ \mathrm{VDD} - 1\mathrm{V}$$

For voltage-driven bridge sensors, the common-mode voltage of its output is usually close to VREF/2. One can easily meet the limitation by choosing a proper 'GAIN_P' and make VDin (max) <0.8*VREF/GAIN_P. '0.8' here is considered to give some margin for the sensor sensitivity and the amplifier voltage swing. For current-driven sensors, more careful settings are needed to maximize the dynamic range of the PADC.

6.1.3. Digital Filter

The NSA2302 has a digital decimation filter followed the modulator. The output data rate could be separately programmable for sensor signal channel and temperature channel from 256X to 32768X by setting bits 'OSR_P' and 'OSR_T'. Table 6.1 shows the effective number of bits (ENOB) of PADC output with different ODR_P settings. The relationship of ENOB with RMS noise is:

$$ENOB_{RMS} = 24 - log_2(RMS_{ADC})$$

RMSADC is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB (ENOB_RMS) and noise free ENOB (ENOB_NF) is shown as below:

$$ENOB_{NF} = ENOB_{rms} - 2.7$$

Table 6.1 ENOB_RMS of PADC under different ODR settings (VREF = 3.6V, 'SYS_CHOP_EN' = 0)

OSR	Gain														
	1	2	4	6	8	12	16	24	32	48	64	96	128	192	256
256X	15.56	15.69	15.80	15.72	15.77	15.84	15.83	15.82	15.85	15.82	15.88	15.54	15.52	15.12	14.81
512X	16.04	16.04	15.95	15.99	16.05	16.18	15.99	16.20	16.13	16.09	16.03	16.03	15.72	15.45	15.03
1024X	16.48	16.38	16.29	16.45	16.38	16.48	16.40	16.52	16.42	16.57	16.50	16.33	16.13	15.80	15.40
2048X	16.89	16.84	16.73	16.86	16.82	16.95	16.97	17.19	16.95	16.84	16.87	16.85	16.58	16.13	15.85
4096X	17.31	17.31	17.28	17.49	17.33	17.39	17.38	17.45	17.42	17.43	17.33	17.12	16.87	16.52	16.25
8192X	17.77	17.94	17.77	17.96	17.82	17.76	17.90	17.93	17.89	17.97	17.80	17.56	17.41	17.06	16.63
16384X	18.23	18.37	18.23	18.50	18.28	18.40	18.29	18.34	18.33	18.08	18.30	18.16	17.68	17.41	17.13
32768X	18.76	18.93	18.69	18.9	18.65	18.79	18.80	18.53	18.94	18.65	18.56	18.20	17.89	17.66	17.28

6.2. Analog Front-end Module 2: Temperature Measurement Channel

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. The NSA2302 supports both internal temperature sensor and external temperature sensor, selected by register bit 'TEMP_sel' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digital filtered. When the temperature difference between the sensor element and the NSA2302 chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as diode, RTD, NTC or the bridge resistor itself, etc. Through different 'RAW_T' setting, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

6.2.1. Internal Temperature Sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registers reg0xAA, reg0xAB and reg0xAC. When 'RAW_T' is set to 0, the NSA2302 can provide a temperature reading in degree Celsius, in the format of

$$T = Temp\_out\ /2^8$$

For example, 'Temp_out = 0x1FF2' corresponding to 31.94 °C. The relationship between the noise of the internal temperature sensor and 'OSR_T' setting is shown in Table 6.2.

Table 6.2 RMS Noise of Internal Temperature Sensor under different OSR_T

OSR (Hz)	1024	2048	4096	8192	256	512	16384	32768
RMS Noise in ℃	0.006125	0.005859	0.005434	0.005073	0.008403	0.006552	0.003876	0.005662

6.2.2. External Temperature Sensor

When external temperature sensor mode is selected, an internal 6 kΩ low drift resister is connected, which is shown in Figure 6.2. The temperature sensing signal input from the TEMP pin is buffered for TADC conversion. The reference voltage of the TADC is set

by 'T_ref_trim'. The gain of the TADC can be 1X, 2X, 4X, 6X, 8X, 16X, 24X, 32X, 48X, 64X, 96X, 128X, 192X, 256X. The relationship between TDATA_RAW and the temperature input is

$$TDATA_{RAW} = \frac{VTEMP * GAIN\_T}{VEXT} * 2^{23}$$

When RAW_T = 0, the built-in DSP calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. Please refer to application note NOVOSENSE provided.

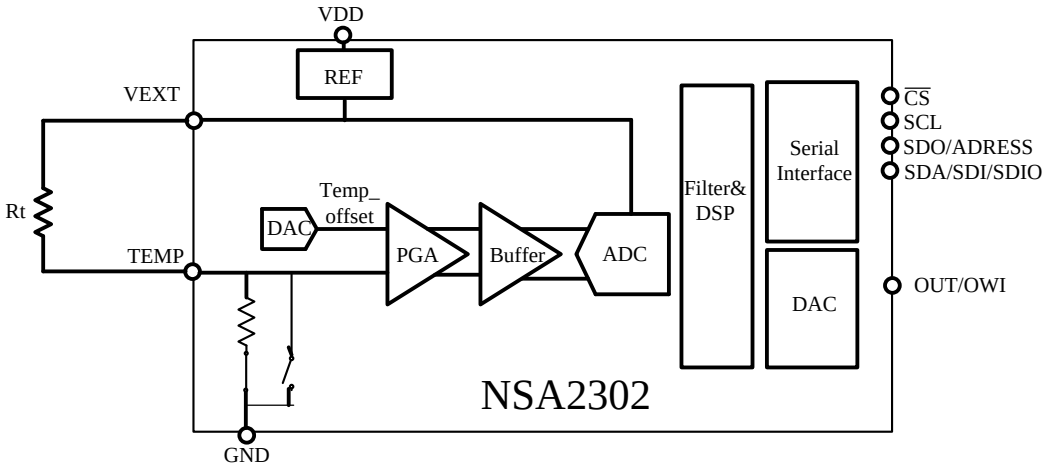


Figure 6.2 External Temperature Sensor Connection

6.3. Analog Output Module

Set 'DAC_on' =1 to get into the analog output mode (no matter what 'CMD' registers contents). During analog output mode, the NSA2302 alternately performs 64 times pressure conversions after once temperature conversion automatically. The higher 12 bits (without the sign bit) of the calibrated pressure data will be mapped to the VOUT pin with the equations below and all negative Data_out values will be mapped to the lower limit voltage. Calibration coefficients must be carefully set in this mode to make the full span of the pressure data occupies the full span of the output voltage.

$$OUT = \frac{Data\_out[22:11]}{4096} * VDD(Vout\_sel = 0)$$

$$OUT = \frac{Data\_out[22:11]}{4096} * 1.5 * VEXT(Vout\_sel = 1)$$

The DAC allows programming a lower and upper clipping limit for the output signal. The internal 12-bit calculated bridge value is compared against the 12-bit value formed by {11, DAC_limit_h [3:0],111111} for the upper limit and {00, DAC_limit_l [3:0], 000000} for the lower limit. If the calculated pressure is higher than the upper limit or lower than the bottom limit, the analog output will be clamped to upper or bottom limit, otherwise it is normal output.

6.3.1. Frequency Output

NSA2302 enables frequency output mode if 'Freq_out_en' = 1.

The full scale of output frequency is set by Freq_FS<1:0>, which is shown in Table 6.3.

Table 6.3 Freq_FS Setting

Freq_FS<1:0>	*Frequency Scale(kHz)*
2'b00	250
2'b01	125
2'b10	62.5
2'b11	31.25

The output frequency value is expressed as below.

$$\text{Frequency} = \frac{Data\_out\,[22:11]}{4096} * Freq\_FS$$

6.4. Power Supply and Sensor Driver Module

The NSA2302 internally includes a precision bandgap reference with very low temperature drift. This reference voltage is used in the constant voltage driving circuits for sensors, JFET regulator, clock generator and ADC/DAC etc.

6.4.1. Sensor Driver

The VEXT pin can provide a constant voltage to drive the bridge sensors, which is also the reference voltage for ADC. The constant voltage can be selected either 3.6V or 2.4V via the EERPOM register bit 'Regulator_sel'.

6.4.2. JFET Regulator

By tuning the gate of external JFET (for example, BSS169) through VGATE pin, the JFET regulator integrated in the NSA2302 can convert the external high voltage supply to 5V and supply it to the VDD pin (Figure 6.3). An external NPN bipolar (for example, BCX5610) with a 50kohm resistor has same function (Figure 6.4).

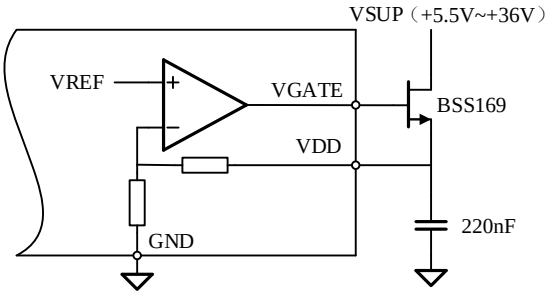


Figure 6.3 Regulation with external JFET

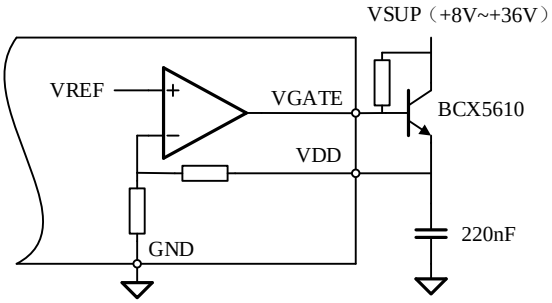


Figure 6.4 Regulation with external NPN Bipolar

6.5. Built-in DSP and Control Logics

6.5.1. Work Mode

6.5.1.1. Single-shot Sensor Signal Conversion

Setting 'measurement_control' = 3'b001 and 'sco' = 1 to initiate once single-shot sensor signal conversion, the chip powers up, performs once sensor signal conversion, and returns back to standby mode with automatically changing 'sco' to 0. INT goes high when data is ready and returns low after the data value (0x06-0x08) has been read out from the 'Data_out' registers. The 'Data_out' registers can be read several times if required, even when the INT pin is low, but care must be taken not to read data when the 'Data_out' registers are just in refreshing.

A following calibration DSP is optional during the single-shot sensor signal conversion. When the DSP is enabled ('raw_data_on' = 0), a 24-bit calibrated sensor data will be stored in the 'Data_out' registers after conversion ends, and else, the raw 24-bit ADC output is stored there.

6.5.1.2. Single-shot Temperature Conversion

Setting 'measurement_control' = 3'b000 and 'sco' = 1 to initiate once single-shot temperature conversion, the chip powers up, performs once temperature conversion, and returns back to standby mode with automatically changing 'sco' to 0. When setting 'raw_data_on' = 0, the calibrated temperature data is stored in 'Temp_out' registers and else, the raw ADC data of the temperature

channel conversion would be stored in the 'Data_out' registers. INT pin also goes high when the conversion ends and will return low after a reading of the 'Temp_out' or 'Data_out' registers.

6.5.1.3. Combined Conversion

Setting 'measurement_control' = 3'b010 and 'sco' = 1 to initiate once combined conversion, the chip powers up, successively performs once temperature conversion and once sensor signal conversion, then returns back to standby mode with automatically changing 'sco' to 0. The 'raw_data_on' bit should be set 0 during combined conversion and the calibrated temperature data and sensor signal data are separately stored in 'Temp_out' and 'Data_out' registers. INT pin will go high when the sensor signal conversion ends and will return low after a reading of the 'Data_out' registers.

6.5.1.4. Sleep Conversion

Setting 'measurement_control' = 3'b011 and 'sco' = 1 to get into sleep conversion mode, the chip powers up and periodically performs once temperature conversion, once sensor signal conversion and a period of sleep phase. The duration of the sleep phase is configured by the 'sleep_time' bits from 0ms to 1s. The chip will not get back to standby mode until manually setting 'sco' bit to '0'. The 'raw_data_on' bit will be forced to 0 during sleep conversion and the calibrated temperature data and sensor signal are separately stored in 'Temp_out' and 'Data_out' registers. INT pin will go high when the sensor signal conversion ends and will automatically return low before next temperature conversion starting or after a reading of the 'Data_out' registers.

6.5.1.5. EEPROM

The NSA2302 contains 32 EEPROM bytes, which are used for customer to program the default configurations and the sensor calibration coefficients.

6.5.1.6. Loading

The contents of the EEPROM will be loaded into the EEPROM registers automatically after power up or soft-reset.

6.5.1.7. Programming

Writing EEPROM registers will not program the EEPROM directly. The contents of the EEPROM registers will be programmed into the EEPROM in auto mode by following sequence:

1, Set the register byte 'EE_pwr_on' (0x6A [7:5]) with 3'b010, to power on EEPROM;

2, Writing the register byte 'Blow_start' (Reg0x6C) with 0x6A, to start EEROM programming.

3, Customer can also program a specific register in manual mode by following sequence:

4, Set the register 'EE_pwr_on' (0x6A [7:5]) with 3'b010, to power on EEPROM;

5, Write the register 'EE_prog_address' (0x6A [4:0]) with targeted EEPROM register address offset (Base address is 0xA0);

6, Write the register byte 'Programmed data' (0x6B) with targeted EEPROM register value;

7, Writing the register byte 'Blow_start' (Reg0x6C) with 0x68, to start EEROM programming.

6.6. Diagnosis

A suite of diagnosis is provided on NSA2302 through 4 fault monitor comparators, refer to Figure 6.5.

When diagnosis are enabled by set 'Diag_on' to 1, two branches of 100nA current sources are added on the input pair from sensor. This will add some voltage shift to the input signal but mostly common mode drift and any error introduced could be minimized during sensor calibration. Four comparators are used to monitor if the voltage is in 100mV range of VEXT or ground. User could use this information to find out sensor faults like loss of bridge positive, loss of bridge negative, open sensor connection and sensor input short.

The outputs of all the comparators are locked into the 'Error_code<5:0>' register at the end of every data conversion. When either of the fault comparator outputs is asserted, indicating a fault, NSA2302 analog output VOUT will be forced to a fault indicating voltage level of 2.5% of VDD. Together with the lower or upper clip limit function, system diagnostic can be performed to determine if the sensor is detective or the process being monitored by the sensor is out of range.

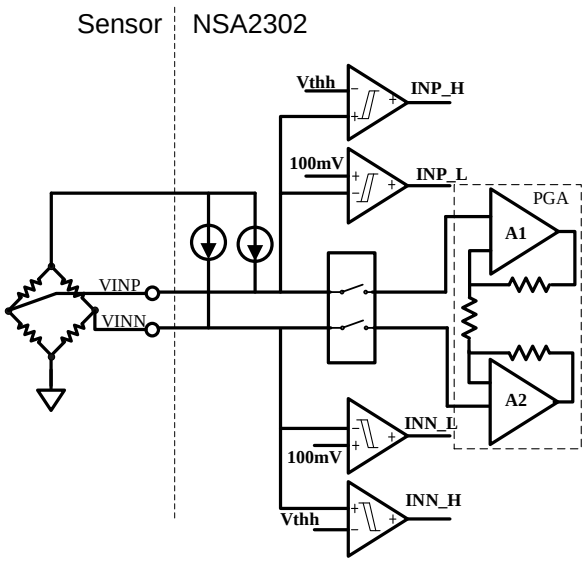


Figure 6.5 NSA2302 Fault Monitoring System

7. Serial Interface

Three different serial interfaces (OWI, SPI and I²C) are supported in the NSA2302 to configure registers, program EEPROM and pulling measured data. The time between 10ms and 80ms after powering up is defined as the OWI entering window. If a special 24 bits OWI entering pattern is detected via OWI pin in this window, the chip enters OWI communication mode, otherwise enters I²C or SPI communication mode. Then, CSB pin is used to further select between I²C and SPI methods, high voltage level or floating indicates the I²C method, low voltage level indicates the SPI method.

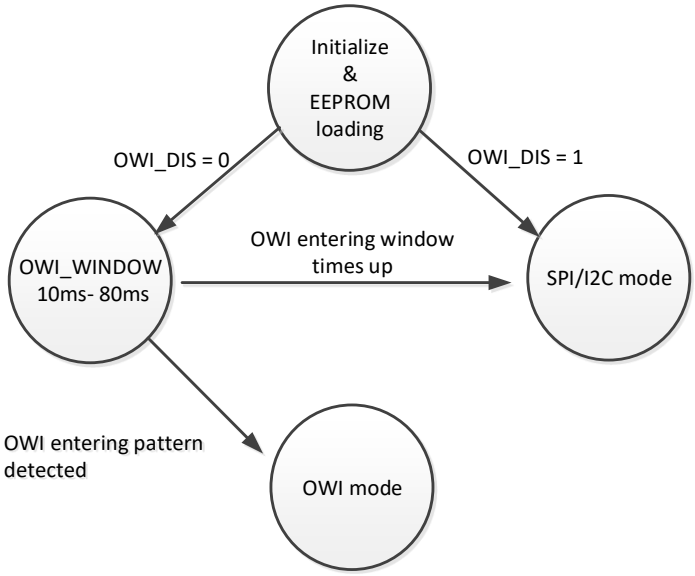


Figure 7.1 Definition of serial communication mode

7.1. OWI Interface

The NOVOSENSE self-owed One Wire Interface (OWI) protocol integrated in the NSA2302 can support serial communication under all 0-5V, frequency output modes with no extra communication wires added. This protocol identifies the data bit transferred by the duty cycle of one rising-to-rising period. Duty cycle more than 5/8 means a logical 1, and less than 3/8 means a logical 0.

7.1.1. Timing Spec

Table 7.1 OWI Timing Spec

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{period}	OWI bit period		20		4000	μs
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	μs
t_{stop}	Stop condition time		2			t_{period}

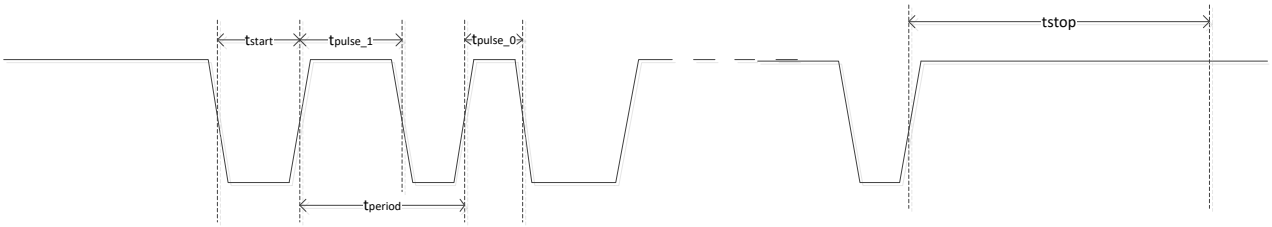


Figure 7.2 OWI Timing

7.1.2. Enter OWI Mode

If 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is OWI entering window. If a special 24 bits OWI entering pattern (0xB5A6, 1b, Chip_address [0xA3(6:0)]) is detected via OWI pin in this window, the chip enters OWI communication mode. Under this setting, the OUT pin is disabled during the OWI window and OWI mode; the OWI pin and the OUT pin can be shorted together to support 3-wire sensor products.

The Chip_address can be programmed to different values for multiple devices sharing the same OWI bus. In this case, the OWI master can communicate with specific NSA2302 chip through the unique address. There is a universal address (0xB5A6FF), which can be used to communicate with any NSA2302 chip. Figure 6.3 shows an example of OWI entering pattern with universal address.

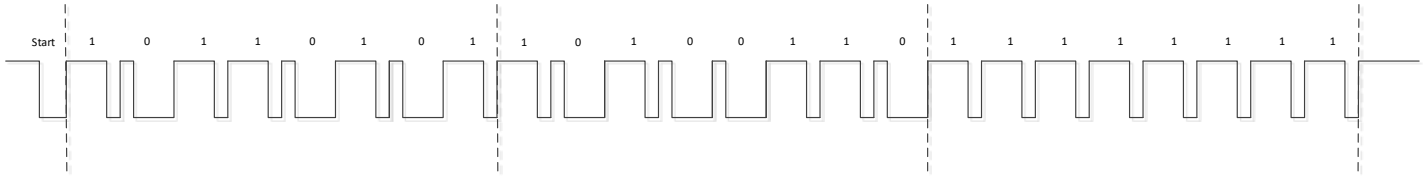


Figure 7.3 OWI Entering Pattern

In OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed during the entire communication, so the bit period during OWI communication should keep the same as the OWI entering pattern.

7.1.3. OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state a low pulse (return to high) with a pulse width between20μs to 4ms indicates a start condition. Every command has to be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c) Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line constant high or low voltage level for at least two times of the bit period (t_{period}).

d) Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number (NO. bits) and a read/write–bit (0–write, 1–read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1 byte, 01: 2 bytes, 10: 3 bytes, 11: 4 bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

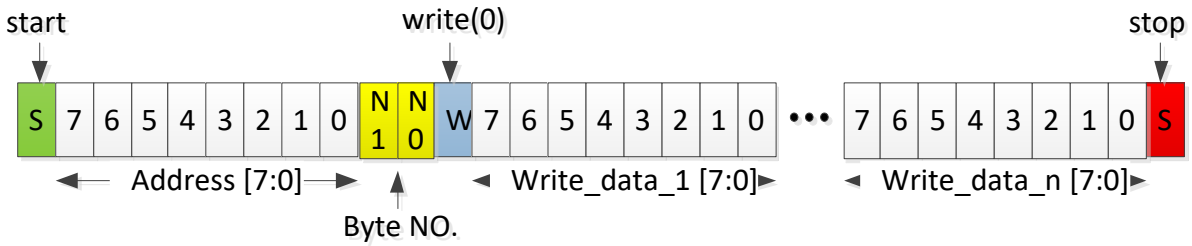


Figure 7.4 OWI Write Operation

f) Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is contented in the addressed register and follows. Each data bytes include 8 bits of data and 2 bits of parity check code C1 and C0.

C1 = Read_data[7] ^ Read_data[5] ^ Read_data[3] ^ Read_data[1];

C0 = Read_data[6] ^ Read_data[4] ^ Read_data[2] ^ Read_data[0];

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.

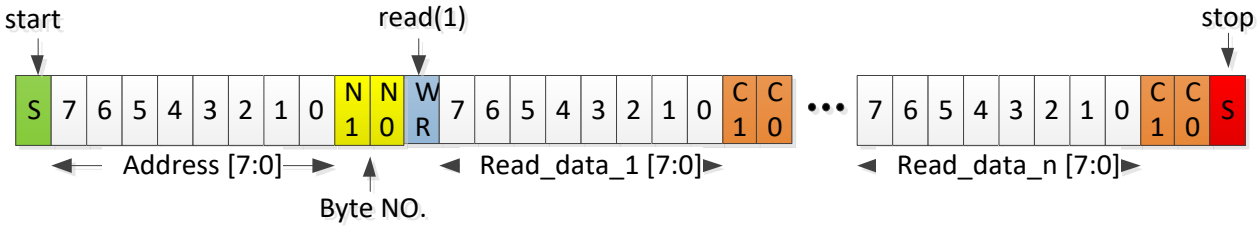


Figure 7.5 OWI Read Operation

7.1.4. Quit OWI Communication

Writing 'Quit_OWI' register (Reg0x61) with 0x5d during OWI mode can temporarily or permanently quit the OWI communication and enter voltage output mode.

Writing 'Quit_OWI' register (Reg0x61) with 0x89 during OWI mode can temporarily or permanently quit the OWI communication and enter output high-Z mode.

The register byte 'OWI_QUIT_CNT' is used to set the quit time with the LSB = 65.5ms (0x00 means permanently quit), and the chip will be back into OWI mode again after the quit time's up.

7.2. SPI Interface

7.2.1. Interface Specification

Table 7.2 SPI interface specifications

Symbol	Parameter	Condition	Min	Max	Unit
f_{sclk}	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{sclk_l}	SLCK low pulse		20		ns
t_{sclk_h}	SLCK high pulse		20		ns
T_{sdi_setup}	SDI setup time		20		ns
T_{sdi_hold}	SDI hold time		20		ns
T_{sdo_od}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
T_{csb_setup}	CSB setup time		20		ns
T_{csb_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in Table 7.2.

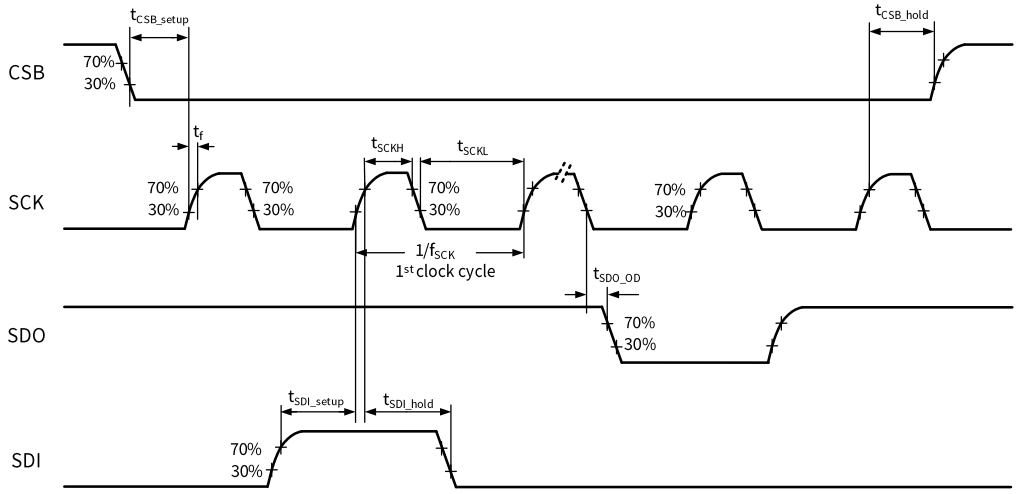


Figure 7.6 SPI Timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 7.7, the instruction phase is divided into a number of bit fields.

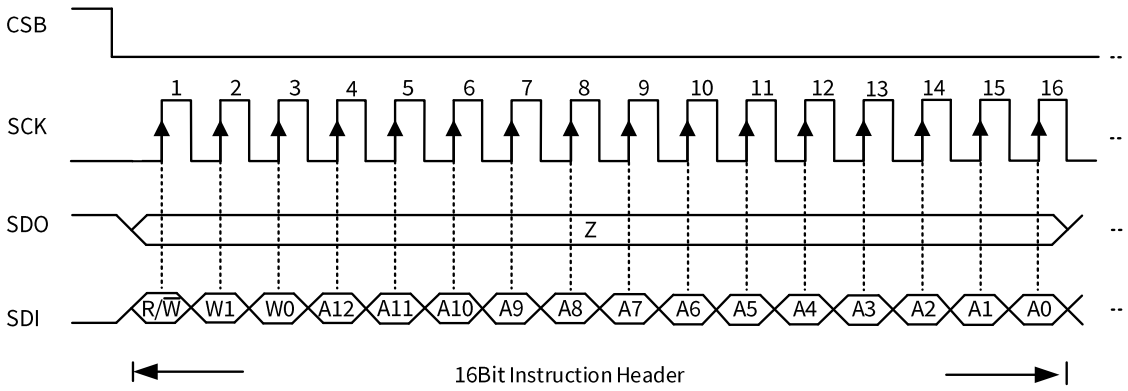


Figure 7.7 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read operation is being requested; otherwise a write operation is requested.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 7.3). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions to high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table 7.3 W1 and W0 settings

W1:W0	*Action*	*CSB Stalling*
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for the entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). There can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed (Figure 7.8).

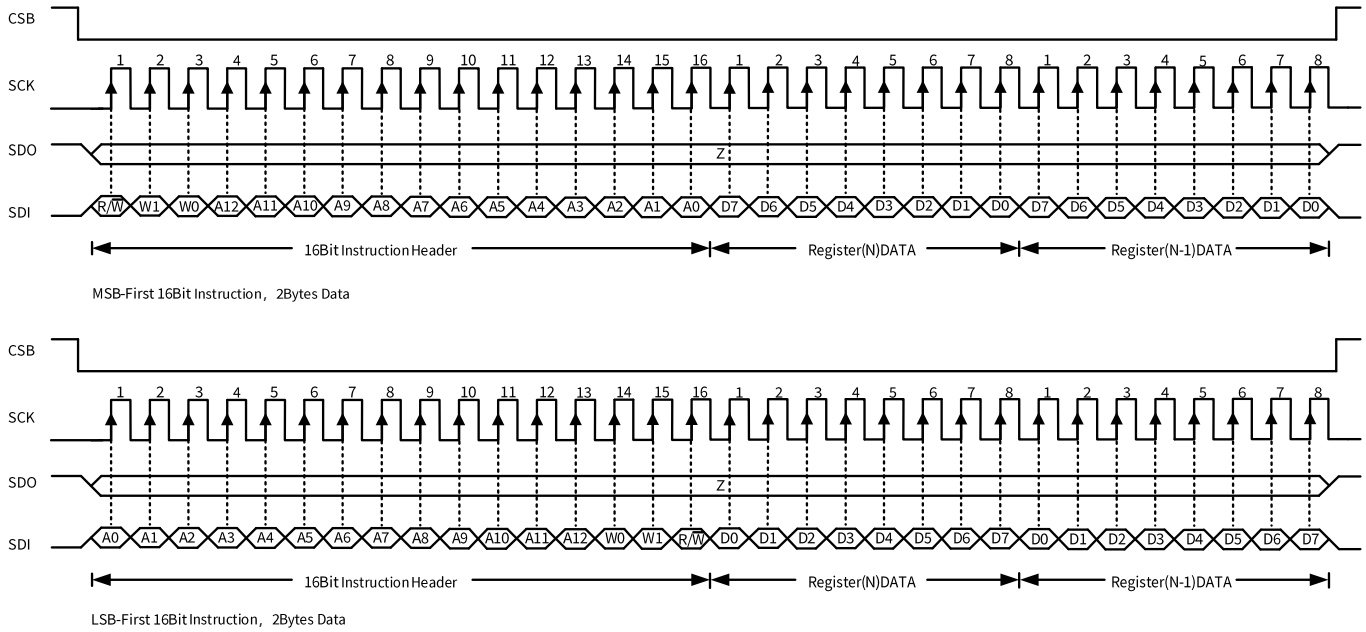


Figure 7.8 MSB First and LSB First Instruction and Data Phases

Register bit 'SDO_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is low, making SDO inactive.

7.3. I²C Interface

I²C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I²C device address of NSA2302 is shown below. The LSB bit of the 7-bit device address is configured via SDO/ADDR pin.

Table 7.4 I²C Address.

A7	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*	*W/R*
1	1	1	1	1	1	1	0/1

Table 7.5lectrical specification of the I²C interface pins

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*
f_{scl}	Clock frequency			400	kHz
t_{LOW}	SCL low pulse		1.3		μs
t_{HIGH}	SCL high pulse		0.6		μs
t_{SUDAT}	SDA setup time		0.1		μs
t_{HDDAT}	SDA hold time		0.0		μs
t_{SUSTA}	Setup Time for a repeated start condition		0.6		μs
t_{HDSTA}	Hold time for a start condition		0.6		μs
t_{SUSTO}	Setup Time for a stop condition		0.6		μs
t_{BUF}	Time before a new transmission can start		1.3		μs

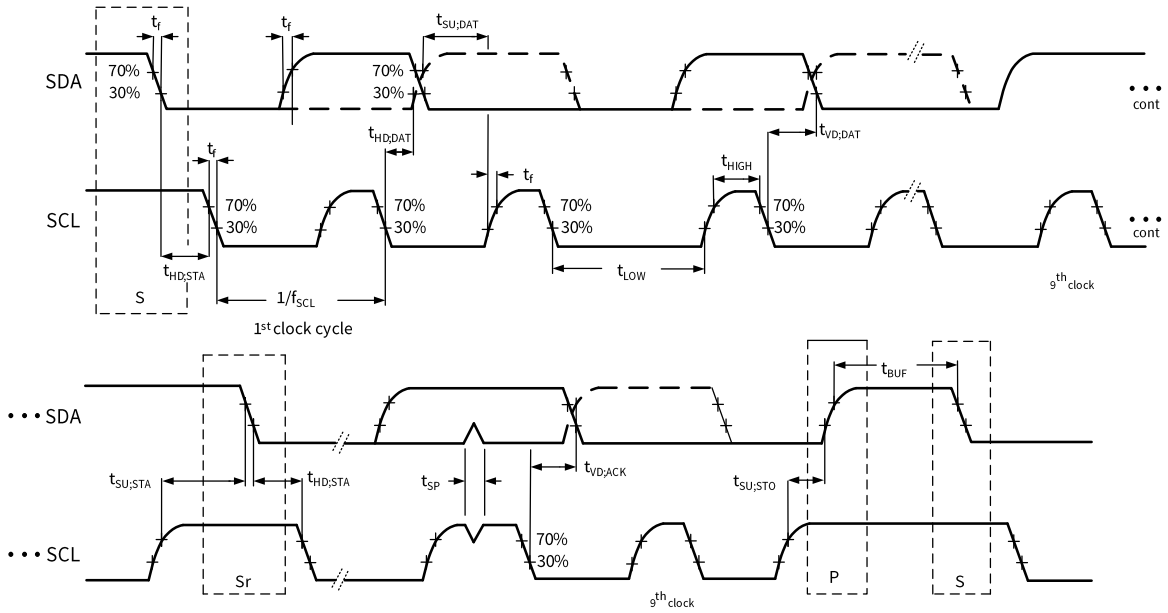


Figure 7.9 I²C Timing Diagram

The I²C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change values at SDA only when SCL is low.

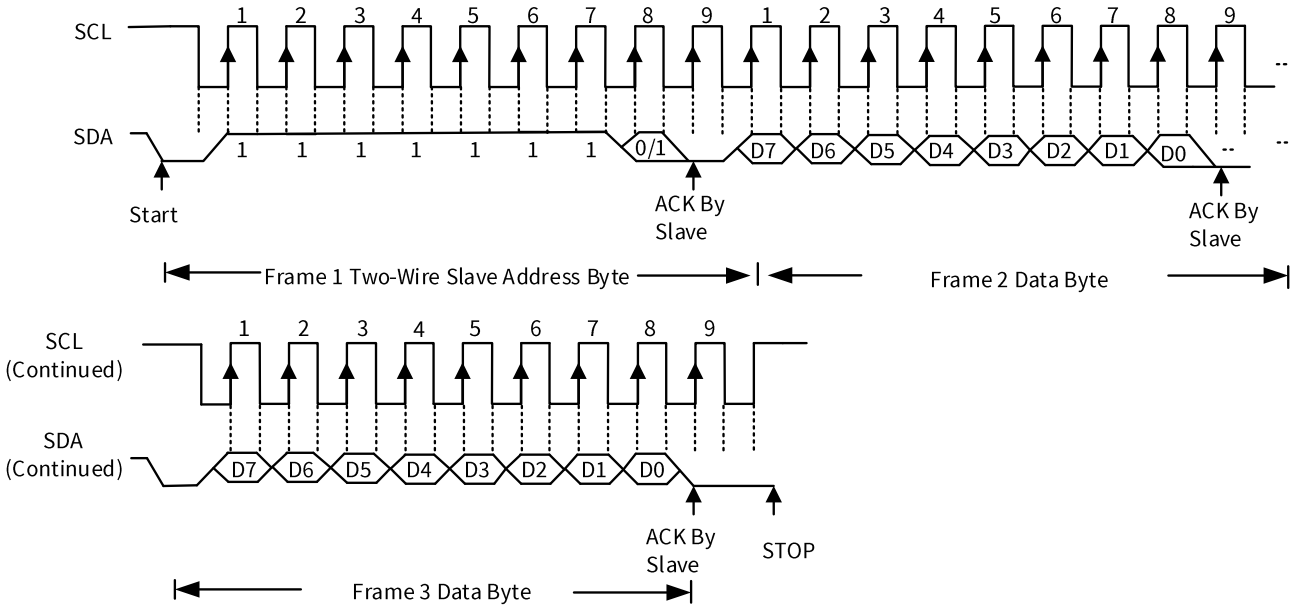


Figure 7.10 I²C Protocol

NSA2302 can support single-byte read/write and multi-byte read/write operations. The transfer format is shown in Figure 7.11 and Figure 7.12.

Byte Write

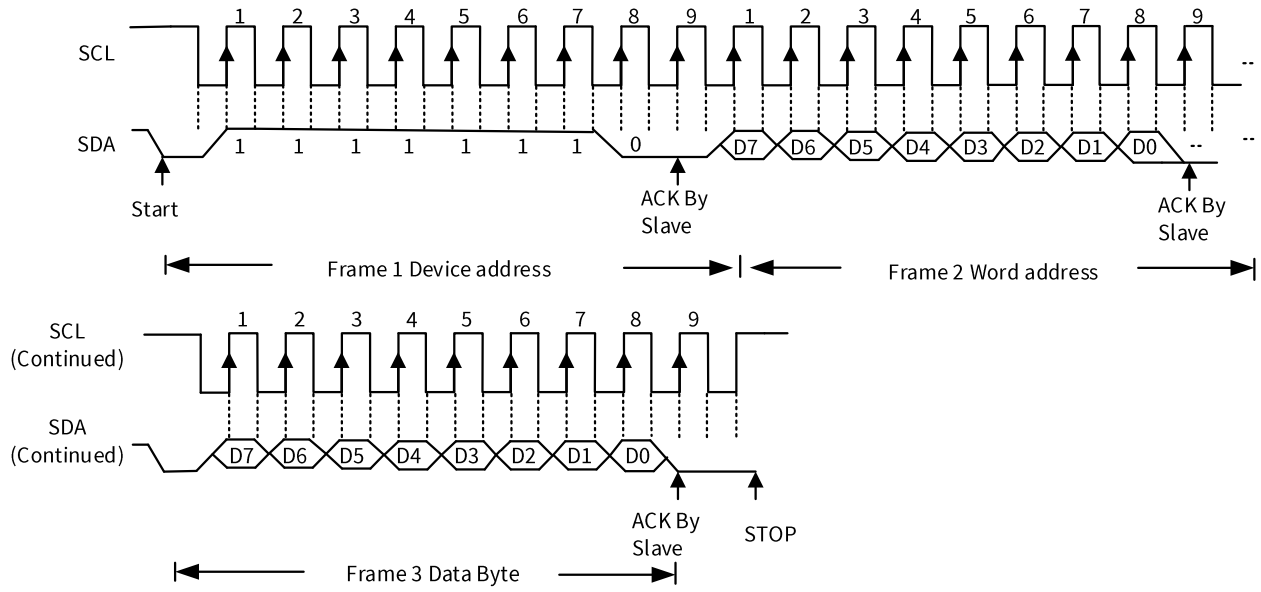


Figure 7.11 I²C Write Byte

Random Read

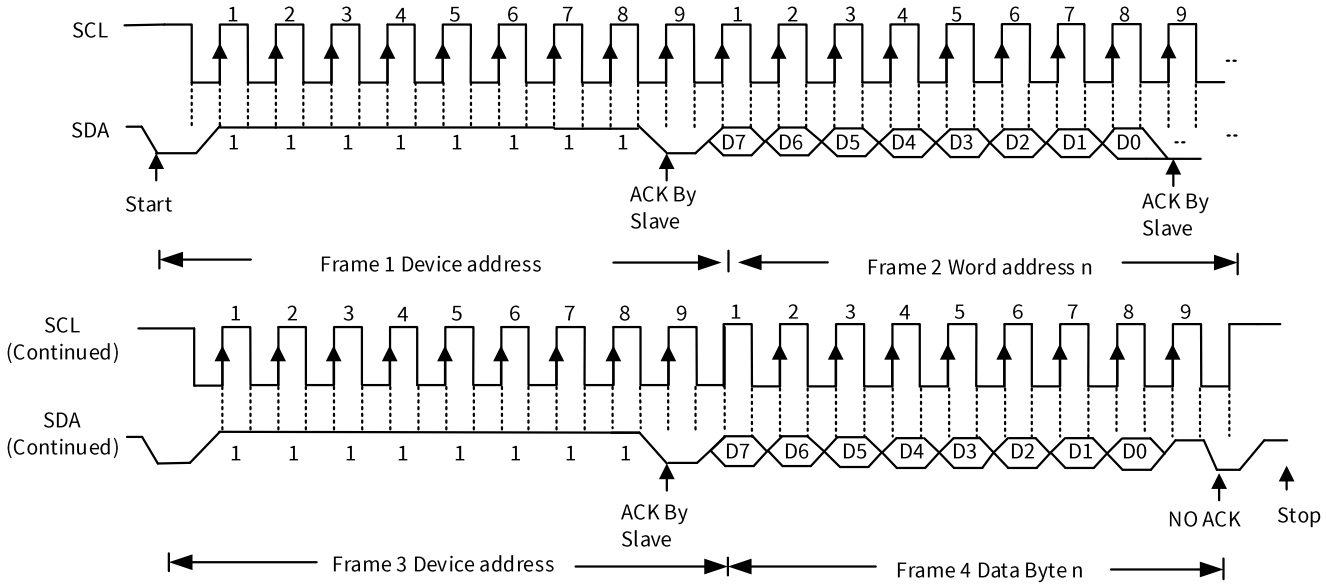


Figure 7.12 I²C Read Byte

8. Package Information

The NSA2302 is offered either via bare die or MSOP-10 Package.

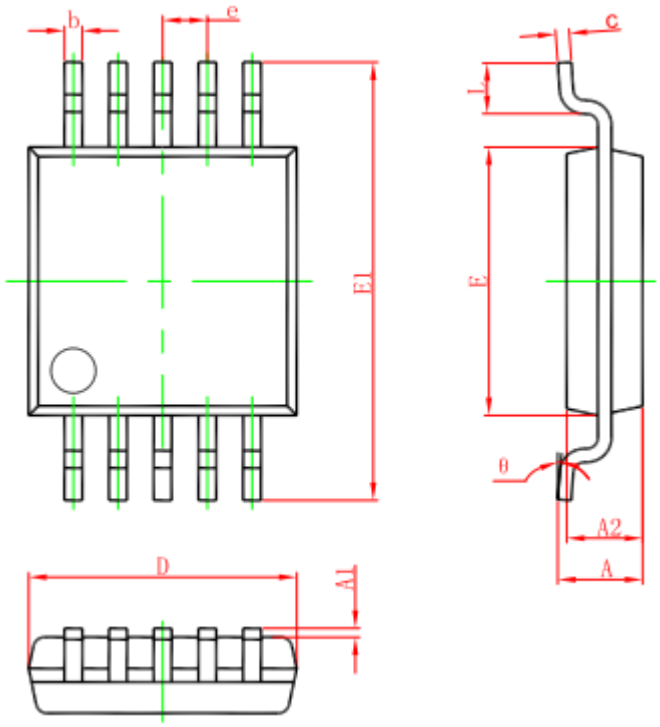


Figure8.1 MSOP-10 package Outline

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Figure8.2 MSOP-10 package Outline Dimensions

9. Typical Application

9.1. 0~5V Voltage Output

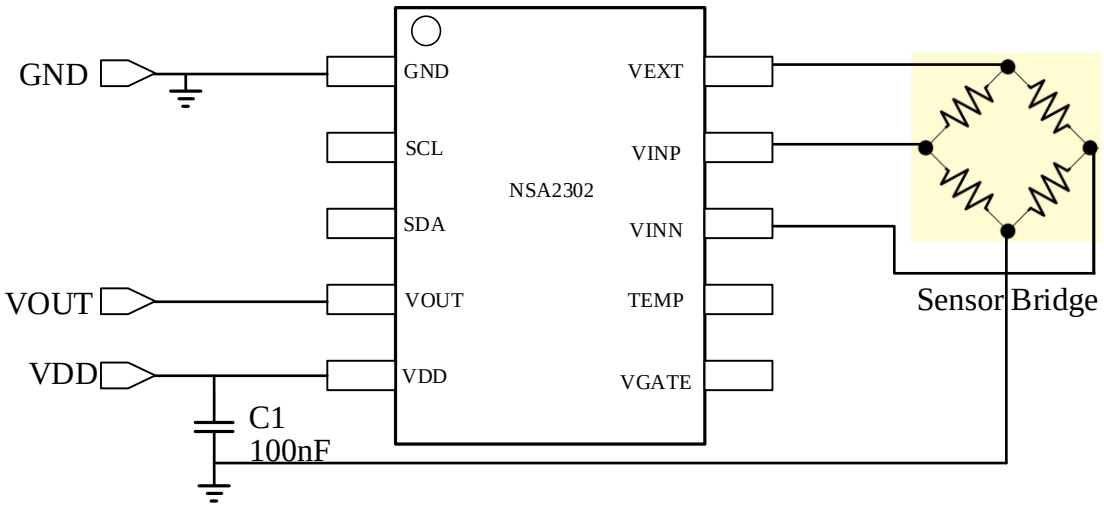


Figure 9.1 Typical Application (0~5V Voltage Output)

9.2. Voltage Output with High Voltage JFET Supply

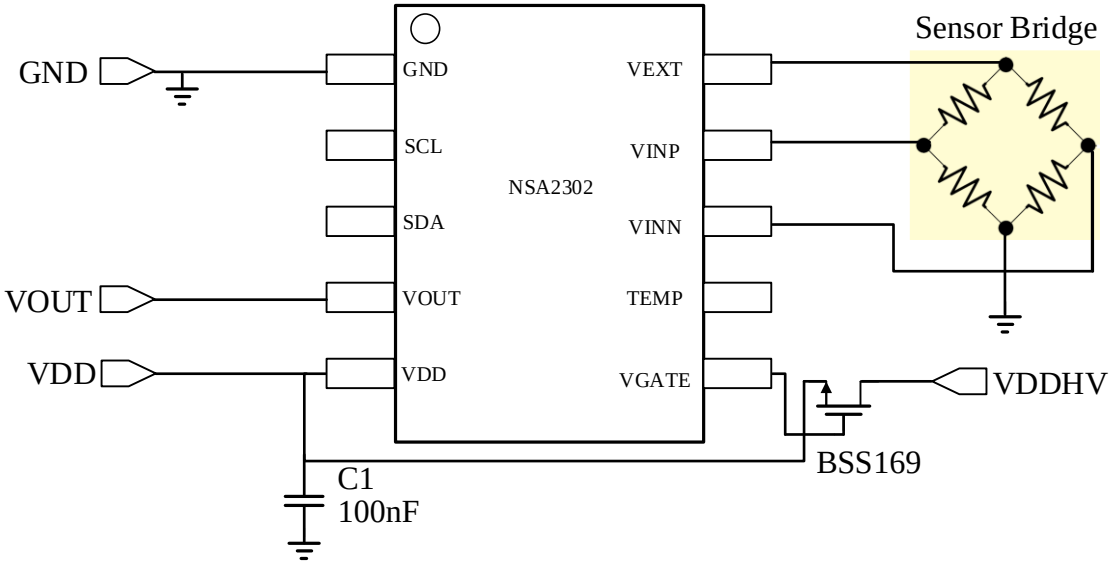


Figure 9.2 Typical Application (Voltage Output with High Voltage JFET Supply)

9.3. I²C Output

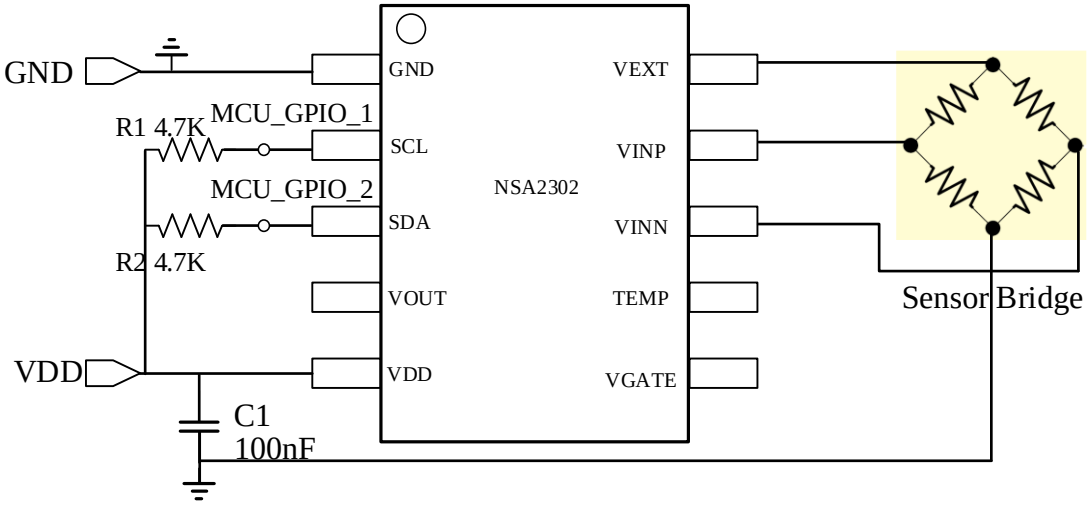


Figure 9.3 Typical Application (I²C Output)

10. Order Information

Part Number	*Temperature*	*MSL*	*Package Type*	*SPQ*
NSA2302_QBW	-40 to 125℃	-	Bare Die	KGD
NSA2302-QMOR	-40 to 125℃	3	MSOP10	3000

11. Revision History

Revision	*Description*	*Date*
1.0	Initial version	2020-10-29
1.1	Amend order information	2023-4-10
1.2	Change to new datasheet template Add wafer information	2023-10-07

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