# NSB12ANT3G

# 600 Watt Peak Power Zener Transient Voltage Suppressor

## Unidirectional

The NSB12ANT3G is designed to protect voltage sensitive components from high voltage, high energy transients. This device has excellent clamping capability, high surge capability, low zener impedance and fast response time. The NSB12ANT3G is ideally suited for use in computer hard disk drives, communication systems, automotive, numerical controls, process controls, medical equipment, business machines, power supplies, and many other industrial/ consumer applications.

### Specification Features:

- Working Peak Reverse Voltage Range − 12 V
- Peak Power − 600 Watts @ 1 ms at Maximum Clamp Voltage @ Peak Pulse Current
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- ESD Rating IEC 61000−4−2 Level 4 (> 30 kV)
- Low Leakage < 5 μA at 12 V
- UL 497B for Isolated Loop Circuit Protection
- Response Time is Typically < 1 ns
- Pb−Free Package is Available

### Mechanical Characteristics:

**CASE:** Void-free, transfer-molded, thermosetting plastic

**FINISH:** All external surfaces are corrosion resistant and leads are readily Solderable

**MAXIMUM CASE TEMPERATURE FOR SOLDERING PURPOSES:** 260°C for 10 Seconds

**LEADS:** Modified L−Bend providing more contact area to bond pads

**POLARITY:** Cathode indicated by polarity band

**MOUNTING POSITION:** Any

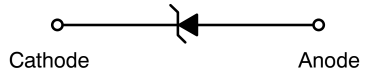
### MAXIMUM RATINGS

Please See the Table on the Following Page

**ON Semiconductor**®

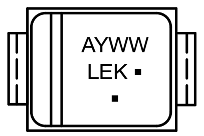
**http://onsemi.com**

### PLASTIC SURFACE MOUNT ZENER OVERVOLTAGE TRANSIENT SUPPRESSOR 600 WATT PEAK POWER



**SMB**
**CASE 403A**
**PLASTIC**

### MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
LEK = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NSB12ANT3G | SMB<br>(Pb−Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

December, 2007 − Rev. 0

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Power Dissipation (Note 1) @ $T_L$ = 25°C, Pulse Width = 1 ms | $P_{PK}$ | 600 | W |
| DC Power Dissipation @ $T_L$ = 75°C<br>Measured Zero Lead Length (Note 2)<br>Derate Above 75°C<br>Thermal Resistance from Junction to Lead | $P_D$<br><br><br>$R_{\theta JL}$ | 3.0<br><br>40<br>25 | W<br><br>mW/°C<br>°C/W |
| DC Power Dissipation (Note 3) @ $T_A$ = 25°C<br>Derate Above 25°C<br>Thermal Resistance from Junction to Ambient | $P_D$<br><br>$R_{\theta JA}$ | 0.55<br>4.4<br>226 | W<br>mW/°C<br>°C/W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −65 to +150 | °C |

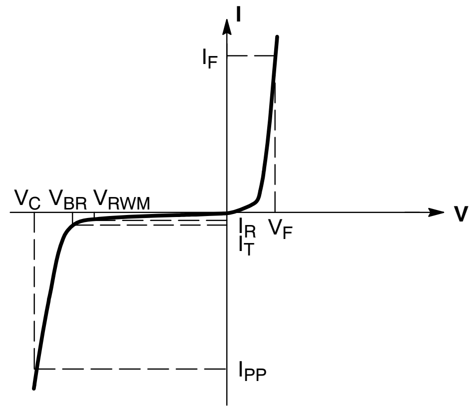
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 X 1000 μs, non−repetitive at maximum $I_{PPM}$ and $V_{CM}$, see electrical characteristics.
2. 1″ square copper pad, FR−4 board
3. FR−4 board, using ON Semiconductor minimum recommended footprint, as shown in 403A case outline dimensions spec.

## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Reverse Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Working Peak Reverse Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $I_F$ | Forward Current |
| $V_F$ | Forward Voltage @ $I_F$ |



Uni−Directional TVS

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Zener Voltage (Note 5) | IT = 1 mA | $V_{BR}$ | 13.2 | 13.75 | 14.3 | V |
| Reverse Leakage Current | $V_{RWM}$ = 12 V | $I_R$ | | | 5.0 | μA |
| Clamping Voltage | $I_{PPM}$ = 30.2 A<br>(Per Figure 1, Note 6) | $V_{CM}$ | | | 19.9 | V |
| Forward Peak Voltage | $I_F$ = 30 A<br>(Note 4) | $V_F$ | | | 3.5 | V |

4. 1/2 sine wave (or equivalent square wave), PW = 8.3 ms, non−repetitive duty cycle.
5. VZ measured at pulse test IT at an ambient temperature of 25°C.
6. Absolute Maximum Peak Current, $I_{PPM}$.

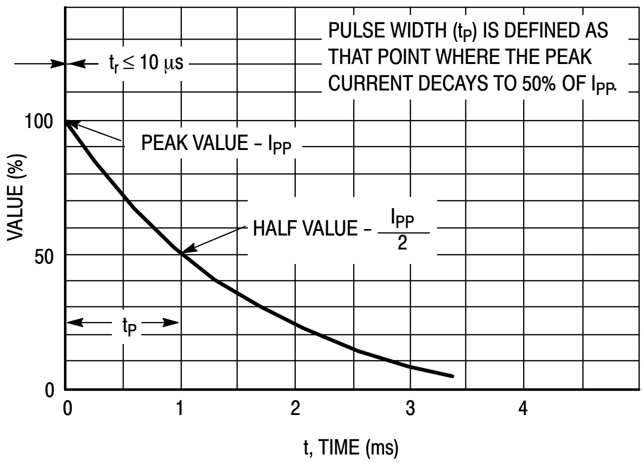


Figure 1. 10 × 1000 μs Pulse Waveform

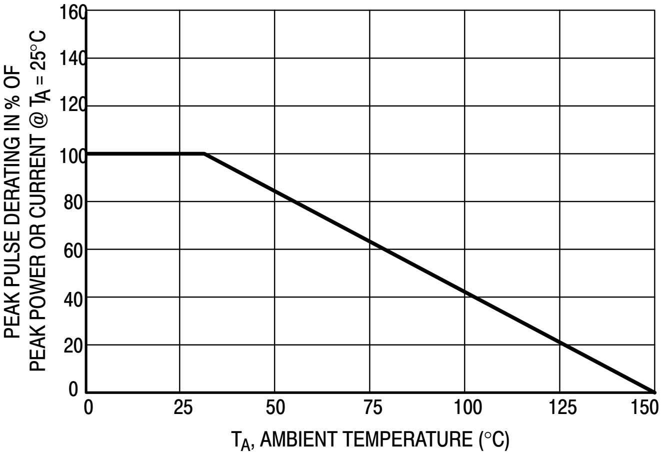
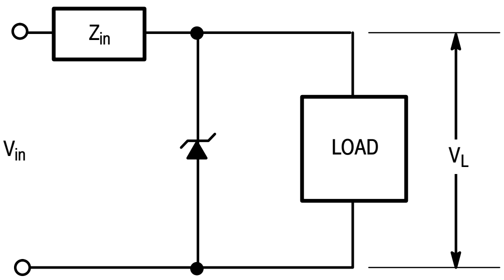


Figure 2. Pulse Derating Curve

## TYPICAL PROTECTION CIRCUIT



## APPLICATION NOTES

### RESPONSE TIME

In most applications, the transient suppressor device is placed in parallel with the equipment or component to be protected. In this situation, there is a time delay associated with the capacitance of the device and an overshoot condition associated with the inductance of the device and the inductance of the connection method. The capacitive effect is of minor importance in the parallel protection scheme because it only produces a time delay in the transition from the operating voltage to the clamp voltage as shown in Figure 3.

The inductive effects in the device are due to actual turn-on time (time required for the device to go from zero current to full current) and lead inductance. This inductive effect produces an overshoot in the voltage across the equipment or component being protected as shown in Figure 4. Minimizing this overshoot is very important in the application, since the main purpose for adding a transient suppressor is to clamp voltage spikes. The SMB series have a very good response time, typically < 1 ns and negligible inductance. However, external inductive effects could produce unacceptable overshoot. Proper circuit layout, minimum lead lengths and placing the suppressor device as close as possible to the equipment or components to be protected will minimize this overshoot.

Some input impedance represented by $Z_{in}$ is essential to prevent overstress of the protection device. This impedance should be as high as possible, without restricting the circuit operation.

### DUTY CYCLE DERATING

If the duty cycle increases, the peak power must be reduced as indicated by the curves of Figure 5. Average power must be derated as the lead or ambient temperature rises above 25°C. The average power derating curve normally given on data sheets may be normalized and used for this purpose.

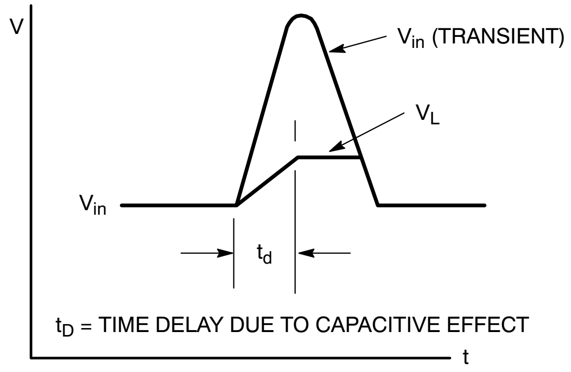


Figure 3.

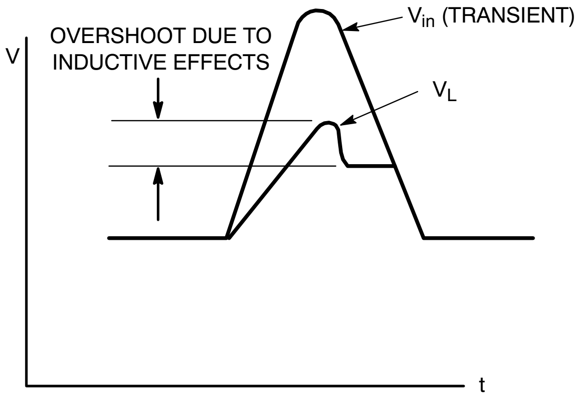


Figure 4.

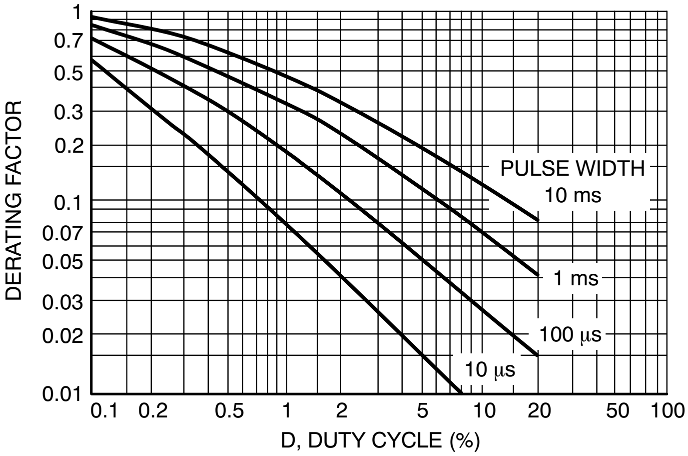


Figure 5. Typical Derating Factor for Duty Cycle

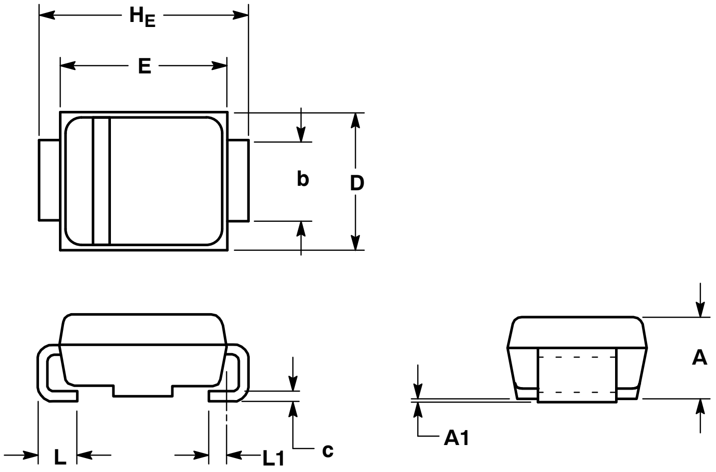
## UL RECOGNITION

The entire series has *Underwriters Laboratory Recognition* for the classification of protectors (QVGV2) under the UL standard for safety 497B and File #116110. Many competitors only have one or two devices recognized or have recognition in a non-protective category. Some competitors have no recognition at all. With the UL497B recognition, our parts successfully passed several tests including Strike Voltage Breakdown test, Endurance Conditioning, Temperature test, Dielectric Voltage-Withstand test, Discharge test and several more.

Whereas, some competitors have only passed a flammability test for the package material, we have been recognized for much more to be included in their Protector category.

## PACKAGE DIMENSIONS

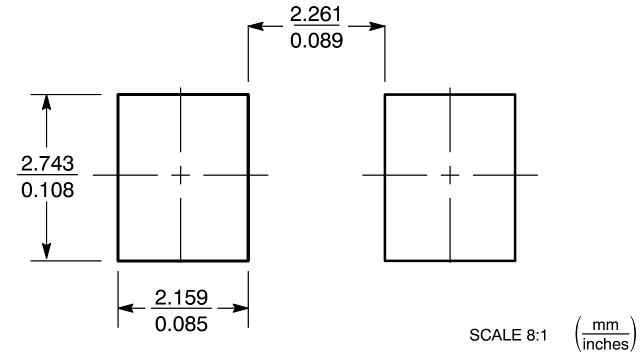
### SMB
CASE 403A-03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| **DIM** | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** |
| **A** | 1.90 | 2.13 | 2.45 | 0.075 | 0.084 | 0.096 |
| **A1** | 0.05 | 0.10 | 0.20 | 0.002 | 0.004 | 0.008 |
| **b** | 1.96 | 2.03 | 2.20 | 0.077 | 0.080 | 0.087 |
| **c** | 0.15 | 0.23 | 0.31 | 0.006 | 0.009 | 0.012 |
| **D** | 3.30 | 3.56 | 3.95 | 0.130 | 0.140 | 0.156 |
| **E** | 4.06 | 4.32 | 4.60 | 0.160 | 0.170 | 0.181 |
| **$H_E$** | 5.21 | 5.44 | 5.60 | 0.205 | 0.214 | 0.220 |
| **L** | 0.76 | 1.02 | 1.60 | 0.030 | 0.040 | 0.063 |
| **L1** | 0.51 REF | | | 0.020 REF | | |

### SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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