Product Overview

The NSC9262 is a highly integrated and AEC-Q100 qualified IC for capacitive sensor conditioning. The NSC9262 integrates a C/V converter, a 24-bit ADC for primary signal measurement channel, a 24-bit ADC for temperature measurement channel and sensor calibration logic. With the calibration algorithm built in the internal MCU, the NSC9262 supports to compensate sensor offset, sensitivity, temperature drift up to 2nd order, and non-linearity up to the 3rd order. The calibration coefficients are stored in a 64-Byte EEPROM that can be programmed multiple times. The NSC9262 also supports Over-voltage and Reverse-voltage protection. It can provide LIN output with sensor diagnostic function.

Key Features

- Over-voltage and Reverse-voltage protection between -40V~40V
- Directly high voltage supply up to 18V through VDDHV pin
- C/V converter with at most $\pm$ 16pF differential capacitor input
- 1X~8X ADC digital gain
- 24-bit ADC for primary signal measurement
- 24-bit ADC for temperature measurement
- Sensor connection fault detection supported
- Internal and external temperature sensor supported
- Sensor calibration algorithm embedded in a built-in MCU
- 64-Bytes EEPROM
- Special OWI interface
- RoHS & REACH compliance

- LIN interface communication up to 20kbit/s
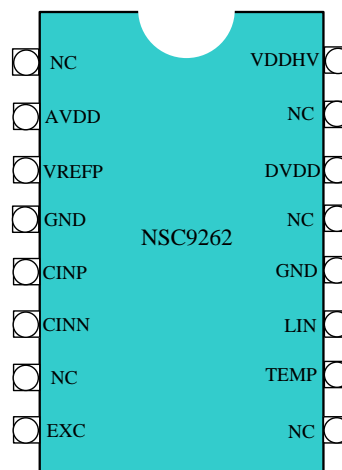- Compliant with LIN Specifications 1.3, 2.0, 2.1 and 2.2
- Package: SSOP16
- Qualified according to AEC-Q100 Grade0
- Operation temperature: -40℃~150℃

Applications

- Capacitive Pressure sensors
- Automotive braking system
- Automotive air-conditioner

Device Information

Part Number	Package	Body Size
NSC9262_Q0SSR	SSOP16	5mm × 6mm

Functional Block Diagrams

Figure 1. NSC9262 Block Diagram

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1. Pin Configuration and Functions

Figure 1.1 NSC9262 Block Diagram

Table 1.1 NSC9262 Pin Configuration and Description

PIN No.	Symbol	Function
1	NC	Floating
2	AVDD	Internal analog power supply
3	VREFP	Internal Reference voltage VREF output
4	GND	Ground
5	CINP	Capacitance measurement channel positive input
6	CINN	Capacitance measurement channel negative input
7	NC	Floating
8	EXC	Output excitation source
9	NC	Floating
10	TEMP	External temperature sensor input
11	LIN	LIN interface
12	GND	Ground
13	NC	Floating
14	DVDD	1.8V digital supply from internal LDO
15	NC	Floating
16	VDDHV	Power supply with OVP/RVP

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	VDDHV$_{max}$	-40		40	V	
Withstand voltage to ground (LIN)	V$_{LIN}$	-40		40	V	
AVDD Output	AVDD$_{max}$	-0.3		6.5	V	
Analog Pin Voltage		-0.3		AVDD+0.3	V	
Analog Output Current Limit				25	mA	
Digital Pin Voltage		-0.3		AVDD+0.3	V	25℃
Maximum Junction Temperature	T$_{jmax}$			155	℃	
Storage Temperature		-60		150	℃	
Operation Temperature	T$_{A\_EXT}$	-40		150	℃	

3. ESD Rating

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 Rev E ● All other pins to AVDD/VDDHV ● All other pins to GND ● IO pins to IO pins	±1.5	kV
	Charged device model(CDM), per AEC-Q100-011 Rev D ● All pins	±500	V

4. Electrical Characteristics

4.1. Electrical Characteristics

Typical conditions: VDDHV = 5V; Temperature = 25℃;

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage Range	VDDHV	7	12	18	V	
AVDD Output	AVDD		5		V	
DVDD LDO Output	DVDD	1.75	1.8	1.85	V	
Power on Reset	V$_{POR\_AVDD}$		2.5		V	POR threshold during power-up
	V$_{POR\_HYS}$		0.1		V	POR threshold hysteresis

Operation Current	I$_{avdd}$		1.9		mA	
Reference Voltage and Current Source						
VREF Output	VREF		2		V	
VREF Current Limit	I$_{VREF\_limit}$		20		mA	Short to Ground
Capacitance Measurement Channel						
Differential Input Capacitance Range	C$_{RANGE}$		±16		pF	CV_RANGE<1:0> = 2'b00
			±12		pF	CV_RANGE<1:0> = 2'b01
			±8		pF	CV_RANGE<1:0> = 2'b10
			±4		pF	CV_RANGE<1:0> = 2'b11
Common Mode Capacitance Range	C$_{CM\_RANGE}$		48		pF	CV_RANGE<1:0> = 2'b00
			36		pF	CV_RANGE<1:0> = 2'b01
			24		pF	CV_RANGE<1:0> = 2'b10
			24		pF	CV_RANGE<1:0> = 2'b11
CAPDAC Range		0		63.5	pF	0.5pF/LSB
PADC Resolution	RESRAW		24		Bits	
PADC Output Data Rate	ODR_P	5		4800	Hz	
PADC ENOB	ENOB_P	Refer to Table 6.1			Bits	Depends on ODR_P
Excitation Source (EXC)						
Excitation Frequency	CV_FREQ		76.8		kHz	
Excitation Voltage Amplitude	VAC		2	2.2	V	
Drivability	DRV		50		pF	Allow ground capacitance
Temperature Measurement Channel (Internal and External Temperature Sensor)						
TADC Resolution	RES_T	24			Bit	
TADC GAIN	GAIN_T	1		4		1, 2, 4
TADC Output Data Rate	ODR_T	5		4800	Hz	
TADC ENOB	ENOB_T	Refer to Table 6.3				
Error of Internal Temperature Sensor			±1	±2	℃	-40~125 ℃
TEMP Input Impedance			1		Gohm	
LIN Interface						
Input Low Level Voltage Receiver	V$_{RECL}$			0.4	VDDHV	
Input High Level Voltage	V$_{RECH}$	0.6			VDDHV	

Receiver						
Input Hysteresis Receiver	V_{RECHYS}	0.08		0.12	VDDHV	$V_{RECHYS} = V_{RECH} - V_{RECL}$
Input Center Point Receiver	V_{BUS_CNT}	0.475	0.5	0.525	VDDHV	$V_{BUS\_CNT} = (V_{RECH} + V_{RECL})/2$
Output Low Level Voltage Transmitter	V_{LINL}	0.6	1.2	2.0	V	
Output High Level Voltage Transmitter	V_{LINH}	0.9		1	VDDHV	
Pull Up resistance VDDHV to LIN	R_{LINPU}	20	30	47	kohm	in series with diode to VDDHV
Output Capacitance LIN	C_{LIN_OUT}			250	pF	
Output Current Limitation LIN Output Driver	I_{LIM}	40	90	200	mA	Sink, driver on, $V_{LIN} = $ VDDHV
Input Current LIN Dominant	$I_{LINPASdom}$	-1			mA	$V_{LIN} = 0V$, VDDHV = 12V Driver off
Input Current LIN Recessive	$I_{LINPASrec}$		3	20	µA	$V_{LIN} \geqslant$ VDDHV $7V \leqslant V_{LIN} \leqslant 18V$ $7V \leqslant$ VDDHV $\leqslant 18V$ Driver off
Input Current LIN Lost GND	I_{LIN_NOGND}	-1		1	mA	$0V \leqslant V_{LIN} \leqslant 18V$ VDDHV = 12V Lost GND
Input Current LIN Lost Supply				20	µA	$0V \leqslant V_{LIN} \leqslant 18V$ VDDHV = 0V
Voltage Drop over Pull Up Diode	$V_{SerDiode}$	0.4	0.7	1	V	
TXD Timeout	$t_{TXDTIMEOUT}$	10	19	30	ms	
Slew Rate (Rising and Falling Edges)	SR_{LIN}	0.5	1.3	3	V/µs	Refer to Figure 4.1
Propagation Delay Receiver:LIN low -> RXD low	$t_{RXDLINL}$	2	4	6	µs	Refer to Figure 4.2
Propagation Delay Receiver:LIN high-> RXD high	$t_{RXDLINH}$	2	4	6	µs	Refer to Figure 4.2
Symmetry of Receiver Propagation Delay	$t_{RXDLINSYM}$	-2		2	µs	$t_{RXDLINH} - t_{RXDLINL}$

Symmetry of Transmitter Propagation Delay	$t_{TXDLINSYM}$	-2		2	µs	$t_{TXDLINL}$ - $t_{TXDLINH}$
Diagnostic and Alarm						
Over Temperature Protection	T_{OT}	170	180		℃	
VDDHV Over Voltage	$V_{OVDetThres}$		35		V	
VDDHV Under Voltage	$V_{UVDetThres}$		6		V	
OSC						
ADC Clock	FOSC_MOD		1.2		MHz	
Clock Rate Error	FOSC_ERR	-1%		1%		-40~125℃
PWM						
PWM Frequency	FPWM		600		Hz	
PWM Resolution	RPWM		12		Bit	
EEPROM						
Programming Temperature	T_{EEP}	-25		105	℃	
Endurance	N_{EEP}	500				
Programming Time	t_{EEP}		800		ms	
Date Retention	t_{DR}	10			year	150℃
Serial Interface						
OWI Bit Period	T_{owi}	0.03		4	ms	
OWI Pull-up Resistance	R_{owi_pu}	300			ohm	
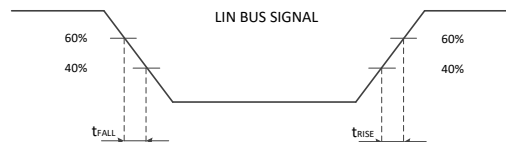
Figure 4.1 t_{FALL} and t_{RISE}
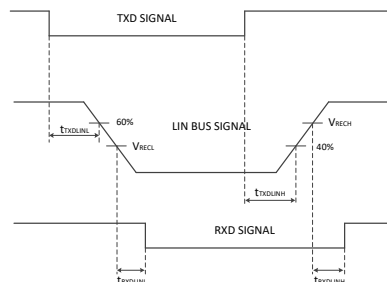
Figure 4.2 $t_{TXDLINSYM}$ and $t_{RXDLINSYM}$

5. Register Description

The register map of the NSC9262 includes two parts, normal registers and EEPROM registers. The normal registers include data registers and some control registers, while the EEPROM registers are mainly configuration registers and calibration coefficients. All EEPROM registers should be written through external interface in command mode (register 'CMD' = '0x00').

5.1. Normal Registers

SOFT_RESET(R/W)

Addr	Bit	Register Name	Default	Description
0x00	5, 2	SOFTRESET	1'b0	Set either of these two bits to 1 to reset the chip. Return to 0 after reset.

ERROR_STATUS (Read Only)

Addr	Bit	Register Name	Default	Description
0x02	7 – 3	Reserved	5'b00000	Reserved
	2	CRC_ERR	1'b0	1: CRC error detected during EEPROM loading; When CRC error is asserted, EEPROM register bits 'OWI_DIS', 'OWI_AC_EN','OWI_WINDOW,''JFET_DIS','VREF_DIS','EEPROM_LOCK' are forced to 0.
	1	LOADING_END	1'b0	1: EEPROM loading end flag
	0	ROM_CHECK_ERR	1'b0	1: ROM check error flag

PDATA (Read Only, Primary Channel Data Register)

Addr	Bit	Register Name	Default	Description
0x06	7 – 0	PDATA<23:16>	0x00	Signed, 2's complement:
0x07	7 – 0	PDATA<15:8>	0x00	When 'RAW_P' = 1, store the ADC output of primary channel;
0x08	7 – 0	PDATA<7:0>	0x00	When 'RAW_P' = 0, store the calibrated primary channel data.

TDATA (Read Only, Temperature Channel Data Register)

Addr	Bit	Register Name	Default	Description
0x09	7 – 0	TDATA<23:16>	0x00	Signed, 2's complement:
0x0a	7 – 0	TDATA<15:8>	0x00	When 'RAW_T' = 1, store the ADC output of temperature channel;
0x0b	7 – 0	TDATA<7:0>	0x00	When 'RAW_T' = 0, store the calibrated temperature data, LSB = $1/2^{16}$℃. Real Temperature = $TDATA/2^{16}+25$℃

COMMAND (R/W, Command Register)

Addr	Bit	Register Name	Default	Description
0x30	7 – 0	CMD<7:0>	0x03	0x00: Command mode, all EEPROM can be written only in command mode; 0x03: Active mode; 0x33: Enter EEPROM program mode

QUIT_OWI (Write Only)

Addr	Bit	Register Name	Default	Description
0x61	7 – 0	QUIT_OWI <7:0>	0x00	Write '0x5D' to this register to quit OWI communication. If'QUIT_OWI_CNT'= 0x00, quit OWI communication permanently; If 'QUIT_OWI_CNT' is not 0x00, quit OWI mode temporarily with a certain time and then get back to OWI mode.

QUIT_OWI_CNT (R/W)

Addr	Bit	Register Name	Default	Description
0x62	7 – 0	QUIT_OWI_CNT<7:0>	0x00	Time for temporarily quit OWI communication Mode. 0x00: Quit forever, 0x01: 50ms, 0x02: 100ms … 0xFF: 12.8s

EE_PROG (R/W)

Addr	Bit	Register Name	Default	Description
0x6a	7 – 0	EE_PROG<7:0>	0x00	Write '3E' to this register to start EEPROM Programming. Automatically cleared to '0x00' after programming finished.

5.2. EEPROM Registers

SYS_CONFIG (R/W)

Addr	Bit	Register Name	Default	Description
0xa1	7	CAL_MODE	1'b0	0: One segment calibration with the 2nd order temperature coefficients; 1: Two segment calibration with the 1st order temperature coefficients
	6-3	Reserved	4'b0000	Reserved
	2	LIN_PID2_en	1'b0	0: disable LIN Product Identification – PID2 (internal use); 1: enable LIN Product Identification – PID2 (internal use)
	1	OWI_DIS	1'b0	1: OWI disabled (won't be effective until next power on reset or soft reset after EEPROM is programmed)
	0	Reserved	1'b0	Reserved

OUTPUT_CONFIG (R/W)

Addr	Bit	Register Name	Default	Description
0xa2	7 - 6	LIN_version	2'b00	00: LIN version1.3; 01: LIN version1.3; 10: LIN version2.0; 11: LIN version2.1(2.2)
	5	LIN_save_config_dis	1'b0	0: enable saving configuration to EEPROM through LIN; 1: disable saving configuration to EEPROM through LIN
	4	LIN_sleep_mode_dis	1'b0	0: enable sleep mode; 1: disable sleep mode

| | 3 | LIN_sample_point | 1'b0 | 0: 3 samples/bit
1: 5 samples/bit |
| | 2 - 0 | Reserved | 3'b000 | Reserved |

CV_CONFIG (R/W)

Addr	Bit	Register Name	Default	Description
0xa3	7	Reserved	1'b0	Reserved.
	6 – 0	CAPOFF<6:0>	7'b0000000	Set internal CAPDAC offset for input CAPOFF = CAPOFF<6:0>*0.5pF

PCH_Config1 (R/W)

Addr	Bit	Register Name	Default	Description
0xa4	7 – 6	Reserved	2'b00	Reserved.
	5 – 4	CV_RANGE<1:0>	2'b00	00: CRANGE = ±16pF, CCM_RANGE = 48pF ; 01: CRANGE = ±12pF, CCM_RANGE = 36pF ; 10: CRANGE = ±8pF, CCM_RANGE = 24pF ; 11: CRANGE = ±4pF, CCM_RANGE = 24pF ;
	3 – 0	ODR_P<3:0>	4'b0000	PADC Output Data Rate Setting 0000: 4.8kHz, 0001: 2.4kHz, 0010: 1.2kHz, 0011: 600Hz, 0100: 300Hz, 0101: 150Hz, 0110: 75Hz, 0111: 37.5Hz, 1000: 20Hz(with 60Hz notch), 1001: 20Hz（with 50Hz notch）, 1010: 10Hz（with 60Hz notch）, 1011: 10Hz（with 50Hz notch）, 1100: 5Hz（with 60Hz notch）, 1101: 5Hz (with 50Hz notch), 1110,1111: PADC disabled

PCH_Config2 (R/W)

Addr	Bit	Register Name	Default	Description
0xa5	7 – 6	DIG_GAIN<1:0>	2'b00	Digital gain configuration 00: 1X, 01:2X, 10: 4X, 11: 8X
	5 – 1	Reserved	5'b00000	Reserved.
	0	RAW_P	1'b0	0: update calibrated sensor data into 'PDATA' register. 1: update raw primary ADC data into 'PDATA' register after conversion.

TCH_Config (R/W)

Addr	Bit	Register Name	Default	Description
0xa6	7	EXT_TEMP	1'b0	0: Internal temperature sensor selected; 1: External temperature sensor selected (TEMP pin as external temperature sensor input)
	6 – 5	GAIN_T<1:0>	2'b00	Gain for External temperature sensors; 00: 1X, 01: 2X, 10/11: 4X (Fixed 4X for internal temperature)
	4 – 1	ODR_T	4'b0000	TADC output data rate, similar as ODR_P

| | | | | 0000: 4.8kHz, 0001: 2.4kHz, 0010: 1.2kHz, 0011: 600Hz, 0100: 300Hz, 0101: 150Hz, 0110: 75Hz, 0111: 37.5Hz, 1000: 20Hz (with 60Hz notch), 1001: 20Hz (with 50Hz notch), 1010: 10Hz (with 60Hz notch), 1011: 10Hz (with 50Hz notch), 1100: 5Hz (with 60Hz notch), 1101: 5Hz (with 50Hz notch), 1110, 1111: TADC disabled |
| | 0 | RAW_T | 1'b0 | 1: Store the raw TADC output into 'TDATA' register; 0: Store the calibrated TADC data into 'TDATA' register |

CLAMPH (R/W)

Addr	Bit	Register Name	Default	Description
0xa7	7 – 0	CLAMPH<7:0>	0x00	high clamp voltage: 0x00: VoutFS. 0xFF: 1/2 VoutFS

CLAMPL (R/W)

Addr	Bit	Register Name	Default	Description
0xa8	7 – 0	CLAMPL<7:0>	0x00	low clamp voltage: 0x00: 0V. 0xFF: 1/2VoutFS

OFFSET0 (R/W)

Addr	Bit	Register Name	Default	Description
0xa9	7 – 0	OFF0<15:8>	0x00	Sensor calibration coefficient, offset at T0. LSB = $1/2^{15}$, RANGE (-1, +1)
0xaa	7 – 0	OFF0<7:0>	0x00	

CTC1 (R/W)

Addr	Bit	Register Name	Default	Description
0xab	7 – 0	CTC1<15:8>	0x00	Sensor calibration coefficient,
0xac	7 – 0	CTC1<7:0>	0x00	CAL_MODE = 0: the 1st order temperature coefficient of offset. LSB = $1/2^{22}$, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1st order temperature coefficient of offset for segment 0. LSB = $1/2^{22}$, RANGE (-0.00781, +0.00781)

CTC2 (R/W)

Addr	Bit	Register Name	Default	Description
0xad	7 – 0	CTC2<15:8>	0x00	Sensor calibration coefficient,
0xae	7 – 0	CTC2<7:0>	0x00	CAL_MODE = 0: the 2nd order temperature coefficient of offset. LSB = $1/2^{29}$, RANGE (-6.1e-5, 6.1e-5); CAL_MODE = 1: the 1st order temperature coefficient of offset for segment 1, LSB = $1/2^{22}$, RANGE (-0.00781, +0.00781)

S0 (R/W)

Addr	Bit	Register Name	Default	Description
0xaf	7 – 0	S0<15:8>	0x00	Sensor calibration coefficient, sensitivity at T0. LSB = $1/2^{15}$ (unsigned), RANGE (0, 2)
0xb0	7 – 0	S0<7:0>	0x00	

STC1 (R/W)

Addr	Bit	Register Name	Default	Description
0xb1	7 – 0	STC1<15:8>	0x00	Sensor calibration coefficient,
0xb2	7 – 0	STC1<7:0>	0x00	CAL_MODE = 0: the 1st order temperature coefficient of sensitivity. LSB = $1/2^{22}$, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1st order temperature coefficient of sensitivity for segment 0. LSB = $1/2^{22}$, RANGE (-0.00781, +0.00781)

STC2 (R/W)

Addr	Bit	Register Name	Default	Description
0xb3	7 – 0	STC2<15:8>	0x00	Sensor calibration coefficient,
0xb4	7 – 0	STC2<7:0>	0x00	CAL_MODE = 0: the 2nd order temperature coefficient of sensitivity. LSB = $1/2^{29}$, RANGE (-6.1e-5, 6.1e-5); CAL_MODE = 1: the 1st order temperature coefficient of sensitivity for segment 1. LSB = $1/2^{22}$, RANGE (-0.00781, +0.00781)

KS (R/W)

Addr	Bit	Register Name	Default	Description
0xb5	7 – 0	KS<15:8>	0x00	Sensor calibration coefficient, the 2nd order nonlinearity coefficient. LSB = $1/2^{15}$, RANGE (-1, +1)
0xb6	7 – 0	KS<7:0>	0x00	

KSS (R/W)

Addr	Bit	Register Name	Default	Description
0xb7	7 – 0	KSS<15:8>	0x00	Sensor calibration coefficient, the 3rd order nonlinearity coefficient, LSB = $1/2^{16}$, RANGE (-0.5, +0.5)
0xb8	7 – 0	KSS<7:0>	0x00	

SUPPLIER_ID (R/W)

Addr	Bit	Register Name	Default	Description
0xb9	7 – 0	SUPPLIER_ID<15:8>	0x00	LIN Product Identification – Supplier ID
0xba	7 – 0	SUPPLIER_ID<7:0>	0x00	

FUNCTION_ID (R/W)

Addr	Bit	Register Name	Default	Description
0xbb	7 – 0	FUNCTION_ID<15:8>	0x00	LIN Product Identification – Function ID
0xbc	7 – 0	FUNCTION_ID<7:0>	0x00	

VARIANT_ID (R/W)

Addr	Bit	Register name	Default	Description
0xbd	7 – 0	VARIANT_ID<7:0>	0x00	LIN Product Identification – Variant ID

LIN_NAD(R/W)

Addr	Bit	Register name	Default	Description
0xbe	7 – 0	LIN_NAD<7:0>	0x00	LIN node address – LIN NAD

T0 (R/W)

Addr	Bit	Register Name	Default	Description
0xbf	7 – 0	T0<7:0>	0x00	Temperature Sensor calibration coefficient, reference temperature point, real reference temperature, REAL_T0 = T0 + 25. LSB = 1. RANGE (-128, +127)

KTS (R/W)

Addr	Bit	Register Name	Default	Description
0xc0	7 – 0	KTS<7:0>	0x00	Temperature Sensor calibration coefficient, the 2nd order nonlinearity coefficient for external temperature sensor. LSB = $1/2^7$, RANGE (-1, +1)

MTO (R/W)

Addr	Bit	Register Name	Default	Description
0xc1	7 – 0	MTO<15:8>	0x00	Temperature Sensor calibration coefficient, offset coefficient of external temperature sensor, MTO: LSB = $1/2^{15}$, RANGE (-1, +1)
0xc2	7 – 0	MTO<7:0>	0x00	

KT (R/W)

Addr	Bit	Register Name	Default	Description
0xc3	7 – 0	KT<15:8>	0x00	Temperature Sensor calibration coefficient: sensitivity coefficient of external temperature sensor, KT: LSB = $1/2^{12}$, RANGE (-8, +8)
0xc4	7 – 0	KT<7:0>	0x00	

TEMP_THRES (R/W)

Addr	Bit	Register Name	Default	Description
0xc5	7 – 0	TEMP_THRES_H<7:0>	0x00	Upper limit of temperature data
0xc6	7 – 0	TEMP_THRES_L<7:0>	0x00	Lower limit of temperature data

SPARE(R/W)

Addr	Bit	Register Name	Default	Description
0xc7	7 – 0	SPARE1<7:0>	0x00	Spare register 1
0xc8	7 – 0	SPARE2<7:0>	0x00	Spare register 2
0xd5	7 – 0	SPARE3<7:0>	0x00	Spare register 3
0xd6	7 – 0	SPARE4<7:0>	0x00	Spare register 4

PADC_OFF (R/W)

Addr	Bit	Register Name	Default	Description
0xc9	7 – 0	PADC_OFF<23:16>	0x00	PADC calibration coefficient: PADC offset, LSB = 1/2^23, RANGE (-1, +1)
0xca	7 – 0	PADC_OFF<15:8>	0x00	
0xcb	7 – 0	PADC_OFF<7:0>	0x00	

PADC_GAIN (R/W)

Addr	Bit	Register Name	Default	Description
0xcc	7 – 0	PADC_GAIN<15:8>	0x00	PADC calibration coefficient: PADC gain, LSB = 1/2^16, RANGE (-0.5, +0.5)
0xcd	7 – 0	PADC_GAIN<7:0>	0x00	

P0 (R/W)

Addr	Bit	Register Name	Default	Description
0xce	7 – 0	P0 <7:0>	0x00	Sensor calibration coefficient: reference pressure point for nonlinearity calibration, LSB = 1/2^7, RANGE (-1, 1)

SERIAL_NUMBER (R/W)

Addr	Bit	Register Name	Default	Description
0xcf	7 – 0	SERIAL_NUMBER<31:24>	0x00	LIN Product Identification – Serial Number
0xd0	7 – 0	SERIAL_NUMBER <23:16>	0x00	
0xd1	7 – 0	SERIAL_NUMBER <15:8>	0x00	
0xd2	7 – 0	SERIAL_NUMBER <7:0>	0x00	

MESSAGE_ID1 (R/W)

Addr	Bit	Register name	Default	Description
0xd3	7 – 0	MESSAGE_ID1<15:8>	0x00	LIN Product Identification – Message ID1 Only for PID1
0xd4	7 – 0	MESSAGE_ID1<7:0>	0x00	

PID1 (R/W)

Addr	Bit	Register name	Default	Description
0xd7	7-0	PID1<7:0>	0x00	LIN Product Identification – PID1

PID2 (R/W)

Addr	Bit	Register name	Default	Description
0xd8	7 - 0	PID2<7:0>	0x00	LIN Product Identification – PID2 (internal use)

EEPROM_LOCK (R/W)

Addr	Bit	Register name	Default	Description
0xd9	7	EEPROM_LOCK	1'b0	1: EEPROM lock, set 1 and then EEPROM can't be programmed. (Won't be effective until next power on reset or soft reset after EEPROM is programmed)
	6 – 0	PartID (read only)	7'b0001001	NOVOSENSE chip ID,customer should not erase these bits

6. Function Description

6.1. Overview

The NSC9262 is a highly integrated and AEC-Q100 qualified sensor conditioner for capacitive sensors. The chip supports Over-voltage and Reverse voltage protection. LIN output compliant with Specification 1.3/2.0/2.1/2.2 is available, high voltage power supplied directly through VDDHV. The NSC9262 uses differential inputs with at most ±16pF differential input capacitance range and 76.8pF common mode capacitance range. The chip incorporates five parts: analog front-end module, digital module, LIN interface module, power supply module and serial interfaces. The block diagram of the NSC9262 is shown in Figure 6.1.

Analog front-end module includes a primary signal measurement channel with a C/V converter followed by a 24-bit $\Sigma\Delta$ ADC, a temperature measurement channel with also a 24-bit $\Sigma\Delta$ ADC, for precision sensor signal and temperature measurement.

The digital module is composed of registers, EEPROM, control logic, and a built-in MCU. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2nd order temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3rd order. The configuration parameters and coefficients for calibration are stored in the EERPOM of 64 bytes.

The LIN interface module includes LIN protocol control part and LIN physical transceiver part, compatible with LIN Specification 1.3//2.0/2.1/2.2. Meanwhile it supports diagnostic function of Class I.

The power supply module includes a high precision voltage reference, a sensor voltage driver, over-voltage and reverse voltage protection block.

The NSC9262 supports OWI serial interface, writing and reading registers of configuration, calibration coefficients and data. Through the highly integrated and flexible interface, the NSC9262 only needs one wire to realize sensor calibration, field verification and full scale range modification.
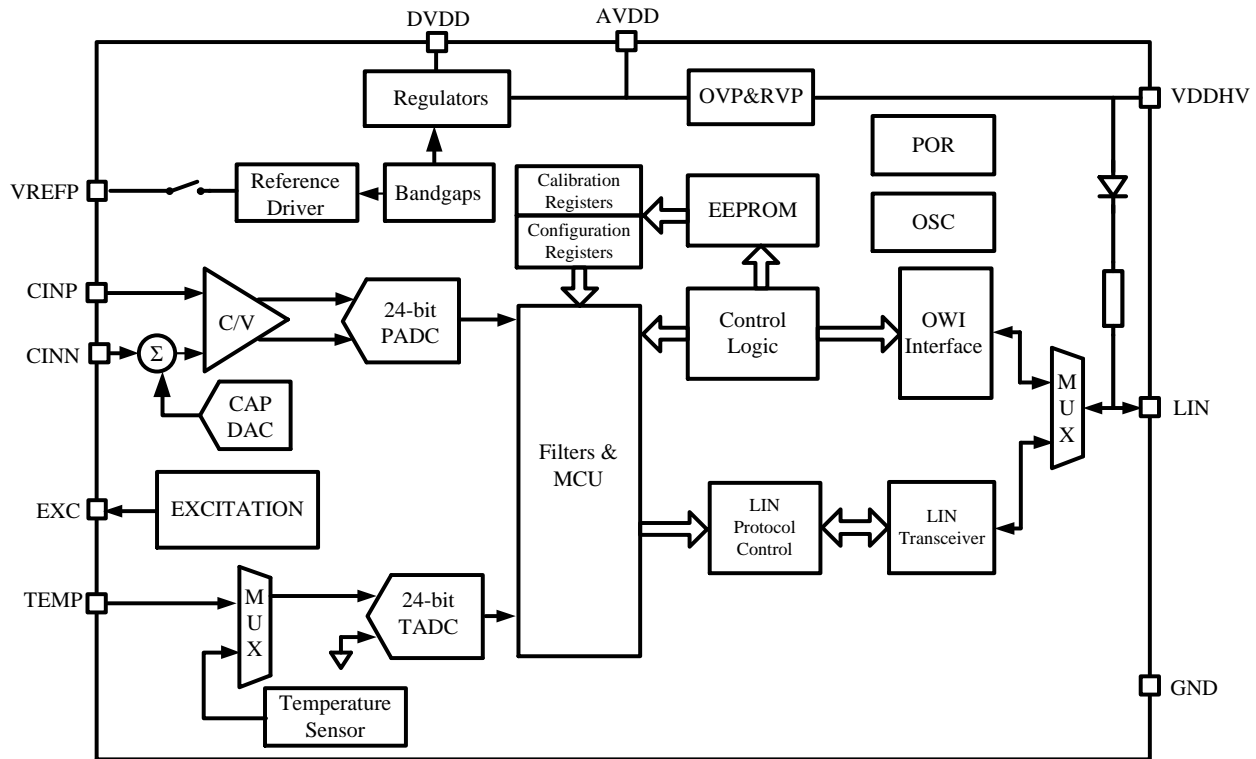
Figure 6.1 Block diagram of the NSC9262

6.2. Analog Front-end Module 1: Primary Signal Channel

6.2.1.Capacitance Measurement Mode

The NSC9262 generates a square wave at EXC pin with 76.8KHz frequency and 2V amplitude, which is used to drive input capacitor.

As shown in Figure 6.2, the external input capacitors are connected. The differential input capacitors' common plate is driven by the square wave at EXC pin. Since the voltage at CINP and CINN keeps constant, the input parasitic capacitance would not affect the output.
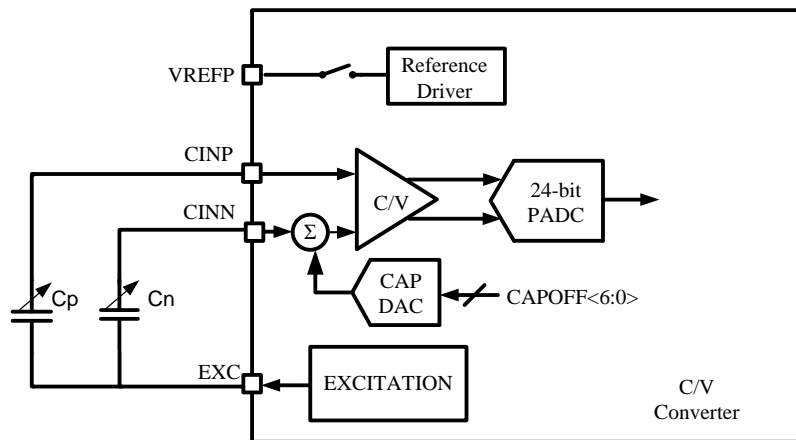
Figure 6.2 C/V converter at Drive Mode

6.2.2.The Measurement Range of C/V Converter

6.2.2.1. The Differential Input Capacitance Range

The PADC converts the analog output of C/V converter to digital output, which is filtered by a digital filter with 24-bit digital output PDATA$_{RAW}$. PDATA$_{RAW}$ is expressed by,

$$PDATA_{RAW} = \frac{Cp - Cn - CAPOFF}{|C_{RANGE}|} * 2^{23}$$

CAPOFF is an internal offset compensated capacitance configured by CAPOFF<6:0>. The capacitance step of CAPDAC is 0.5pF, so it's as large as 127*0.5pF = 63.5pF. CRANGE is the full-scale range of C/V measurement configured by CV_RANGE<1:0> as referred to Section 5.1. PDATA_RAW can be read from P channel data registers (Reg0x06, 07, 08) when RAW_P = 1. When RAW_P = 0, the built-in MCU will calibrate the sensor using sensor calibration coefficients and the data of temperature measurement. Therefore, the contents of PDATA registers are the sensor output after temperature calibration.

6.2.2.2. The Common Mode Capacitance Range

When the differential input capacitance is not out of range (PDATAraw is in between ± 1 after normalization), the common mode capacitance range is related to VREF and CV_RANGE<1:0> as referred to Section 5.2.

6.2.3. Digital Filter

The bandwidth and output data rate (ODR) of the digital filter can be set by 'ODR_P'. ODR can be set from 4.8 KHz to 5 Hz. The lower ODR, the lower noise the PADC output will have, in the cost of slower time response. Table 6.1 shows the effective number of bits (ENOB) of PADC output with different ODR_P settings. The relationship of ENOB with RMS noise is:

$$ENOB_{RMS} = 24 - log_2(RMS_{ADC})$$

RMSADC is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB (ENOBRMS) and noise free ENOB (ENOBNF) is shown as below:

$$ENOB_{NF} = ENOB_{rms} - 2.7$$

Table 6.1 ENOB$_{RMS}$ of PADC under different ODR settings

ODR_P(Hz)	CRANGE=$\pm16pF$	CRANGE=$\pm12pF$	CRANGE=$\pm8pF$	CRANGE=$\pm4pF$
4800	15.6	15.7	16.0	15.9
2400	15.9	15.9	16.2	16.0
1200	16.3	16.2	16.7	16.6
600	16.7	16.6	17.1	17.0
300	17.1	17.2	17.6	17.4
150	17.6	17.6	18.0	17.8
75	18.1	18.1	18.5	18.4
37.5	18.6	18.6	19.1	18.7
20	19.0	19.1	19.4	19.3
10	19.6	19.5	19.9	19.8
5	20.1	20.0	20.4	20.1

6.3. Analog Module 2: Temperature Measurement Channel

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. This channel works independently of the capacitance measurement channel. The NSC9262 supports both internal temperature sensor and external temperature sensor, selected by register bit 'EXT_TEMP' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digital filtered. The ODR setting of the temperature measurement channel is the same as the primary signal channel, set by 'ODR_T'. When the temperature difference between the sensor element and the NSC9262 chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as RTD or the bridge resistor itself, etc. Through different 'RAW_T' setting, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

6.3.1. Internal Temperature Sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registers reg0xC1, reg0xC2 and reg0xC3. When 'RAW_T' is set to 0 and 'GAIN_T' is set to 4X, the NSC9262 can provide a temperature reading in degree Celsius, in the format of

$$T = TDATA/2\,^\wedge 1\,6 + 25℃$$

For example, 'TDATA = 0x1FF24B' corresponding to 56.95°C. The relationship between the noise of the internal temperature sensor and 'ODR_T' setting is shown in Table 6.2.

Table 6.2 RMS noise of internal temperature sensor under different ODR_T

ODR (Hz)	4800	2400	1200	600	300	150	75	37.5	18.75	10	5
RMS Noise in ℃	0.0079	0.0060	0.0045	0.0038	0.0032	0.0020	0.0015	0.0011	0.0008	0.0008	0.0007

6.3.2. External Temperature Sensor

When external temperature sensor mode is selected, the temperature sensing signal input from the TEMP pin is buffered for TADC conversion. The reference voltage of the TADC is also VREF. The gain of the TADC can be 1X, 2X and 4X. The relationship between TDATA$_{RAW}$ and the temperature input is

$$TDATA_{RAW} = VTEMP * GAIN\_T/VREF * 2^{23}$$

When RAW_T = 0, the built-in MCU calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. Please refer to application note.Novosns provided for calibration description details. The external temperature sensing can be done in many ways, including RTD and sensor bridge resistance itself. Figure 6.3 gives an example using a low TC drift resistor to sense the bridge resistance, which is usually proportional to the temperature of the sensor element.
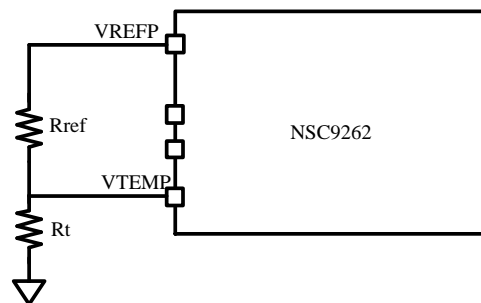

Figure 6.3 External temperature sensing using sensor bridge and a reference resistor

The output data rate of TADC can be set by 'ODR_T', similar as the primary signal channel. The relationship between ODR_T and the ENOB of TADC is shown in Table 6.3.

Table 6.3 ENOB of TADC under different ODR_T (External temperature sensor mode)

ODR_T(Hz)	ENOB		
	GAIN_T = 1	GAIN_T = 2	GAIN_T = 4
4800	17.2	17.0	16.4
2400	17.6	17.4	16.7
1200	18.0	17.6	16.7
600	18.3	17.8	16.9
300	18.6	18.0	17.1
150	19.0	18.4	17.5
75	18.9	18.1	17.1
37.5	19.4	18.2	17.6
20	19.8	18.9	18.0
10	19.8	19.1	18.0
5	20.4	19.4	18.3

6.4. LIN interface module

The LIN interface module includes LIN protocol control part and LIN physical transceiver part, as shown in Figure 6.4.

LIN protocol control part is used for frame structure in data link layer, node configuration in transport layer and data process of measuring channels in application layer. Meanwhile it supports diagnostic function of Class I. The integrated LIN transceiver part is compatible with LIN Specification 1.3/2.0/2.1/2.2, which reduces the external electronic components and simplify the complexity of sensor system.

An internal time-out filter prevents the LIN-bus from being permanently driven in dominant state. If $T_{XD-signal}$ is at low level for longer than $t_{TXDTIMEOUT}$, the pin LIN is switched off to recessive mode. To reset this mode the pin TXD has to be switched high.

An internal wake-up filter helps the chip to switch from low-power sleep mode to normal operation mode, with wake-up event of qualified pulse signals detected from LIN-bus.

For a detailed description, refer to the application note "*NSC9262 LIN Interface Description*".
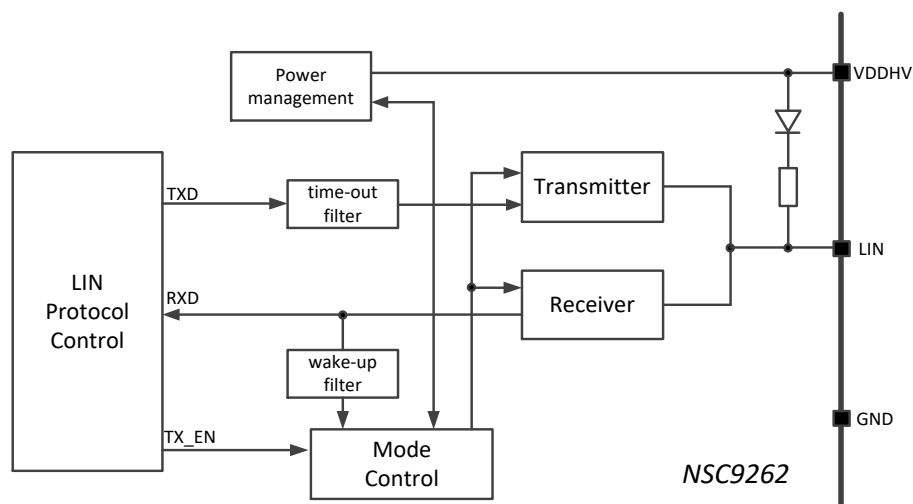
Figure 6.4 LIN interface module diagram

6.5. Power Management and Sensor Drive

The NSC9262 internally includes a precision bandgap reference with very low temperature drift, less than 0.2% during full temperature range (-40~125°C). This reference voltage is used in the constant voltage or current driving circuits for clock generator and ADC/DAC etc.

6.5.1. Power on Reset

A POR block is integrated in the NSC9262 for power on reset and EEPROM loading. When AVDD<2.5V, the chip is in reset state. After AVDD > 2.5V, the POR output is released and EEPROM is loaded afterwards. The POR circuits have 100mV hysteresis, that is to say the chip won't go into the reset state again until the AVDD is dropped as low as 2.4V.

6.5.2. Over-voltage and Reverse-voltage Protection

The NSC9262 integrates an Over-voltage and Reverse-voltage Protection on power supply. Over-voltage as high as 40V and Reverse-voltage as low as -40V are allowed. In the case of Over-voltage, AVDD is clamped at a normal voltage as to protect the internal circuit.

6.6. Build-in MCU Core and Control Logics

6.6.1. Work Modes

Two Different work modes are supported by the NSC9262, command mode and active mode, which can be configured by the register 'CMD' (Reg0x30).

6.6.1.1. Command Mode

The command mode can be entered by writing the register 'CMD' with 0x00, which is used for configuring the chip outside. All the EEPROM registers (from Reg0xA1 - Reg0xD9) can be modified only in this mode.

6.6.1.2. Active Mode

The active mode is the default mode after powering up, which can also be entered by writing the register 'CMD' with 0x03. In this mode, the primary measurement channel and the temperature channel continuously update their measured values into the 'PDATA' or 'TDATA' registers, and the selected output mode will be activated simultaneously. When the register bit 'RAW_P/T' = 1, the ADC conversion results will be put into the 'PDATA' or 'TDATA' directly; otherwise, every time the primary measurement channel ADC conversion ends, the built-in MCU core performs once sensor calibration flow with the latest temperature value measured.

The shadow registers inside the NSC9262 can also guarantee a non-glitch reading by keeping the 'PDATA' and 'TDATA' registers stable during once serial interface reading. Note that, the multiple bytes of one measured data should be read out together in one multi-byte serial interface reading command.

6.6.2. EEPROM

64 bytes EEPROM is contained in the NSC9262 to store the chip configurations and sensor calibration coefficients.

6.6.2.1. Loading

The contents of the EEPROM will be loaded into the shadow registers automatically after powering up or soft-reset with the CRC checking. If the calculated CRC result does not match with what stored in the EEPROM, the 'CRC_ERROR' bit will be set and the analog output state will be decided according to the fault diagnostic and alarm configurations. Another status register bit 'LOADING_END' will be set after the loading completes.

6.6.2.2. Programming

EEPROM registers will not be programmed into the EEPROM directly after OWI writing. The contents of the EEPROM registers will be programmed into the EEPROM by following sequences:

1.Set the register byte 'COMMAND' (Reg0x30) with 0x33 to enter EEPROM programming mode;

2.Writing the register byte 'EE_PROG' (Reg0x6A) with 0x3E to start EEPROM programming.

During EEPROM programming, a new CRC check code will be generated according to the contents of the EEPROM registers and will be programmed to the EEPROM simultaneously. The content of the 'EE_PROG' register will automatically come back to 0x00 to indicate the programming finish. A re-powering up or soft-reset is needed to reload the EEPROM contents back to the EEPROM registers to check the programmed value.

6.6.2.3. Lock and Unlock

The EEPROM inside the NSC9262 can be locked by setting the 'EEPROM_LOCK' bit and programming it into the EEPROM. After locked, the EEPROM cannot be programmed again, and only a special EVAL-kits provided by NOVOSENSE can unlock it.

6.6.3. Built-in MCU Core

The NSC9262 is integrated with a built-in MCU core, which performs the signal processing, sensor calibration, EEPROM loading and programming etc. The MCU's program code is pre-stored in the internal ROM, which cannot be modified by customers.

6.6.4. Calibration

The NSC9262 can compensate the sensor with offset, sensitivity, up to the 2nd order offset temperature drift, up to the 2nd order sensitivity temperature drift, up to the 3rd order non-linearity.

6.7. Diagnosis and Alarm

NSC9262 can detect open of the capacitor input pin, or leakage current of capacitor input pin.

NSC9262 supports over-voltage detection and under-voltage detection. The over-voltage detection threshold is 35V and the under-voltage detection threshold is 6V.

NSC9262 supports temperature out-of-range check and thermal shutdown protection. The over temperature threshold is 180°C. When thermal shut down happens, the LIN output interface is disabled until the temperature recovers. NSC9262 records whether there is thermal shut down happens after recent power-on-reset. This function may fail over guaranteed operation temperature.

Besides the sensor diagnostic functions, the NSC9262 supports ROM failure check, EEPROM CRC check, watch-dog timeout check, out-of-range detection of measuring channels and the error handling function for LIN protocol, including Response Error, Checksum Error and Bit Error.

The Fault Type can be identified through the status bits from the LIN output.

7. Serial Interface

The OWI serial interface is supported in the NSC9262 to configure registers, program EEPROM and read measured data. When register bit 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is defined as the OWI entering window. If a specific 24 bits OWI entering pattern is detected via OWI pin in this window, the chip enters OWI communication mode, otherwise enters analog output mode (as shown in Figure 7.1).
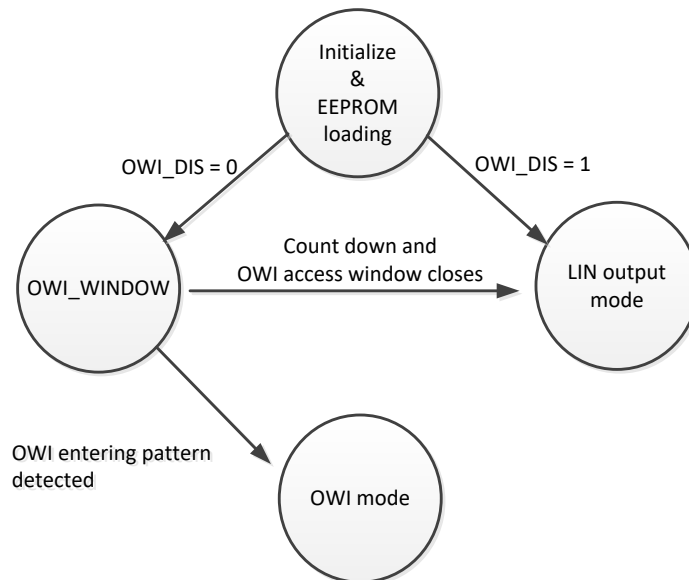

Figure 7.1 Definition of serial communication mode

7.1. OWI Pin Configuration

The OWI pin is shared with the LIN pin as open-drain output. An external pull-up resistor is needed for the OWI pin.

7.2. Timing Spec

Table7.1 OWI Timing Spec

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{period}	OWI bit period		20		4000	µs
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	µs
t_{stop}	Stop condition time		2			t_{period}
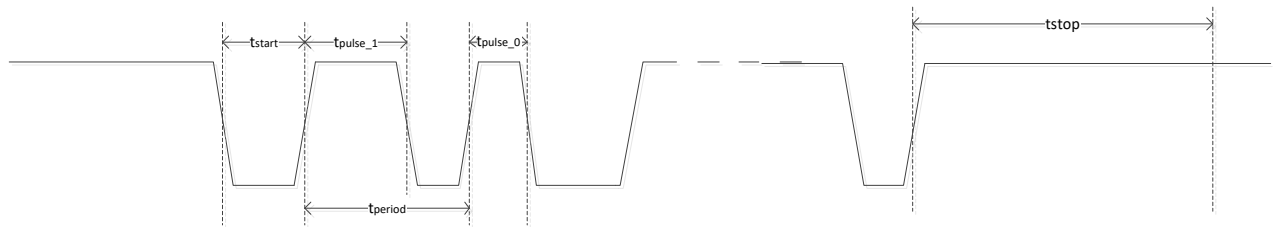
Figure 7.2 OWI Timing

7.3. Enter OWI Mode

If 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is OWI entering window. If a special 24 bits OWI entering pattern (0xB5A6C0, as shown below) is detected via OWI pin in this window, the chip enters OWI communication mode. Under this setting, the OUT pin is disabled during the OWI window and OWI mode; the OWI pin and the OUT pin can be shorted together to support 3-wire sensor products.

If 'OWI_WINDOW' = 1, the OWI window's length becomes infinite, the OUT pin is activated during OWI window and OWI mode, and the OWI pin and OUT pin cannot be shorted together.
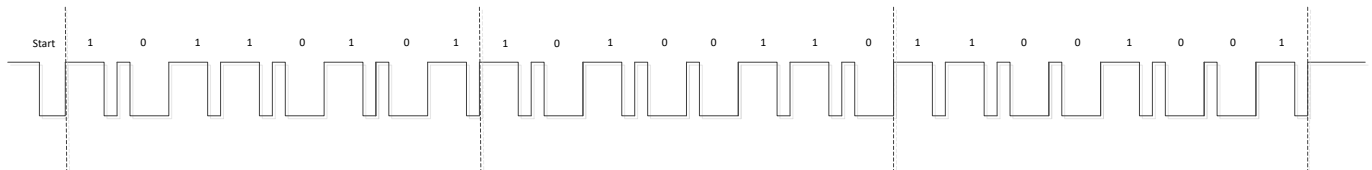
Figure 7.3 OWI Entering Pattern

In OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed during the entire communication, so the bit period during OWI communication should keep the same as the OWI entering pattern.

7.4. OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state a low pulse (return to high) with a pulse width between 20us to 4ms indicates a start condition. Every command has to be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c)   Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line to reach a constant high or low voltage level for at least twice of the bit period ($t_{Bperiod}$).

d)   Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number and a read/write-bit (0-write, 1-read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1 byte, 01: 2 bytes, 10: 3 bytes, 11: 4 bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e)   Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.
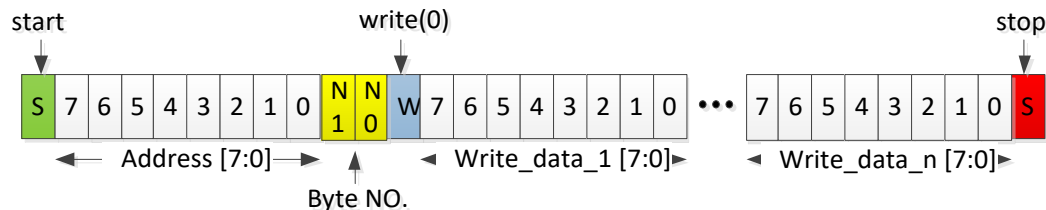

Figure 7.4 OWI Write Operation

f)   Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is the content in the addressed register and following ones. Each data bytes include 8 bits of data and 2 bits of parity check code C1 and C0,

C1 = Read_data [7] ^ Read_data [5] ^ Read_data [3] ^ Read_data [1];

C0 = Read_data [6] ^ Read_data [4] ^ Read_data [2] ^ Read_data [0].

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.
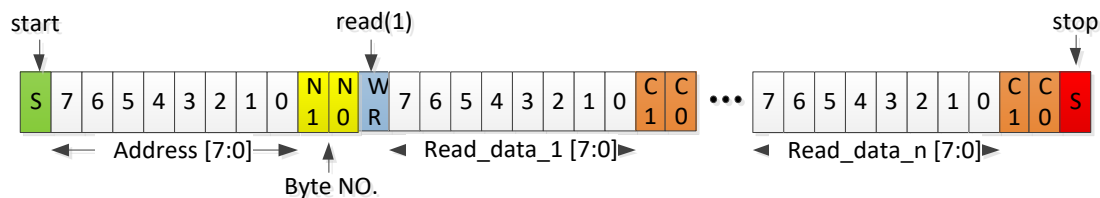

Figure 7.5 OWI Read Operation

7.5. Quit OWI Communication

Writing Reg0x61 with 0x5d during OWI mode results in quitting the OWI communication for LIN output.

8. Application Note

8.1. Typical Application Circuit1

Capacitive sensor application circuit with LIN output is shown in Figure 8.1.
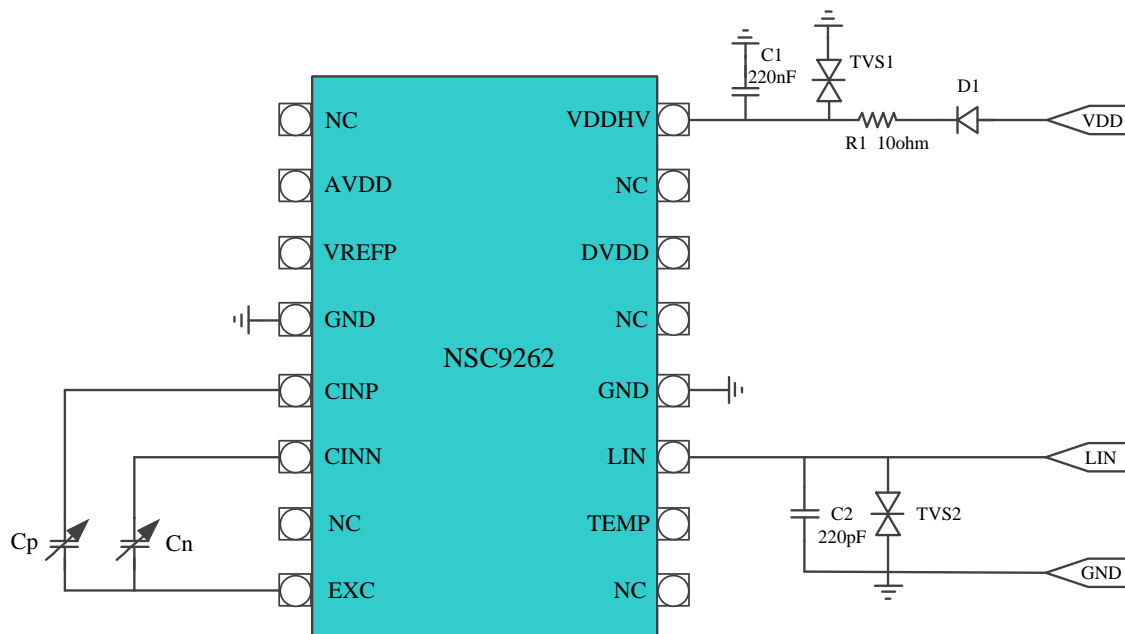

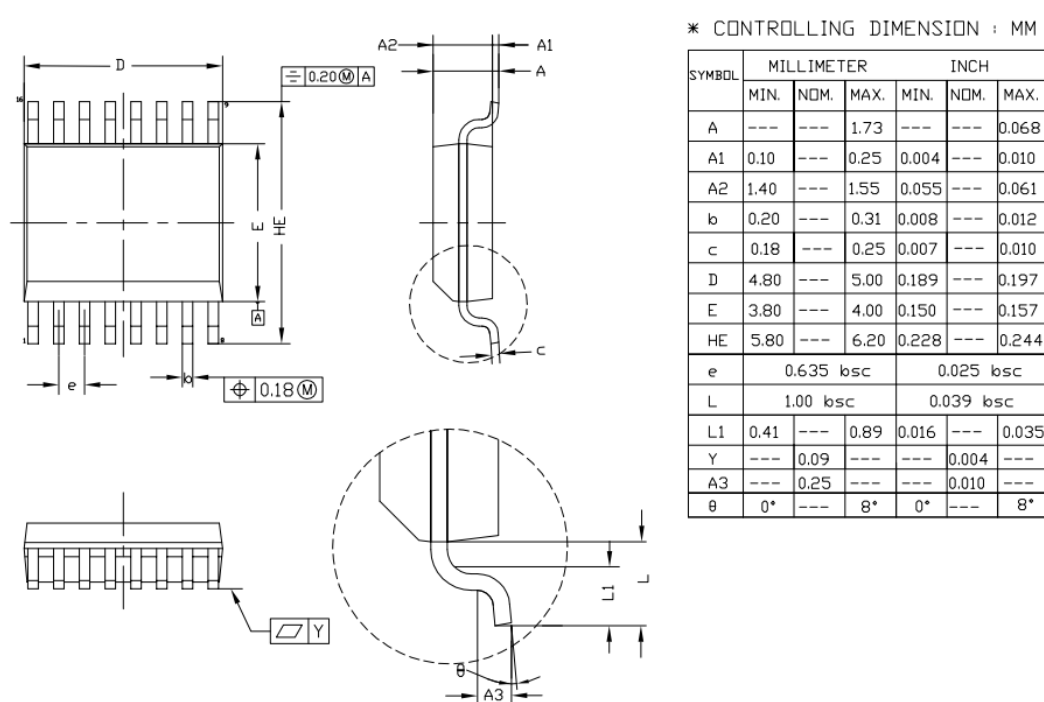Figure 8.1 Capacitive Sensor with LIN output

9. Package Information

Figure 9.1 SSOP16 package shape and dimension

10. Ordering Information

Part Number	Temperature	Vehicle specification level	MSL	Package Type	SPQ
NSC9262_Q0SSR	-40 to 150℃	AEC-Q100 Grade 0	1	SSOP16	2500

11. Tape and Reel Information
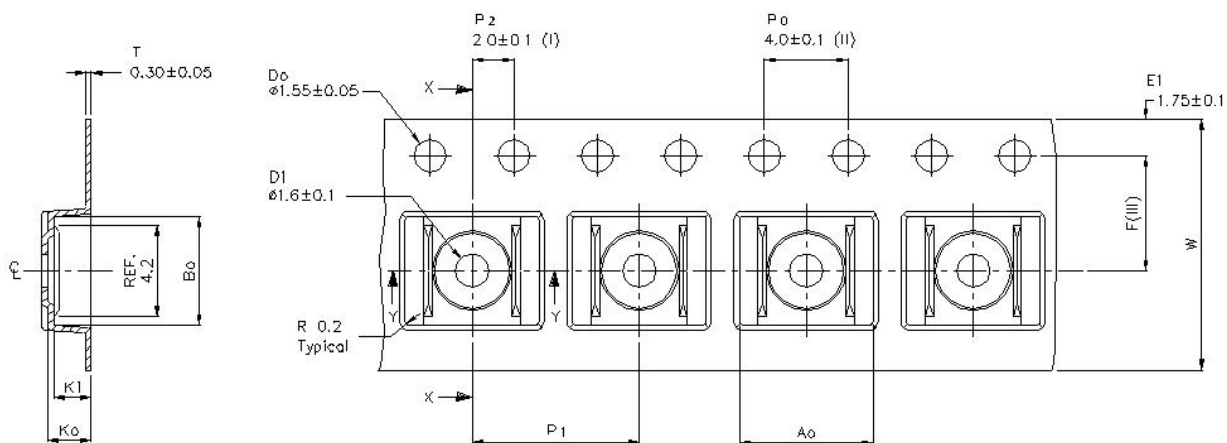
Figure 11.1 Tape/reel digram for SSOP16

Part No.	Package type	A0 (mm)	B0 (mm)	K0 (mm)	K1 (mm)	F (mm)	P1 (mm)	W (mm)
NSC9262_Q0SSR	SSOP16	6.5±0.1	5.3±0.1	2.2±0.1	1.9±0.1	5.5±0.1	8.0±0.1	12.0±0.3

There is no component at the head and the tail of each tape/reel, where the space is 50cm, as shown in the following figure.
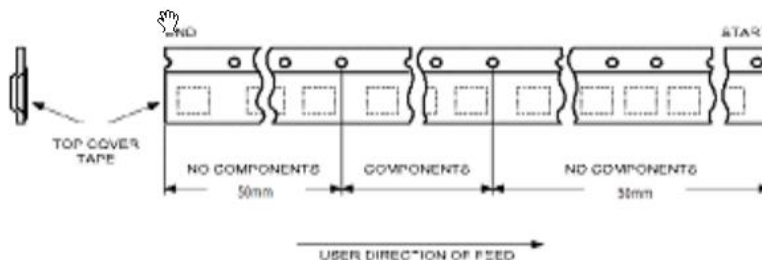
Pin 1 is located at the first quadrant, as shown in the following figure.
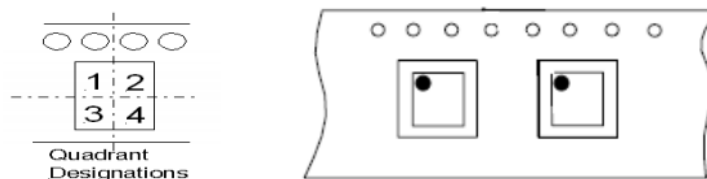
12. Revision History

Revision	Description	Date
0.0	Initial Version	2019/3/18
1.0	First Release	2019/12/13
1.1	Add ESD/EMC description Add list of related documents	2020/2/20
1.2	Add RoHS-compliant information Add document of Calibration Algorithm Introduction	2020/3/23
1.3	Modify the maximum value of over-voltage and reverse voltage protection	2021/7/30
1.4	Modify some English description, change to released document template	2023/09/14

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