

NSD-1202

Dual Piezo Motor Driver IC for SQL Series SQUIGGLE Motors



1 General Description

The NSD-1202 is a dedicated piezo motor driver ASIC capable of driving two SQL Series SQUIGGLE motors from a single 2.8 to 5.5 VDC supply.

The two motors can be controlled independently using a standard I²C interface.

An on-chip DC-DC step-up converter generates the high supply voltage (24 to 40 VDC) required by the piezoelectric elements of the SQUIGGLE motor.

Four half bridge drivers create pairs of phase-shifted square waves with ultrasonic frequency as required to drive SQL Series SQUIGGLE motors.

2 Key Features

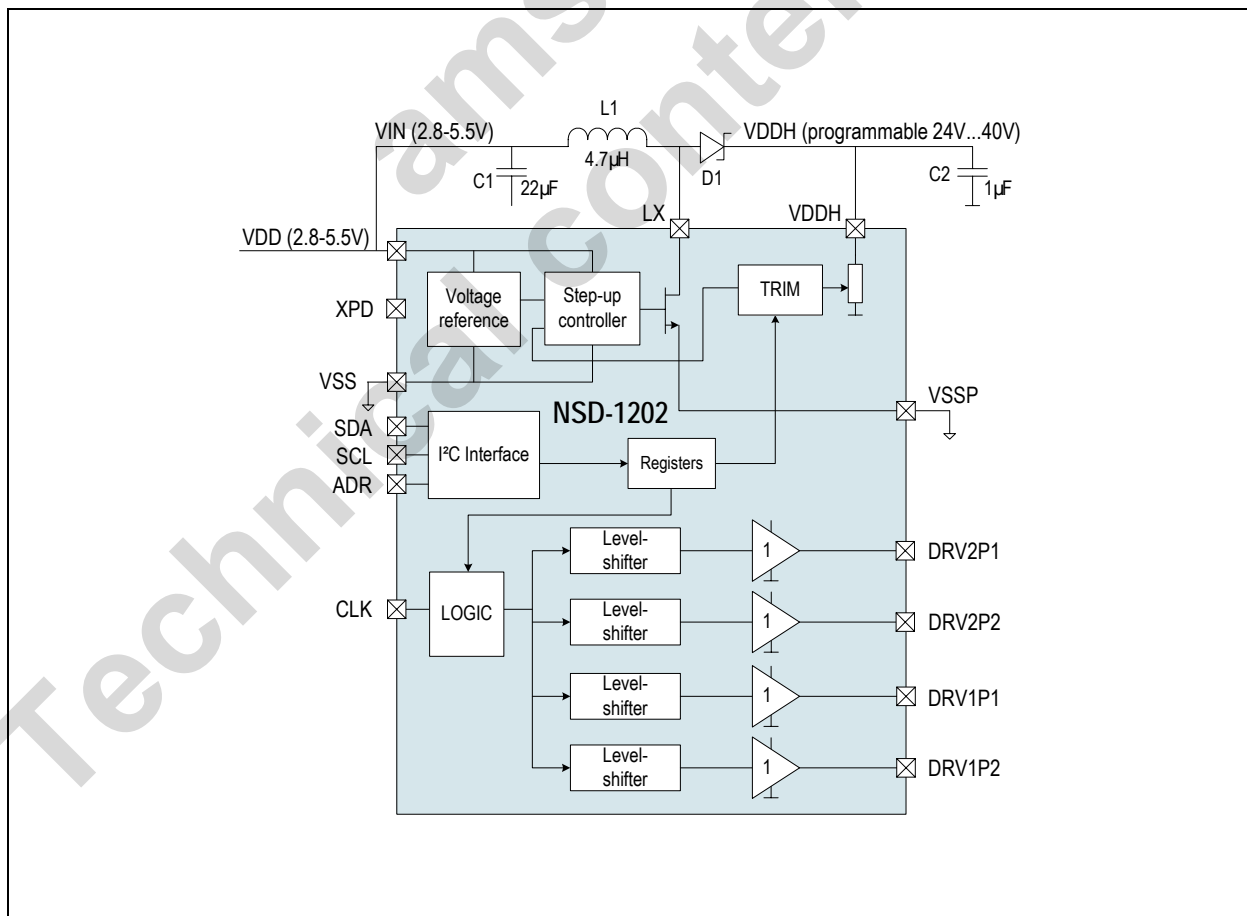
- Wide Input Supply Voltage Range: 2.8 to 5.5VDC
- Step-up converter to generate programmable high-voltage power supply (24 to 40V)
- Minimum 65% efficiency (at VDD=2.8V, I_{OUT}=25mA, freq=2MHz)
- 4x output driver with defined rise/fall time
- I²C interface
- On chip registers store driver instructions
- Power-down mode for minimal power consumption in stand-by
- Small 4x4mm 16-Pin QFN Package

This part supersedes and is backward-compatible with the NSD-1102.

3 Applications

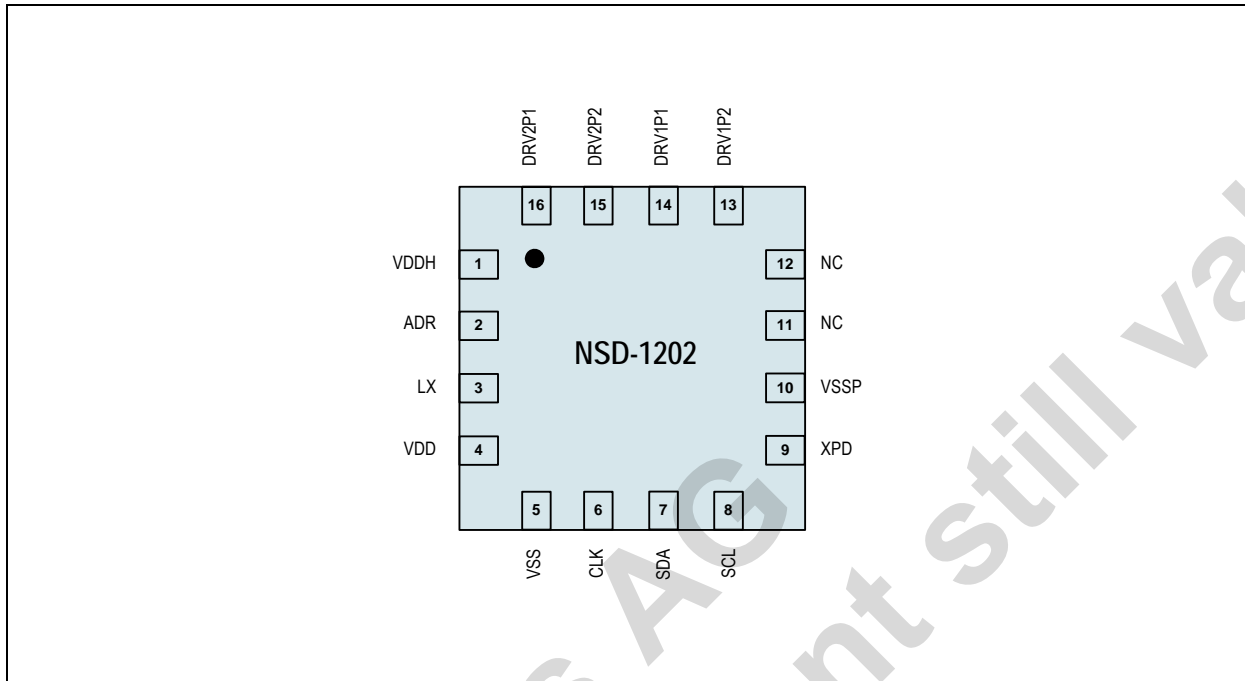
The NSD-1202 is ideal for SQUIGGLE piezoelectric motor driver.

Figure 1. NSD-1202 Functional Block Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Character	Description
VDDH	1	Supply pad	Power	High Voltage Supply
ADR	2	Digital input	Input	Slave address input
LX	3	Analog I/O	Output	Power Output to Inductor
VDD	4	Supply pad	Power	Low Voltage Supply
VSS	5		GND	Signal Ground
CLK	6	Digital input	Input	20MHz Clock input
SDA ¹	7	Digital I/O	BiDir	Data IO
SCL ¹	8			Data clock (400 kHz Max)
XPD	9	Digital input	Input	Power Down, active low
VSSP	10	Supply pad	GND	Power Ground
NC11	11	Digital I/O	BiDir	Test mode pin, connect to VSS
NC12	12			Test IO pin, connect to VSS
DRV1P2	13	Analog I/O	Output	Half Bridge 1 Phase2 Output
DRV1P1	14			Half Bridge 1 Phase 1 Output
DRV2P2	15			Half Bridge 2 Phase2 Output
DRV2P1	16			Half Bridge 2 Phase1 Output

1. SDA (Data IO) and SCL (Data clock) constitute an I²C interface. Both have open drain outputs.

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Comments
V _{VDD}	Voltage at low voltage supply pin	-0.3		7	V	Internal 3.3V supply (VDDA)
V _{VDDH}	Voltage at high voltage supply pin	-0.3		50	V	High voltage supply
V _{LX}	Voltage at LX pin	-0.6		V _{VDDH} +0.3	V	
V _{LV}	Voltage at CLK, SDA, SCL, XPD	-0.3		7	V	Low voltage pads
I _{scr}	Input current (latchup immunity)	-50		50	mA	Norm: Jedec 78
ESD	Electrostatic discharge	±1			kV	Norm: MIL 883 E method 3015 Human body model: R=1.5kΩ, C=100pF
P _{tot}	Total power dissipation			1	W	
R _{thja}	Thermal resistance QFN16 4x4mm	29.7	33	36.3	K/W	
T _{strg}	Storage temperature	-40		150	°C	
T _{body}	Soldering temperature			260	°C	Norm: IPC/JEDEC J-STD-020C. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".
	Humidity non-condensing	5		85	%	

6 Electrical Characteristics

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{VDD}	Voltage at VDD	VDD rise time is between 10μs and 100ms	2.8		5.5	V
V _{VDDH}	Voltage at VDDH	High voltage supply	24		40	V
V _{LX}	Voltage at LX pin		-0.6		V _{VDDH} +0.3	V
V _{VSSP}	Voltage at VSSP	GND reference for step up converter	-0.3		0.3	V
V _{VSS}	Voltage at VSS	GND reference potential	0		0	V
V _{LV}	Voltage at CLK, SDA, SCL, XPD	Low voltage pads	-0.3		5.5	V
T _{AMB}	Ambient temperature		-40		85	°C

6.1 Electrical System Specifications

All system parameters are guaranteed up to 125°C junction temperature unless explicitly mentioned.

Table 4. Electrical System Specifications

Parameter	Conditions	Min	Typ	Max	Units
VDD		2.8	3.3	5.5	V
Ambient temperature		-40		+85	°C
Junction temperature		-40		+125	°C
Stand-by current consumption	XPD=LOW, temp=27°C; No activity on I ² C interface and CLK static			5	μA
Operating current consumption	XPD=HIGH, Step-up converter on but NOT RUNNING A MOTOR		1.5		mA
Output Voltage (VDDH)	Default value is 35V after start-up	24		40	V
Output Voltage (VDDH) steps			0.5		V
Output Voltage accuracy		-6		+6	%
Hysteresis		0.325	0.5	0.675	V
Output current	DC			25	mA
Efficiency	V _{IN} =2.8V, Efficiency calculations assume the use of the components as specified in the Applications Description section (see page 6)	65			%

6.2 DC/AC Characteristics for Digital Inputs and Outputs

Table 5. CMOS Input: XPD, ADR, CLK

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	High level input voltage		1.2		V _{DD}	V
V _{IL}	Low level input voltage		V _{SS}		0.3	V
I _{LEAK}	Input leakage current				1	μA
C _{IN}	Capacitive Load				15	pF

Table 6. CMOS I²C Interface: SDA, SCL

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	High level input voltage		1.2		V _{DD}	V
V _{IL}	Low level input voltage		V _{SS}		0.3	V
I _{LEAK}	Input leakage current				1	μA
V _{OH}	High level output voltage	Depending on external pull-up resistor	V _{VDD} -0.5		V _{VDD}	V
V _{OL}	Low level output voltage	@3mA output current			V _{SS} +0.4	V
CL	Capacitive load: SDA, SCL				50	pF
R _{PU}	External pull-up resistor: SDA, SCL	As defined by I ² C spec	1.2	6.0	7.1	kΩ
SCL	I ² C write frequency	Maximum clock frequency to write data			400	kHz

7 Detailed Description

Figure 1 shows the main building blocks of the system:

- Voltage reference
- Step up converter
- I²C interface
- Registers
- Selectable feedback
- Four (4) half bridge drivers

Supplementary blocks such as biasing or power-on reset are not shown. The step-up converter is built as a hysteretic step-up converter. The half bridge drivers operate rail to rail (VSSP to VDDH). User supplied external components C1, C2, L1 and D1 provide voltage boost and regulation. The output voltage can be programmed via the I²C interface in 0.5V steps between 24V and 40V. This voltage, along with the duty cycle (or pulse width) of the drive signal, determines the speed of the motor.

Registers define the switching frequency of the motor, which can be dynamically adjusted from 140 KHz to 180 KHz for optimum motor performance. Other registers control motor direction and the number of pulses the motor is active (correlating to distance traveled). The XPD input enables a stand-by mode.

7.1 Step Up Converter

The internal switching converter, together with L1 and C2, form a step up DC/DC converter used to create the high level voltage VDDH in the range 24 to 40V. The switch includes an over-current detect circuit to ensure safe operation at all times. The output voltage can be programmed via I²C interface in steps of 0.5V from 24V to 40V. At power up the default output voltage is set to 35V.

7.2 I²C

The I²C interface is used to control the NSD-1202 and set the value of several registers. These registers will define the output voltage (by changing the resistive feedback divider) as well as the direction and duration of the output driver signals. The period count, duty cycle (or pulse width) and pulse count registers can be set separately for each motor.

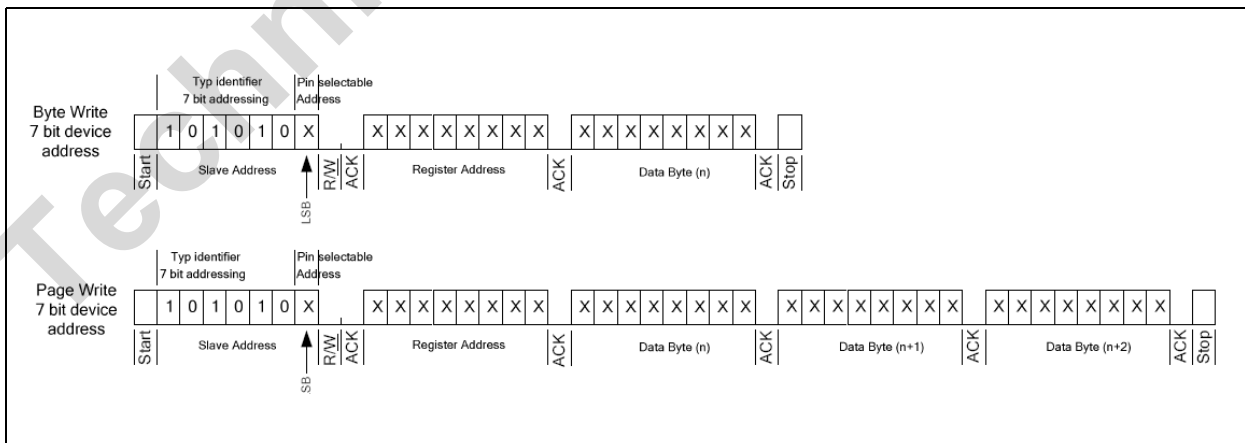
Start/Stop Condition: A HIGH to LOW transition on the SDA line while SCL is HIGH is the start condition for the bus. A LOW to HIGH transition on the SDA line while SCL is HIGH is the stop condition.

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The receiver must pull down the SDA line during the acknowledge clock pulse. The NSD-1202 is a slave device on the bus. There are two different access modes:

- Byte write
- Page write

The device can be addressed using 7-bit addressing. The first 6 bits are fixed. The last bit can be set via package pin. Provision will be made for data collision due to non-synchronization between the external clock and the internally generated clock.



7.3 Register Map

The table below shows the registers which can be addressed over the I²C interface.

Description	Address	Data Byte							
		MSB				LSB			
Period count A	00h	X	X	X	X	X	X	X	X
Pulse count A (high byte) ¹	01h	h	d				X	X	X
Pulse count A (low byte)	02h	X	X	X	X	X	X	X	X
Period count B	03h	X	X	X	X	X	X	X	X
Pulse count B (high byte) ¹	04h	h	d				X	X	X
Pulse count B (low byte)	05h	X	X	X	X	X	X	X	X
Output voltage	06h			X	X	X	X	X	X
Duty cycle A	07h	X	X	X	X	X	X	X	X
Duty cycle B	08h	X	X	X	X	X	X	X	X
Reserved register	10h	X	X	X	X	X	X	X	X

1. The master clock doubling bit ('h') of both registers 01h and 04h must set in order for the doubling to take affect (even if only driving one motor). Do not use clock doubling if the master clock has a frequency > 10 MHz.

7.4 Output Drivers

The output drivers operate rail to rail and are capable of driving a large capacitive load. In power-down mode the output drivers are pulled to ground. The same applies when the motor is off.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Rise/fall time	CLOAD 600pF	25	100	250	ns
CLOAD	Load capacitance	The load capacitance may be lower than 500pF but the lower the value the shorter the rise time.	500	600	700	pF
	Switching frequency	The accuracy of switching frequency and phase shift will be defined depending on master clock frequency; the given values are for 20MHz master clock. Lower master clock frequencies give higher deviations. For Squiggle applications 20MHz clock is required, 10 MHz can be used with the clock doubling feature.	140	170	180	kHz
	Switching frequency step		0.98	1.45	1.61	kHz
	Switching frequency duty cycle		1		50	%
	Duty cycle accuracy		-1		+1	%
	Phase shift			±90		deg
	Phase shift error					±3
	Master clock frequency (CLK)	Clock doubling feature may be employed when using a 10MHz or less master clock frequency	1	20	20	MHz

7.5 Period Counter

The period counter is used to define the switching frequency of the motor. The pulse period is generated by dividing the clock input frequency by the given period counter value.

The MSB of the high byte of the pulse counter (h) is used to enable the internal frequency doubler. This function should be used only for input clock frequencies of 10MHz or less. At 20MHz input clock a decimal period counter value of 111 gives an output frequency of 180.18 kHz. A period counter value of 112 results in a switching frequency of 178.75 kHz. This is equal to a maximum frequency step of 1.61 kHz. The frequency resolution gets better for lower output frequencies, assuming a fixed input clock frequency.

The following table presents examples of the period counter and output switching frequency relationship. The values are given for 20MHz and 10MHz clock input frequency. (At 10MHz the frequency doubler can be activated, which leads to the same results.)

Period Counter Value	Typ	Unit
0110 1111	180.18	kHz
0111 0000	178.57	kHz
1000 0101	150.37	kHz
1000 0110	149.25	kHz
1000 1110	140.85	kHz
1000 1111	139.86	kHz

7.6 Pulse Counter

The pulse counter sets the number of pulses the motor should be active. Writing all zeros to the pulse counter stops the motor, even if the previous set counter value is not completed. All outputs are then low. The same is valid for power-down mode. Bit 6 of the high byte in the pulse counter (d) is used to set the direction of motor motion.

Pulse Counter Value	Typ	Unit	Conditions
XXXX X000 0000 0000	0	pulses	Motor is off, driver outputs are low
XXXX X100 0000 0000	1024	pulses	
XXXX X111 1111 1111	2047	pulses	Maximum possible number of pulses

7.7 Output Voltage Register

This register is used to define the output voltage of the boost converter. The register value is directly transferred to the analog part. The default value for this register set during power up or power down (XPD = LOW) is equal to 35V nominal output voltage.

Output Voltage Register	Typ	Unit	Conditions
0001 0001	24.0	V	
0001 0010	24.5	V	
0001 1111	31.0	V	
0010 0111	35.0	V	Default value
0011 0000	39.5	V	
0011 0001	40.0	V	

Varying the output voltage can be used to vary the speed of the motor. However, if two motors are being driven, both motors use a common output voltage and therefore one setting applies to both motors. To control the speed of two motors independently, use the Duty Cycle Register.

7.8 Duty Cycle Register

A register is used to define the duty cycle (or pulse width) of the driver output signal for each motor. The register value is directly transferred to the analog part.

Since changing the duty cycle will change the speed of the motor, this register can be used to control the speed of two motors independently. (Motor speed can also be controlled by varying the voltage; however, one setting applies to both motors. See the previous section, Output Voltage Register.)

To provide motor independent speed control, the duty cycle may be adjusted from 50% (max speed) down to ~12% (minimum speed). A lower duty cycle could be used, but may not provide enough vibration amplitude to overcome the load.

The default value for this register set during power up or power down (XPD = LOW) is equal to 00h. In this case the default duty cycle of 50% is generated. The resulting duty cycle and resolution of single steps is depending on the master clock frequency and the switching frequency of the driver output.

In the following table an example for 20MHz clock input and 150kHz driver frequency is given. The value of the duty cycle register should not exceed 50% of the period counter value.

Duty Cycle Register	Min	Typ	Max	Unit
0000 0000		49.6/50.4		%
0000 0001		0.8		%
0000 1101		9.8		%
0001 1011		20.3		%
0010 1000		30.1		%
0011 0101		39.8		%
0100 0010		49.6		%
0100 0011		50.4		%

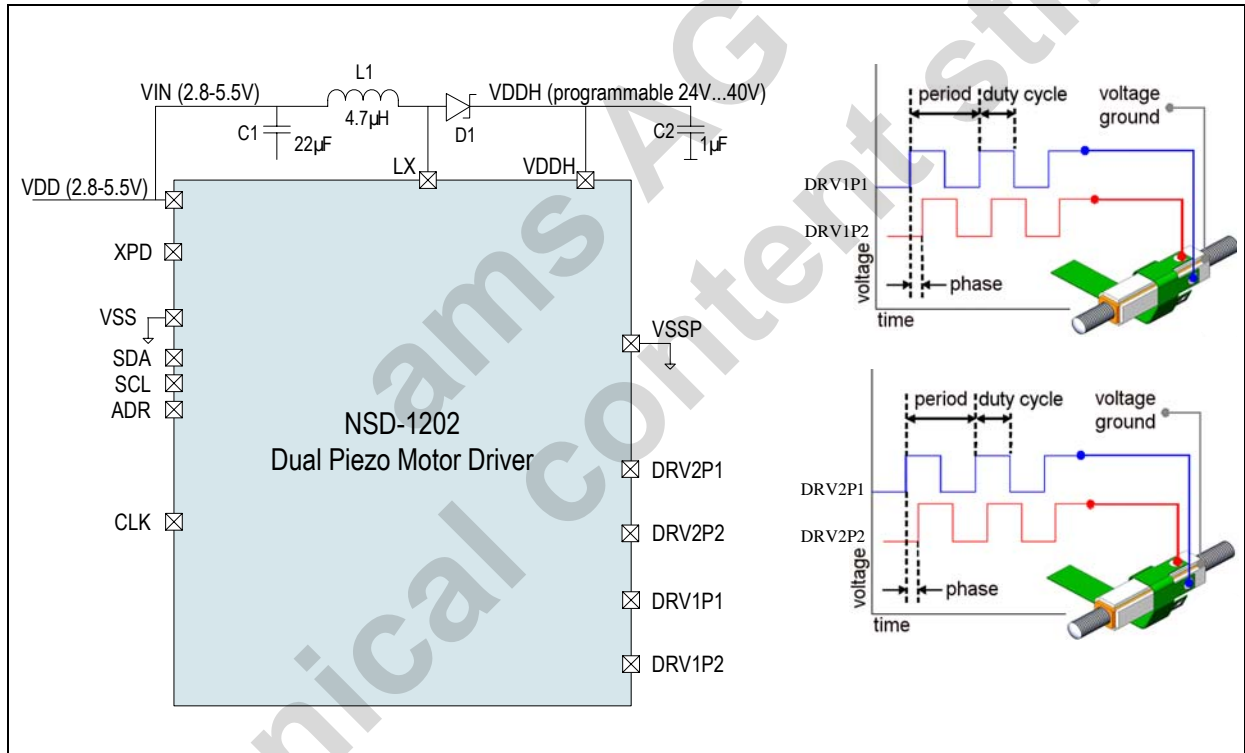
8 Application Information

The NSD-1202 is designed to drive two SQL-1.8 SQUIGGLE motors. Recommended external components are as follows:

Component	Description	Manufacturer	Part Number	WxLxH [mm]
C1	22µF Cap 6.3V	www.murata.com	GRM21BR60J226ME39	1.25x2.0x1.25
C2	1µF Cap 50V		GRM21BR71H105KA12	1.25x2.0x1.25
L1	4.7µH Inductance	www.coilcraft.com	EPL2014-472	2.0x2.0x1.4
D1	Diode	www.nxp.com	PMEG6010CEJ	1.25x2.5x0.80

New Scale offers a convenient MC-33DB evaluation board which includes these components, along with input and motor connectors, to take full advantage of the NSD-1202 ASIC.

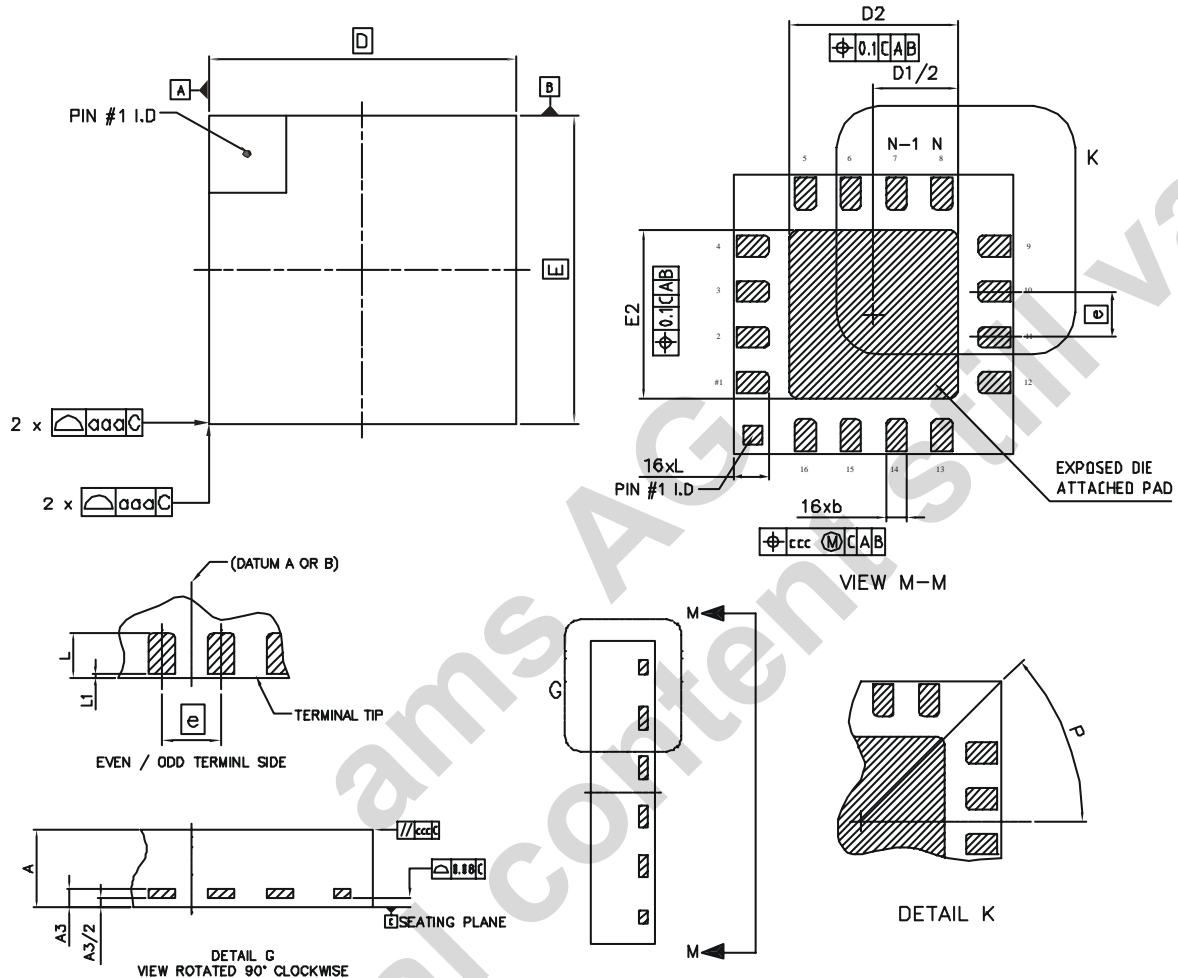
The XPD input can be used to place the ASIC in stand-by mode for minimal current consumption when the motor is not moving. Alternatively, the designer can implement an external switch to power off the ASIC completely when the motor is not moving: the SQUIGGLE motor holds its position with the power off.



9 Package Drawings and Markings

The devices are available in a 16LD QFN (4x4mm) package.

Figure 3. 16LD QFN (4x4mm) Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.75	0.85	0.95
A1	0.203 REF		
b	0.25	0.30	0.35
D	4.00 BSC		
E	4.00 BSC		
D2	2.30	2.40	2.50
E2	2.30	2.40	2.50

Symbol	Min	Nom	Max
e	0.65 BSC		
L	0.40	0.50	0.60
L1	0.10		
P	45° BSC		
aaa	0.15		
ccc	0.10		

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

10 Ordering Information

The devices are available as the standard products shown in [Table 7](#).

Table 7. Ordering Information

Ordering Code	Description	Delivery Form	Package
NSD-1202BQFT	Dual Piezo Motor Driver IC	Tape & Reel	QFN-16 (4x4mm)

Note: All products are RoHS compliant and Pb-free.

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