NOVOSENSE

NSD12430A-Q1
2CH, 300mΩ, 40V, Fully Protected Automotive Low-side Switch
Datasheet (EN) 1.0

Product Overview

NSD12430A-Q1 is a 300mΩ 2 channel low-side switch with 48V clamp voltage for automotive applications, compatible with 3.3V MCU and 5V MCU. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnose function is built to indicate any faults when thermal shutdown through an open-drain status output pin. This device operates in ambient temperatures from –40°C to 125°C.

Applications

- Automotive Relays
- Valves
- Solenoid drivers
- Lighting

Normal MAX DC load current

Part Number	T_a	*Load current* (1)
NSD12430A-Q1SPR	85°C	0.76A
	105°C	0.57A

(1) Based on the JEDEC standard high-K profile, JESD 51-7, four-layer board

Device Information

Part Number	*Package*	*Body Size*
NSD12430A-Q1SPR	SO-8	4.9mm x 3.9mm

Key Features

- AEC-Q100 Grade 1 Qualified
- Compatible with 3.3V MCU and 5V MCU
- Drain current limitation: 4.2A (V_{DD}=5V) / 4A(V_{DD}=3.3V)
- 48V over-voltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block
  - Thermal shutdown diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection
- RoHS & REACH Compliance

Typical Application

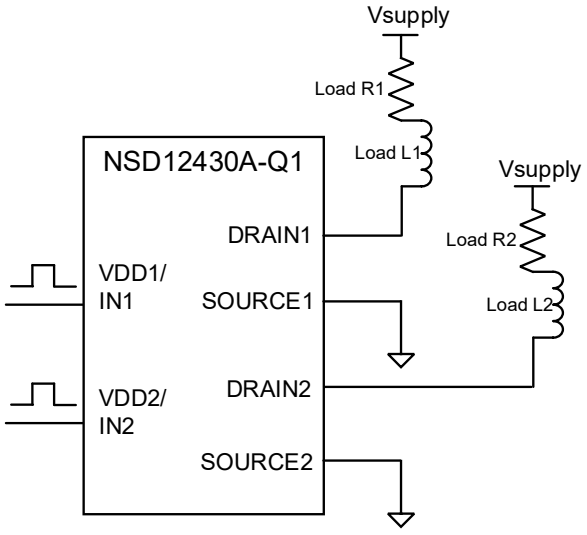

Figure 0.1 NSD12430A-Q1 Typical Application

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1. Pin Configuration and Functions

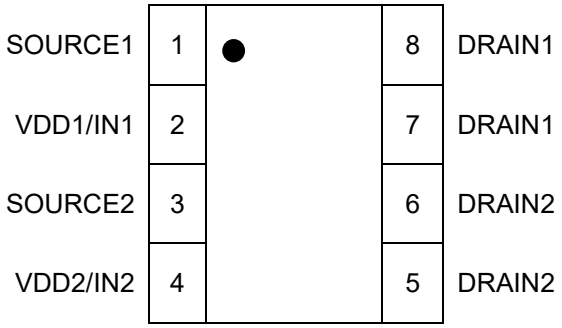


Figure 1.1 NSD12430A-Q1SPR Pin out

Table 1.1 NSD12430A-Q1SPR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1,3	SOURCE1,2	PowerMOS source and ground reference for the control section
2,4	VDD1,2/IN1,2	Voltage controlled input pin with hysteresis, CMOS compatible. They control output switch state
8,7,6,5	DRAIN1,2	PowerMOS drain

2. Block diagram

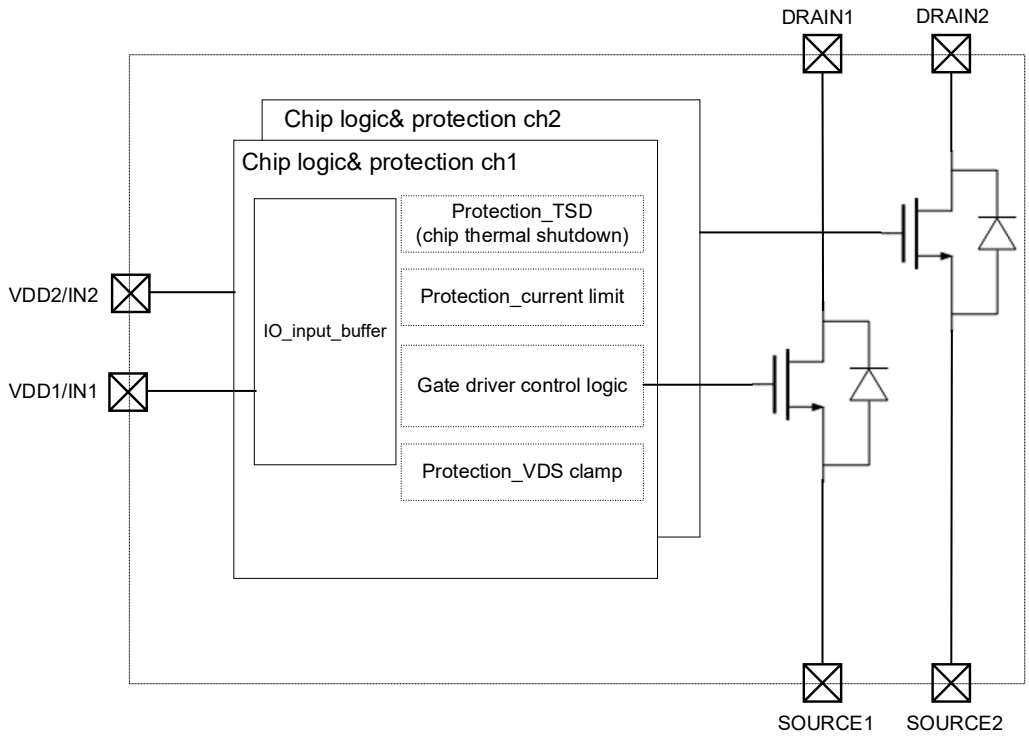


Figure 2.1 NSD12430A-Q1SPR Block diagram

3. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Drain-to-Source Voltage	V_{DS}			Internally clamped	V
DC Drain Current	I_D			Thermal limited	A
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C
Single pulse avalanche energy (L = 15mH; T_J = 150 °C; R_L = 0; I_{OUT} = 3A)	E_{AS}			26	mJ

4. ESD ratings

Parameters	Symbol	Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model, per AEC-Q100-002-RevD ， $V_{ESD-HBM}$	±4000	V
	Charged-device model, per AEC-Q100-011-RevB ， $V_{ESD-CDM}$	±750	V

5. Thermal Information

Parameters	Symbol	SO-8	Unit
Junction-to-ambient Thermal Resistance	θ_{JA}	80.5	°C/W
Junction-to-top characterization parameter	ψ_{JT}	3.75	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC\ (top)}$	35.5	°C/W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layers board.

6. Specifications

6.1. Electrical Characteristics

(V_{DD} = V_{IN}= 4.5 V to 5.5 V, T_J=-40°C to 150°C. Unless otherwise noted.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power MOSFET						
ON-state resistance	R_{ON}		270		mΩ	I_D = 0.8 A; T_J = 25°C; V_{DD} = V_{IN} = 5 V
				540	mΩ	I_D = 0.8 A; T_J = 150°C; V_{DD} = V_{IN} = 5 V
			300		mΩ	I_D = 0.8 A; T_J = 25°C; V_{DD} = V_{IN} = 3.3 V
				600	mΩ	I_D = 0.8 A; T_J = 150°C; V_{DD} = V_{IN} = 3.3 V
Drain-source clamp voltage	V_{CLAMP}	43	48	53	V	V_{IN} = 0 V, I_D = 0.8 A
Drain-source clamp threshold voltage	V_{CLTH}	36			V	V_{IN} = 0 V, I_D = 2 mA
OFF-state output current	I_{DSS}	0		3	μA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 25°C
		0		5	μA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 125°C
Body diode forward voltage	V_{BD}		0.8		V	I_D = 0.8 A; V_{IN} = 0 V
VDD/Input section						
Supply current from VDD/input pin	I_{ISS}		30	65	μA	ON-state; V_{DD}=V_{IN} = 5 V; V_{DS} = 0 V
VDD/input clamp voltage	V_{ICL}	5.5		8	V	I_{ICL} = 1 mA
			-0.7			I_{ICL} = -1 mA
Input threshold voltage	V_{INTH}	1		3	V	V_{DS} = V_{IN}; I_D = 1 mA
Status indicator						
Status low output voltage	V_{STAT}			0.5	V	I_{STAT} = 1 mA
Status leakage current	I_{LSTAT}			10	μA	V_{STAT} = 5 V
Status pin input capacitance (1)	C_{STAT}			100	pF	V_{STAT} = 5 V
Status clamp voltage	V_{STCL}	5.5		8	V	I_{STAT} = 1 mA
			-0.7			I_{STAT} = - 1 mA
Switching characteristics						
Turn-on delay time	$t_{d\ (ON)}$		6		μs	R_L = 16 Ω, V_{CC} = 13 V
Turn-off delay time	$t_{d\ (OFF)}$		13		μs	R_L = 16 Ω, V_{CC} = 13 V
Rise time	t_r		3		μs	R_L = 16 Ω, V_{CC} = 13 V

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Fall time	t_f		8		μs	R_L = 16 Ω, V_{CC} = 13 V
Switching energy losses at turn-on	W_{ON}		6		μJ	R_L = 16 Ω, V_{CC} = 13 V
Switching energy losses at turn-off	W_{OFF}		28		μJ	R_L = 16 Ω, V_{CC} = 13 V
Protection and diagnostics						
DC short-circuit current	I_{lim}	3	4.2	5.5	A	V_{DS} = 13 V, V_{DD} = V_{IN} = 5 V
			4		A	V_{DS} = 13 V, V_{DD} = V_{IN} = 3.3 V
Shutdown temperature	T_{TSD}	150	175	200	°C	
Reset temperature (1)	T_R	T_{RS} + 1	T_{RS} + 5		°C	
Thermal reset of STATUS (1)	T_{RS}	135			°C	
Thermal hysteresis (T_{TSD} - T_R)	T_{HYST}		7		°C	
Dynamic temperature (1)	ΔT_J		40		°C	T_J = -40°C, V_{CC} = 13 V
Dynamic temperature hysteresis (1)	$\Delta T_{J(HYS)}$		15		°C	

(1) Not subject to production test, specified by design.

6.2. Typical Performance Curves (1)

（Unless otherwise specified，T_J =25℃，V_{in}=5 V）

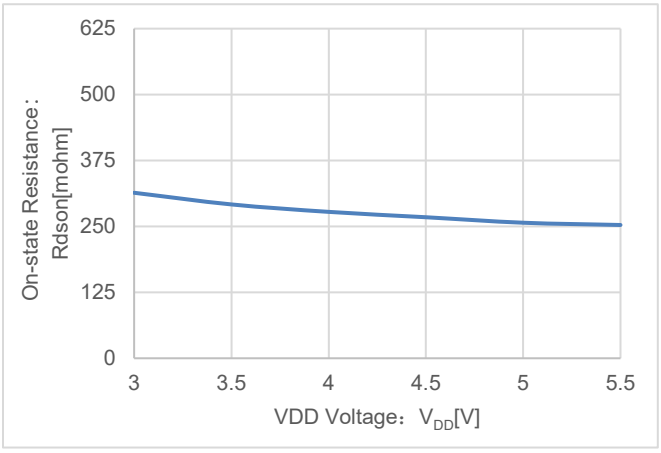


Figure 6.1. On-state Resistance vs VDD Voltage

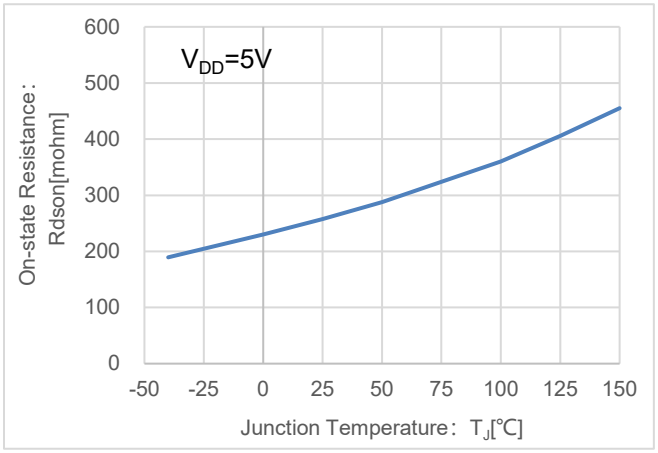


Figure 6.2. On-state Resistance vs Junction Temperature

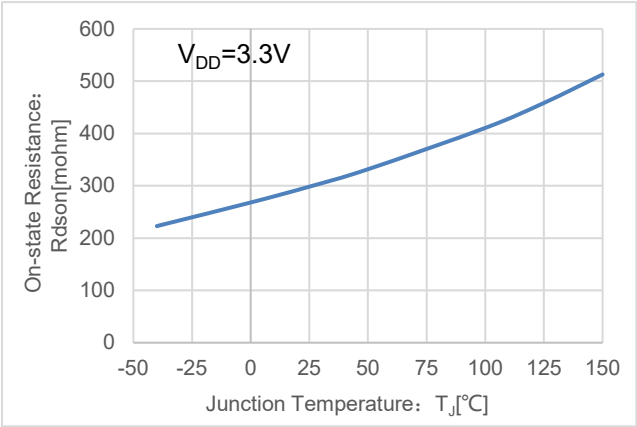


Figure 6.3. On-state Resistance vs Junction Temperature

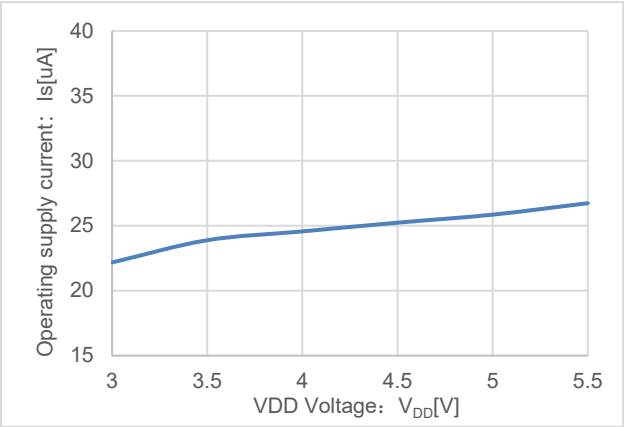


Figure 6.4.VDD Operating supply Current vs VDD Voltage

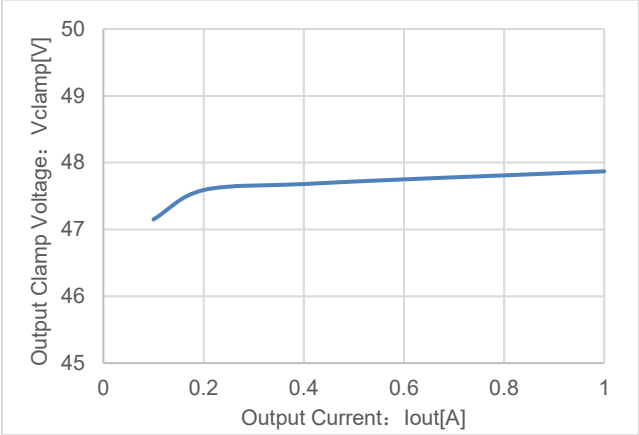


Figure 6.5. Output Clamp Voltage vs Output Current

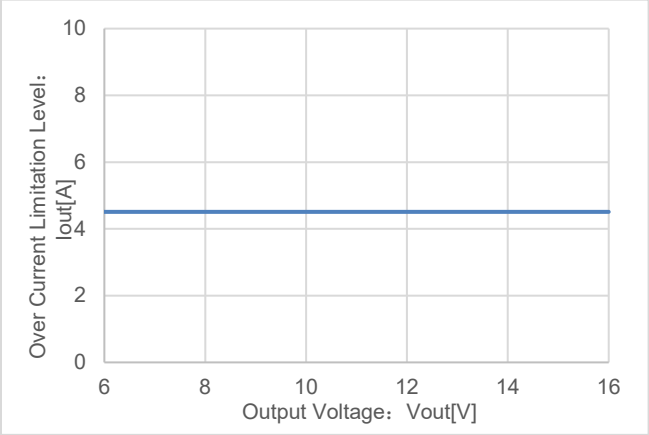


Figure 6.6. Over Current Limitation Level vs Output Voltage

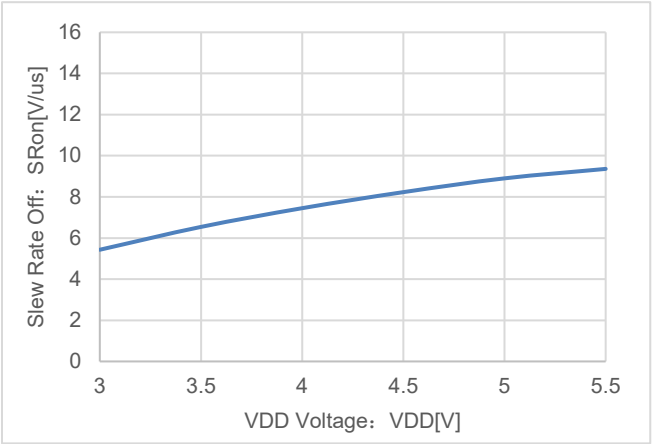


Figure 6.7. Slew Rate Off vs VDD Voltage

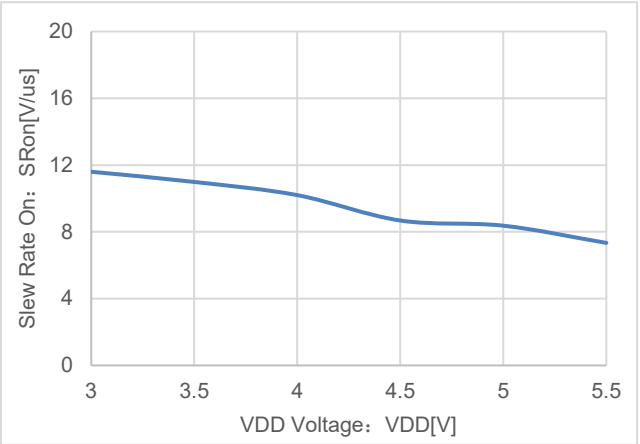


Figure 6.8. Slew Rate On vs VDD Voltage

(1) Not subject to production test, specified by design.

6.3. Switching characteristics

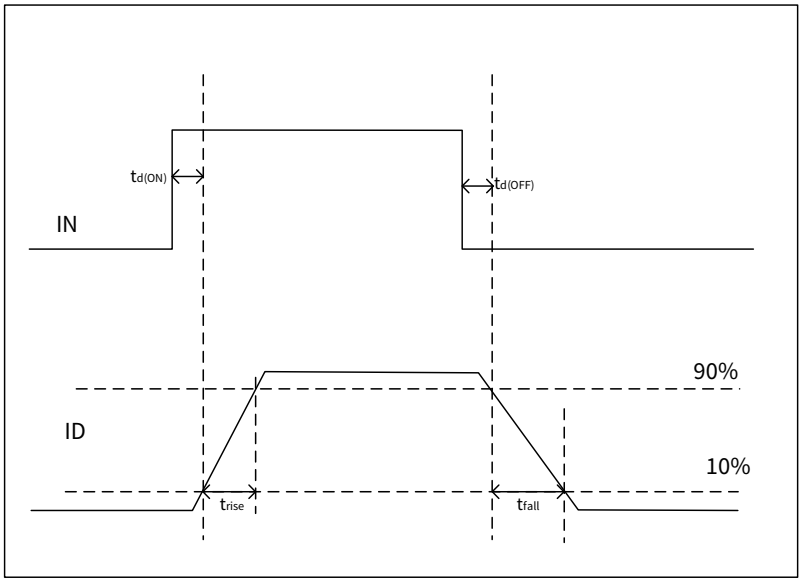


Figure 6.9 NSD12430A-Q1 Switching Characteristics

7. Protections

7.1. Current Limitation

NSD12430A-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to battery.

7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shut down the MOSFET when the hottest junction temperature exceeds the T_{TSD}, and the dynamic temperature protection is also to shut down the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔT_J.

8. Application information

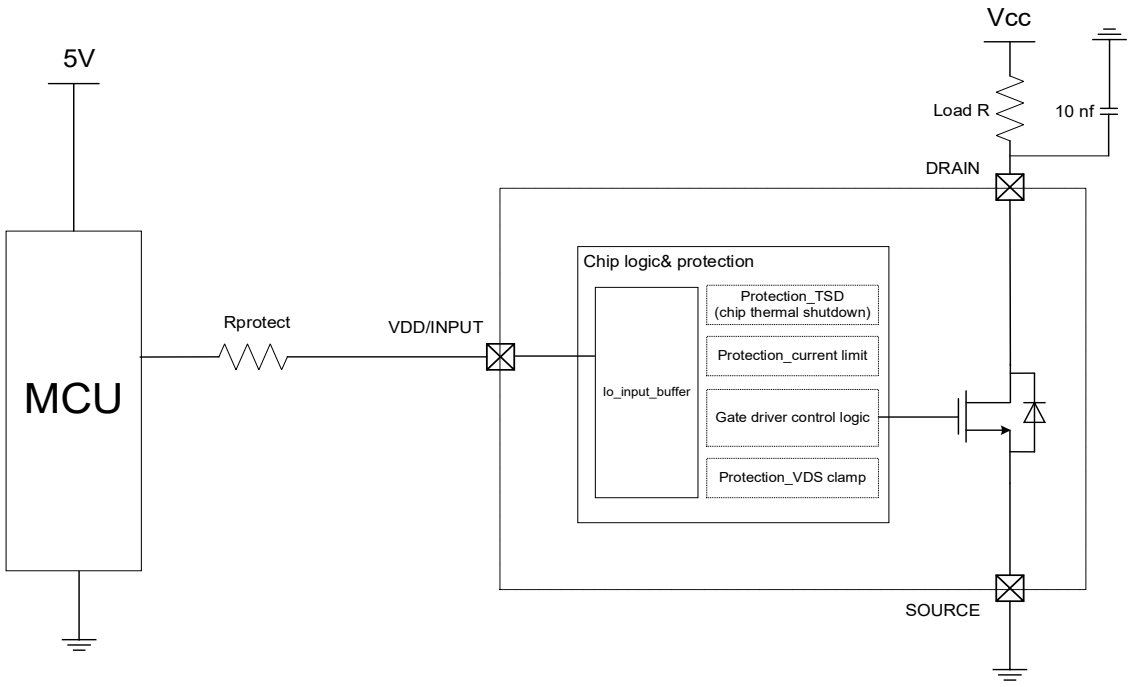


Figure 8.1 NSD12430A-Q1SPR application schematic

8.1. MCU I/O protection

NSD12430A has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection R_{prot} is suggested 100ohm~1. 5kohm.

8.2. Inductive load operation

If the load side of the chip is connected to a pure inductive load, at the moment the channel is switched off, the inductive load will generate a reverse electromotive force, then the chip's activate clamp circuit will clamp the voltage on the drain side at V_{CLAMP}. The current will slowly drop, and the energy generated during this period will be the E_{AS}.

The specific operation schematic is shown in Figure 8.2. E_{AS} is calculated as follows:

$$E_{AS} = \frac{1}{2} \cdot I_L^2 \cdot L \cdot \frac{V_{\text{clamp}}}{V_{clamp} - V_{bat}}$$

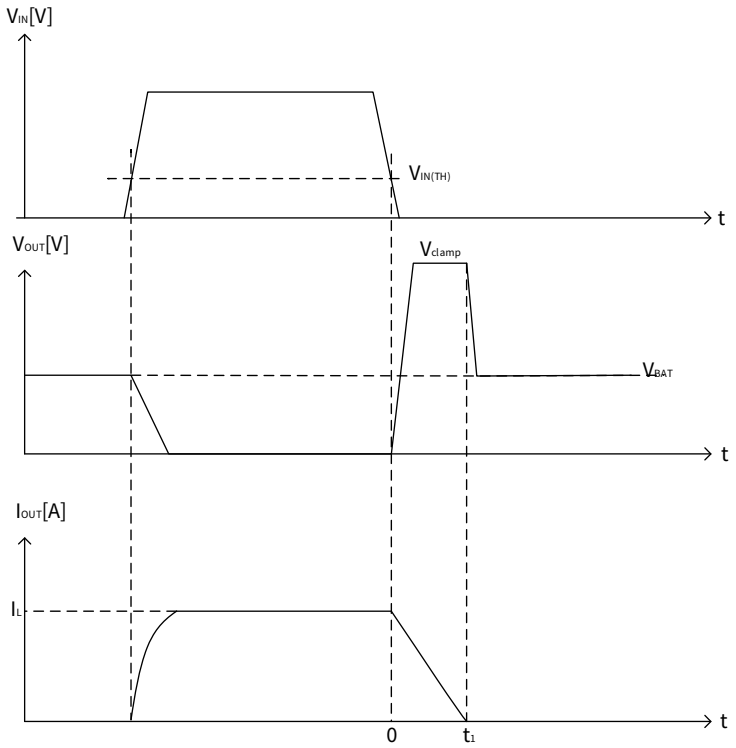
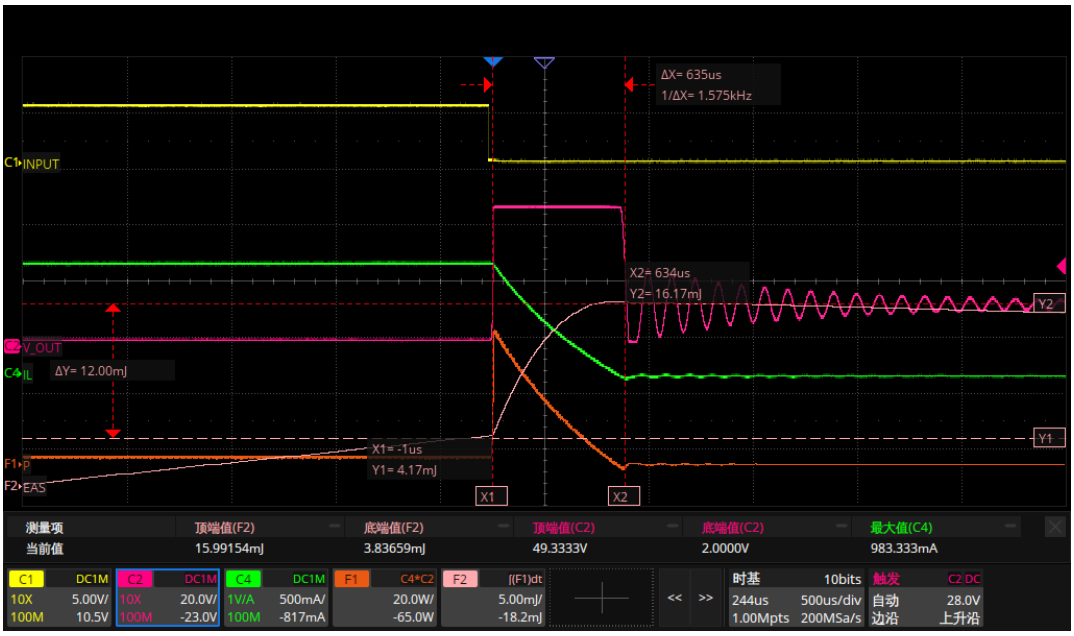


Figure 8.2 LSD Inductive load operation

In practical applications, the loads are not purely inductive and will contain resistance. So, the actual clamping energy calculation is shown in Figure 8.3.

$$E_{AS} = \int (V_{OUT} * I_L)dt = \int (C2 * C4)dt$$

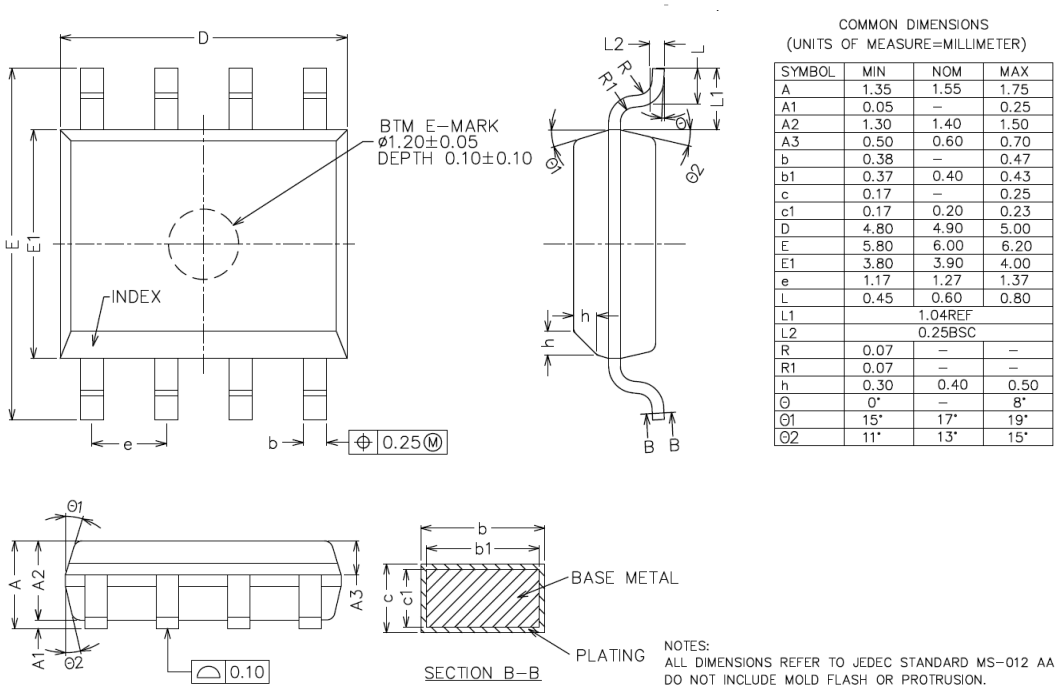


*where C1: INPUT C2: VOUT C4: IL F1: P=C2*C4 F2: EAS*

Figure 8.3 LSD Clamped energy actual test waveform

9. Package Information

9.1. SO-8 package information

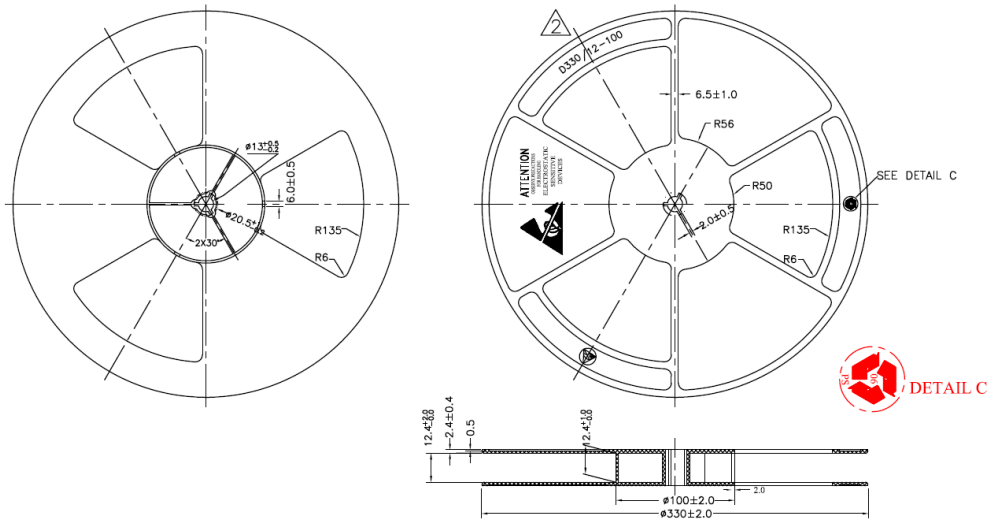


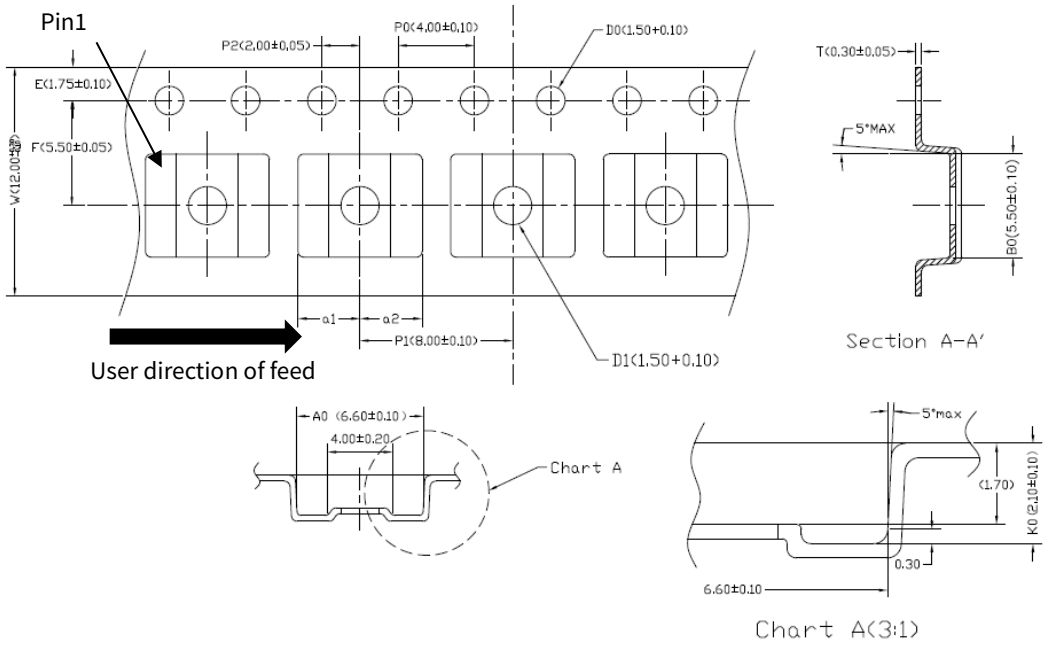
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

9.2. SO-8 packaging information




Pin1
P2(2.00±0.05)
P0(4.00±0.10)
D0(1.50+0.10)
E(1.75±0.10)
F(5.50±0.05)
W(12.00±0.30)
a1
a2
P1(8.00±0.10)
D1(1.50+0.10)
User direction of feed
T(0.30±0.05)
5°MAX
B0(5.50±0.10)
Section A-A'
A0 (6.60±0.10)
4.00±0.20
Chart A
5°max
(1.70)
K0 (2.10±0.10)
0.30
6.60±0.10
Chart A(3:1)

10. Ordering Information

Part Number	Package	MSL	Automotive	SPQ
NSD12430A-Q1SPR	SO-8	3	Yes	2500
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.				

11. Revision History

Revision	Description	Date
1.0	Initial version	2025/2/28

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