

NSF65R280C

N-channel 650V Super Junction MOSFET

Description

NSF65R280C is a N-channel power MOSFET designed according to super junction technology. This device has very low on-resistance and hard ruggedness for switching applications. It's very low conduction loss and fast switching can make applications more efficient and faster.

Features

- Low gate charge
- Low $R_{DS(on)}$ per chip area(Low FOM)
- Very low switching and conduction loss
- Extremely high commutation ruggedness

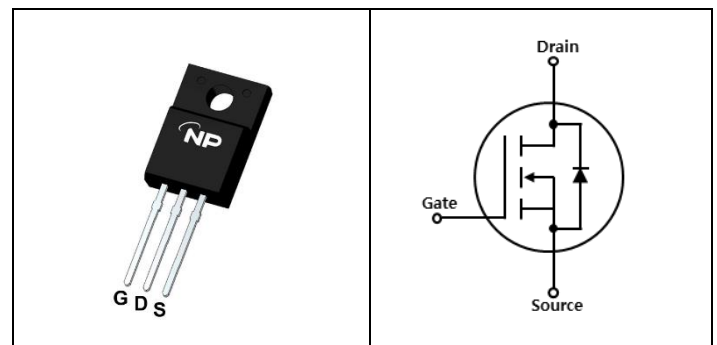
Applications

- TV and PC Power
- Adofter and Lighting
- Telecom and UPS(Uninterruptible Power Supply)

Key parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$Q_{g,typ}$	23	nC
I_D	13.8	A
$R_{DS(on),max}$	0.28	Ω

Package & Internal circuit



Ordering Information

Ordering Code	Package	Marking	Packing type
NSF65R280C	TO-220F	65R280C	Tube

Absolute maximum ratings at $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Unit	Test condition
V_{DS}	Drain-source voltage	650	V	-
V_{GS}	Gate-source voltage	± 30	V	-
$I_D^{(1)}$	Continuous drain current	13.8	A	$T_C = 25^\circ\text{C}$
	Continuous drain current	8.7	A	$T_C = 100^\circ\text{C}$
$I_{DM}^{(2)}$	Pulsed drain current	41	A	$T_C = 25^\circ\text{C}$
E_{AS}	Single pulsed avalanche energy	290	mJ	Starting $T_j = 25^\circ\text{C}$, $I_{AS} = 2.0\text{A}$, $V_{DD} = 50\text{V}$, $I_D = I_{AR}$
P_{tot}	Total power dissipation	32	W	$T_C = 25^\circ\text{C}$
dv/dt	MOSFET dv/dt ruggedness	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
dv/dt	Reverse diode dv/dt	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $T_j = 25^\circ\text{C}$, $I_{SD} \leq I_D$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$	-
T_j	Operating junction temperature	-55 to 150	$^\circ\text{C}$	-

1. limited by $T_{j,max}$

2. Pulse width limited by $T_{j,max}$

Thermal characteristics

Symbol	Parameter	Value	Unit	Test condition
R_{thJC}	Thermal resistance, junction - case	3.9	$^\circ\text{C/W}$	-
R_{thJA}	Thermal resistance, junction - ambient	80	$^\circ\text{C/W}$	-

Static characteristics at $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Maximum value			Unit	Test condition
		Min.	Typ.	Max.		
$V_{(BR)DSS}$	Drain-source breakdown voltage	650	-	-	V	$V_{GS} = 0\text{V}$, $I_D = 0.25\text{mA}$
$V_{GS(th)}$	Gate threshold voltage	2	-	4	V	$V_{GS} = V_{DS}$, $I_D = 0.25\text{mA}$
I_{GSS}	Gate-body leakage current	-	-	100	nA	$V_{GS} = \pm 30\text{V}$, $T_j = 25^\circ\text{C}$
I_{DSS}	Zero gate voltage drain current	-	-	1	uA	$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 25^\circ\text{C}$
		-	-	100		$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 150^\circ\text{C}$
$R_{DS(on)}$	Drain-source on-resistance		0.25	0.28	Ω	$V_{GS} = 10\text{V}$, $I_D = 4.4\text{A}$

Dynamic characteristics

Symbol	Parameter	Values			Unit	Test condition
		Min.	Typ.	Max.		
C _{iss}	Input capacitance	-	1020	-	pF	V _{DS} = 50V, V _{GS} = 0V, f = 400kHz
C _{oss}	Output capacitance	-	79	-	pF	
C _{rss}	Reverse transfer capacitance	-	1.2	-	pF	
t _{d(on)}	Turn-on delay time	-	19	-	ns	V _{DD} = 325V, I _D = 13.8A, V _{GS} = 10V, R _G = 25Ω
t _r	Rise time	-	34	-	ns	
t _{d(off)}	Turn-off delay time	-	76	-	ns	
t _f	Fall time	-	27	-	ns	
R _G	Gate resistance	-	3.2	-	Ω	f = 1MHz, I _D = 0A(open drain)
Q _g	Total gate charge	-	23	-	nC	V _{DS} = 520V, V _{GS} = 10V, I _D = 13.8A
Q _{gs}	Gate-source charge	-	5	-	nC	
Q _{gd}	Gate-drain charge	-	9	-	nC	

Reverse diode characteristics

Symbol	Parameter	Values			Unit	Test condition
		Min.	Typ.	Max.		
V _{SD}	Diode forward voltage	-	-	1.4	V	V _{GS} = 0V, I _{SD} = 13.8A, T _j = 25°C
t _{rr}	Reverse recovery time	-	299	-	ns	I _{SD} = 13.8A, V _{DD} = 100V, di/dt = 100A/μs
I _{rr}	Reverse recovery current	-	24	-	A	
Q _{rr}	Reverse recovery charge	-	3.6	-	μC	

Characteristic Graph

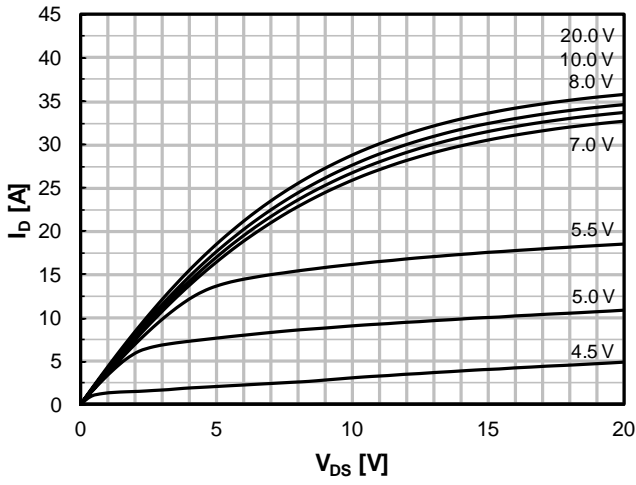


Fig. 1 Output Characteristics

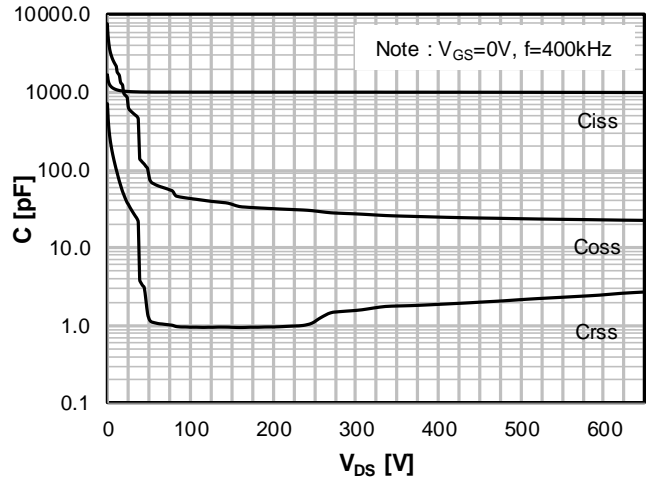


Fig. 2 Capacitances

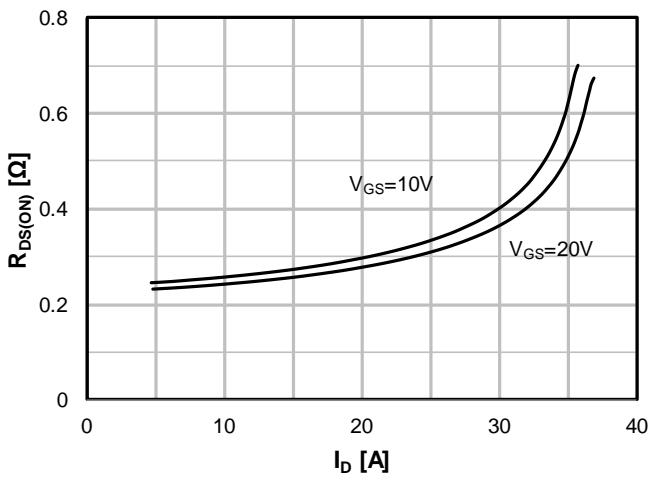


Fig. 3 On-state Resistance

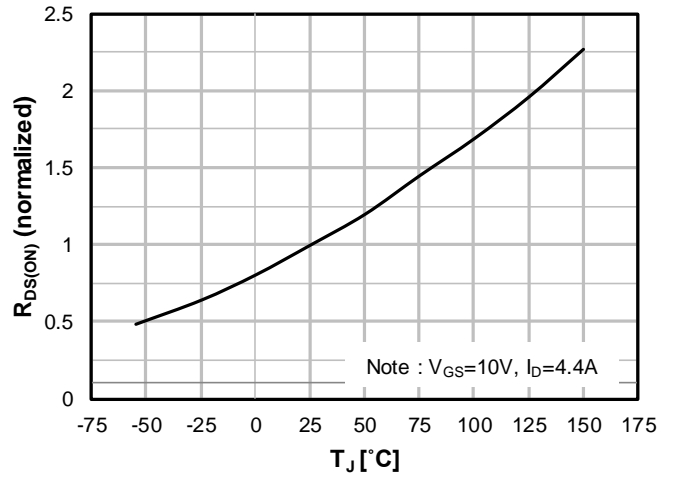


Fig. 4 On-state Resistance with Temperature

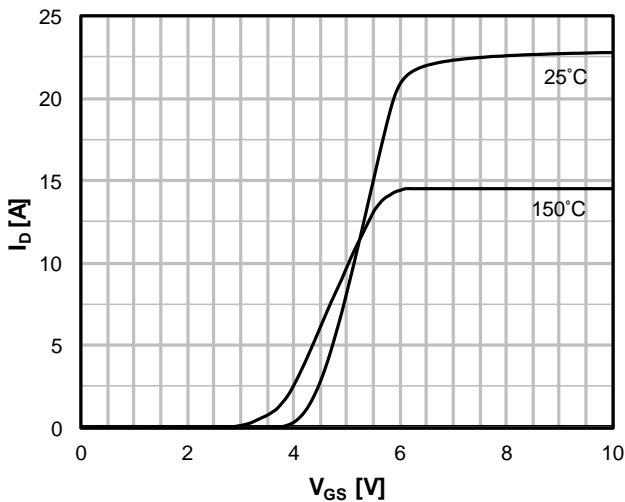


Fig. 5. Transfer Characteristics

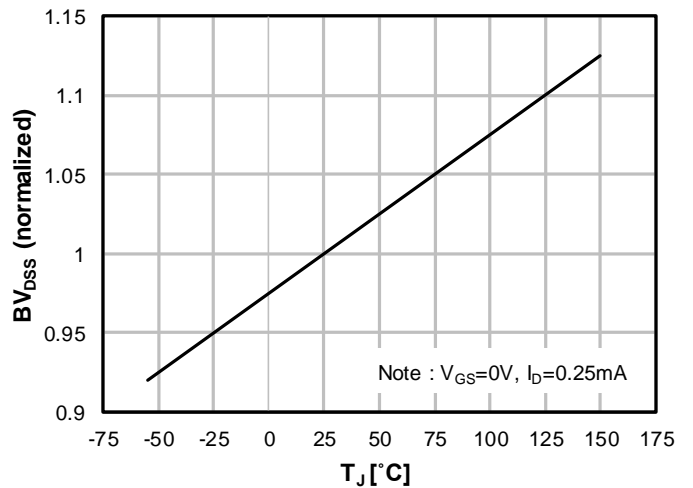


Fig. 6. Breakdown Voltage with Temperature

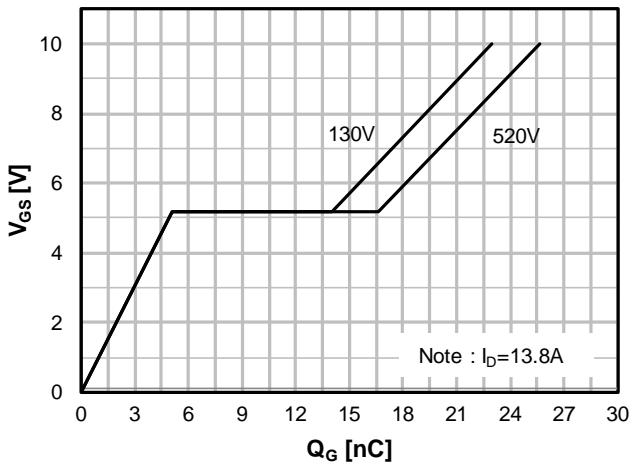


Fig 7. Gate Charge

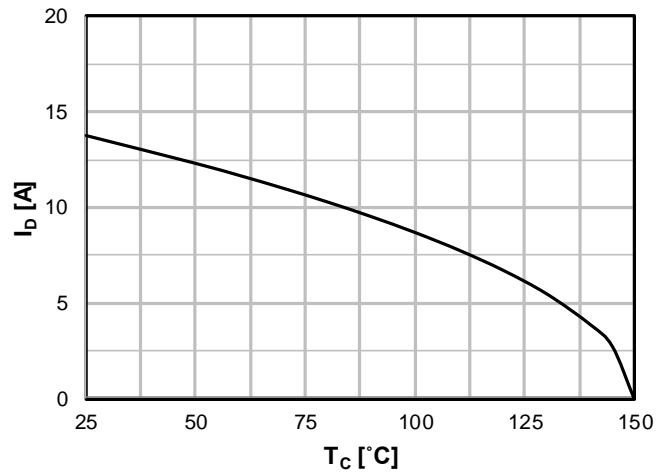


Fig 8. Maximum Drain Current

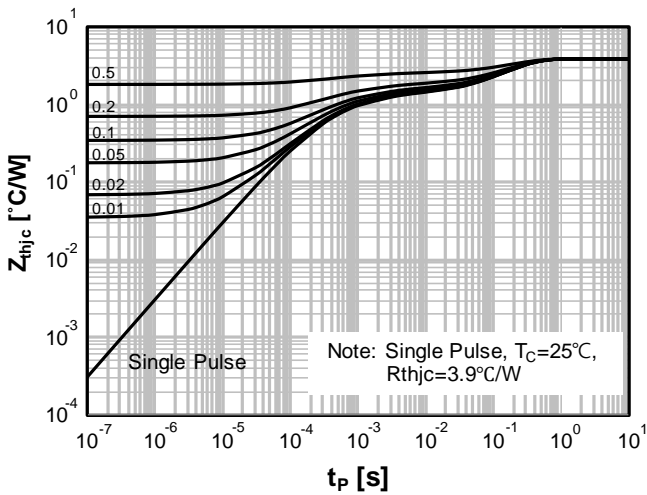


Fig 9. Maximum Transient Thermal Characteristics

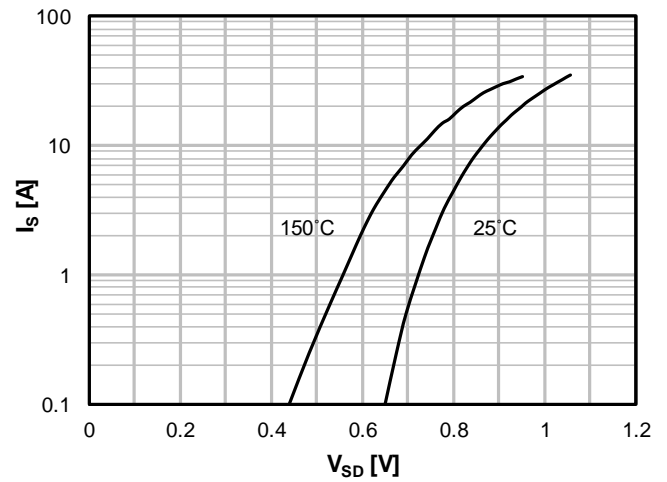


Fig 10. Body Diode Characteristics

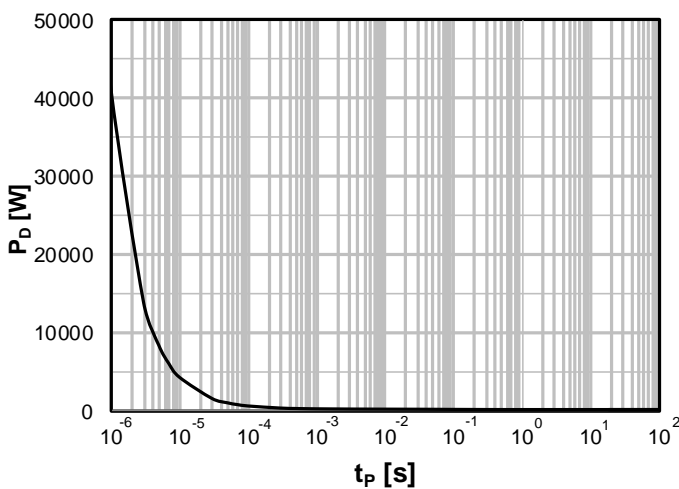


Fig 11. Power Dissipation

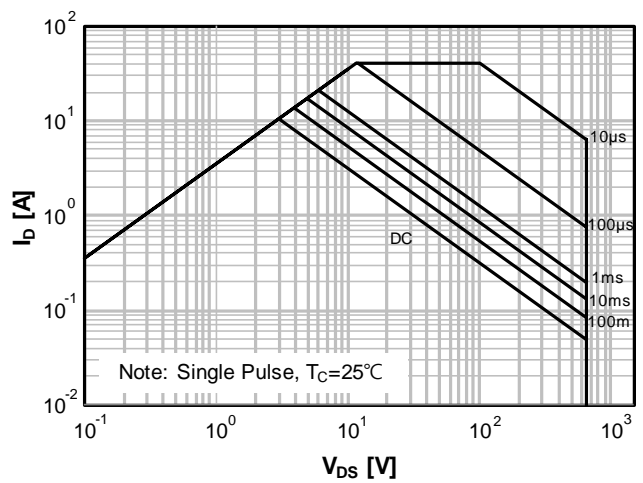


Fig 12. Safe Operating Area

Test Circuits

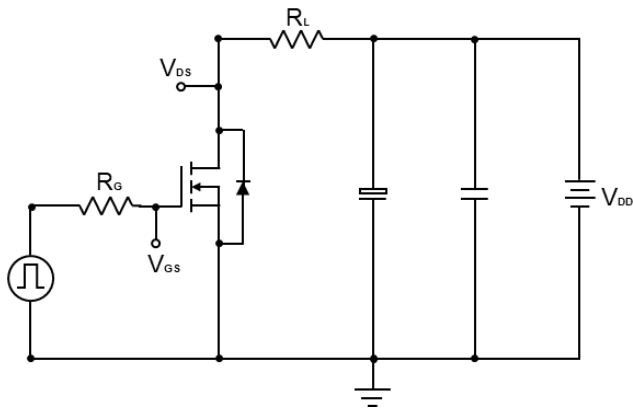


Fig 13. Test circuit for resistive load switching times

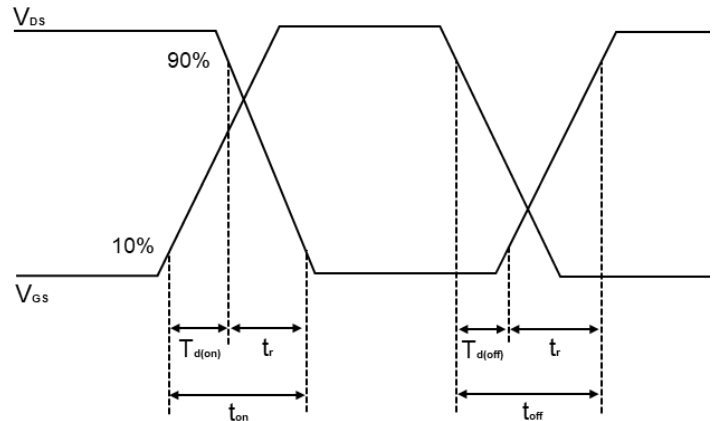


Fig 14. Switching times waveform

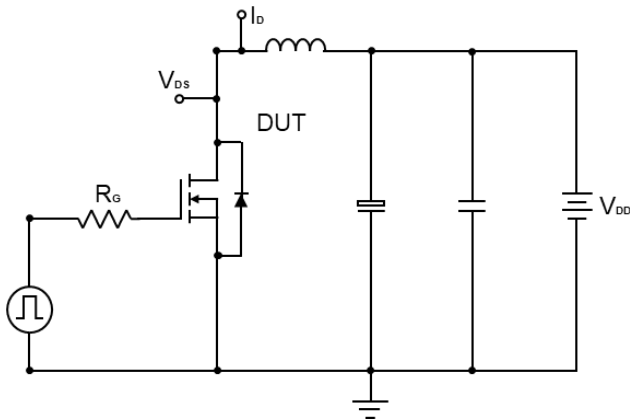


Fig 15. Test circuit for unclamped inductive load

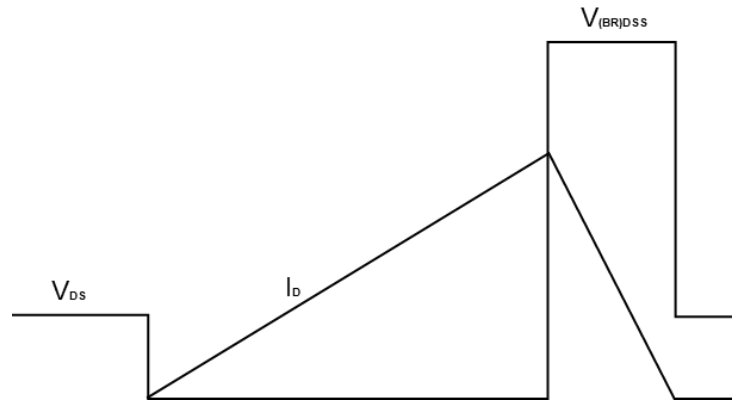


Fig 16. Unclamped inductive waveform

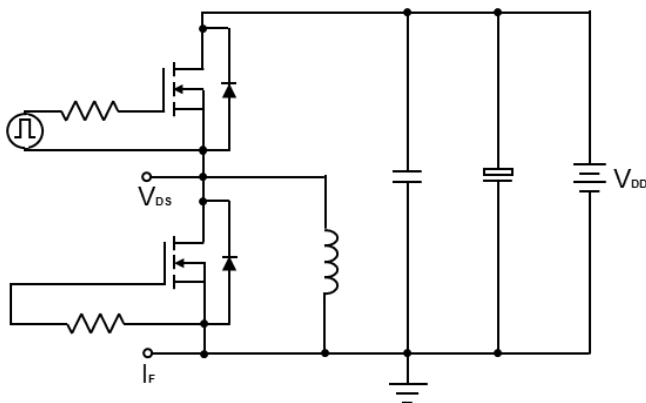


Fig 17. Test circuit for diode

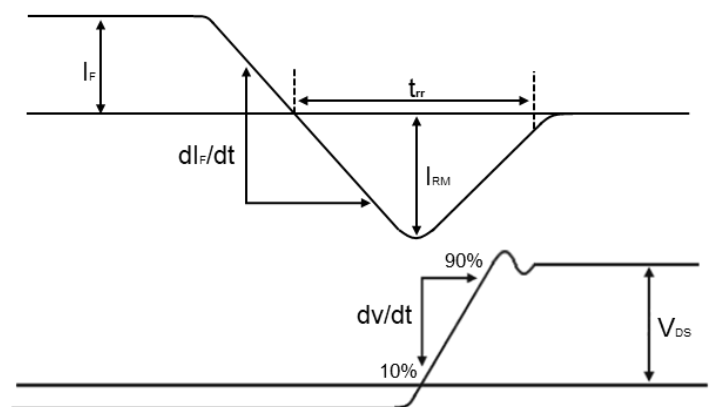
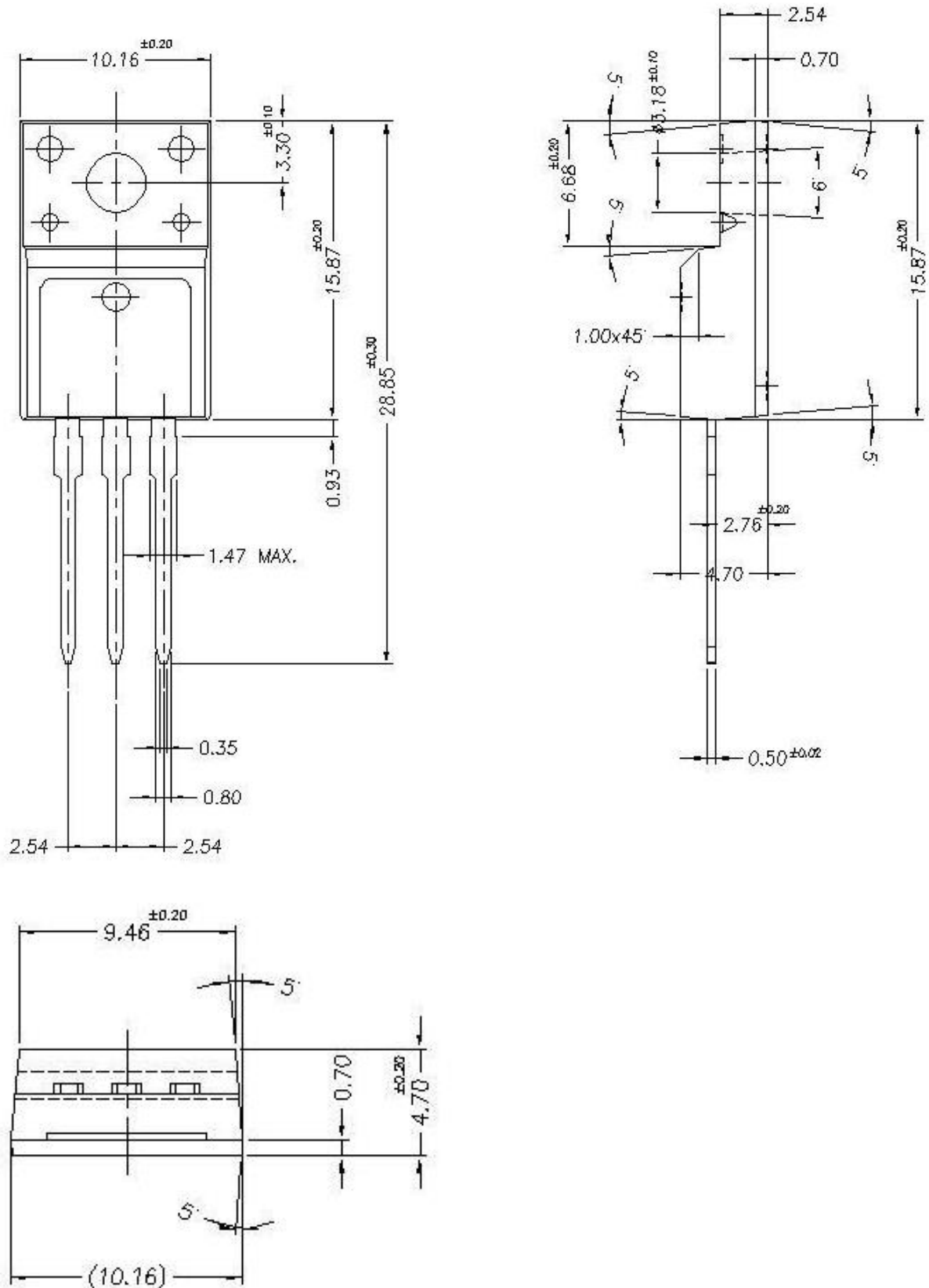


Fig 18. Diode recovery

Package Information

TO-220F Package Outline



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