NOVOSENSE

NSI6602M

High Reliability Isolated Dual-Channel With Miller Clamp Gate Driver

Datasheet 1.0

Product Overview

NSI6602M is a family of high reliability isolated dual-channel gate driver ICs which can be designed to drive power transistor up to 2MHz switching frequency. It can source and sink 5A peak current and has an integrated active Miller Clamp circuit with the same current rating to prevent false turn on caused by Miller current.

The NSI6602M provides 5000Vrms isolation in SOW18 wide package. System robustness is supported by typical ±150V/ns (min. ±100V/ns) common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 32V, while the input-side accepts from 2.7V to 5.5V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

With all these excellent features, NSI6602M is suitable for high reliability, power density and efficiency switching power system.

Key Features

- Isolated dual-channel driver
- Input side supply voltage: 2.7V to 5.5V
- Driver side supply voltage: up to 28V with UVLO
- Typical 5A peak source and Typical 5A peak sink output
- Typical 5A Miller Clamp
- Typical High CMTI: ±150kV/us
- Typical 80ns typical propagation delay
- Max 25ns pulse width distortion
- Programmable deadtime
- Max 60ns minimum input pulse width
- Operation temperature: -40°C ~125°C
- RoHS & REACH Compliance

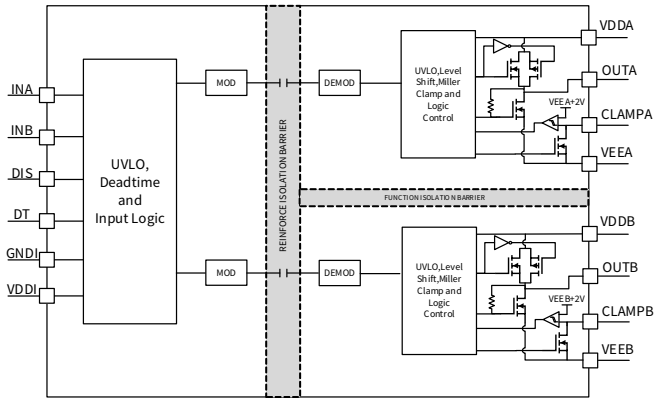
Safety Regulatory Approvals

- UL recognition:
  - SOW18: 5700V_{rms} for 1 minute per UL1577
- DIN VDE V 0884-17:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

Applications

- Isolated DC-DC and AC-to-DC power supplies in server, telecom and industry
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

Functional Block Diagram



NSI6602M Block Diagram

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1. Pin Configuration and Functions

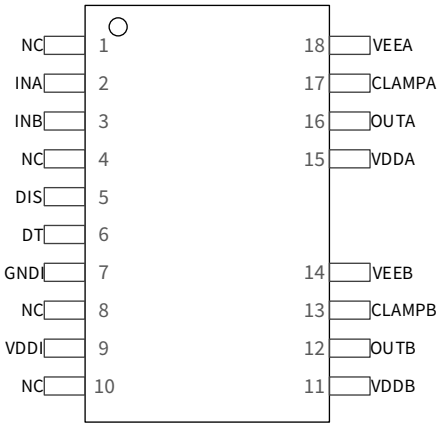


Figure 1.1 NSI6602M SOW18 Package

Table 1.1 NSI6602M Pin Configuration and Description

PIN NO. *SOW18*	*SYMBOL*	*FUNCTION*
2	INA	TTL compatible input signal for channel A with internal pull down to GND. It is recommended to connect this pin to GNDI if not used.
3	INB	TTL compatible input signal for channel B with internal pull down to GND. It is recommended to connect this pin to GNDI if not used.
5	DISABLE	Disables the isolator inputs and driver outputs if asserted high, enables if asserted low or left open. It is recommended to connect this pin to GNDI if not used.
6	DT	Programmable deadtime. Connect DT to VDDI allows the outputs to overlap. Place a 1kΩ to 200kΩ resistor (R_{DT}) between DT and GNDI to adjusts deadtime following: t_{DT} (ns) = 10 x R_{DT} (kΩ). It is recommended to parallel a low ESR capacitor, e.g. 2.2nF or above.
7	GNDI	Input-side ground reference.
9	VDDI	Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GNDI as close as possible.
11	VDDB	Positive output supply rail of channel B
12	OUTB	Gate Driver Output of channel B
13	CLAMPB	Active Miller-Clamp input of channel B
14	VEEB	Driver-side ground reference of channel B
15	VDDA	Positive output supply rail of channel A
16	OUTA	Gate Driver Output of channel A
17	CLAMPA	Active Miller-Clamp input of channel A
18	VEEB	Driver-side ground reference of channel A
1, 4, 8, 10	NC	Not connected

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI - GNDI	-0.3	6	V
Output Side Supply Voltage	VDDA - VEEA, VDDB - VEEB	-0.3	35	V
Input Signal Voltage	INA, INB, DIS, DT - GNDI	-0.3	V_{VDDI}+0.3	V
	INA, INB, DIS, DT - GNDI, Transient for 50ns	-5	V_{VDDI}+0.3	V
Output Signal Voltage	OUTA - VEEA, OUTB - VEEB	-0.3	V_{VDDA}+0.3 V_{VDDB}+0.3	V
	OUTA - VEEA, OUTB - VEEB, Transient for 200ns	-2	V_{VDDA}+0.3 V_{VDDB}+0.3	V
Channel A to Channel B Voltage	VEEA to VEEB		1850	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI - GNDI	2.7	5.5	V
Driver Side Supply Voltage	VDDA - VEEA, VDDB – VEEB (NSI6602MB)	10.5	32	V
Driver Side Supply Voltage	VDDA - VEEA, VDDB – VEEB (NSI6602MC)	13.5	32	V
Input Signal Voltage	INA, INB, DIS, DT -GNDI	0	V_{VDDI}	V
Ambient Temperature	T_a	-40	125	°C

5. Thermal Information

Parameters	Symbol	Typical	Unit
Junction-to-ambient thermal resistance[1)]	R_{JA}	97.0	°C/W
Junction-to-case(top) thermal resistance[2)]	$R_{JC(top)}$	23.3	°C/W
Junction-to-top characterization parameter[3)]	Ψ_{JT}	35.8	°C/W
Junction-to-board characterization parameter[3)]	Ψ_{JB}	39.0	°C/W

1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.

2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.

3) Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V for NSI6602MB/C, Ta=-40°C to 125°C. Unless otherwise noted, typical values are at Ta=25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Side Supply						
VDDI Quiescent Current	I_{VDDIQ}		0.75	2	mA	INA=0, INB=0
VDDI Operation Current	I_{VDDI}		1.8		mA	Input frequency 500kHz, $C_{OUTA/B}$=100pF
VDDI UVLO Rising Threshold	V_{VDDI_ON}	2.35	2.55	2.75	V	
VDDI UVLO Falling Threshold	V_{VDDI_OFF}	2.15	2.35	2.55	V	
VDDI UVLO Hysteresis	V_{VDDI_HYS}		0.2		V	
Output Side Supply						
VDDA/B Quiescent Current, per Channel	I_{VDDAQ}, I_{VDDBQ}		1.6	3	mA	VDDA/B=15V
VDDA/B Operation Current, per Channel	I_{VDDA}, I_{VDDB}		3.2		mA	Input frequency 500kHz, Cload=100pF, VDDA/B=15V
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}		9.2	10	V	NSI6602MB (9V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	8	8.5		V	
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		0.7		V	
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}		12.2	13	V	NSI6602MC (12V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	10.3	11.2		V	
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		1		V	

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Side Characteristic						
Input Pin Pull Down Resistance, INA, INB	R_{INA_PD}, R_{INB_PD}		100		kΩ	
Input Pin Pull Down Resistance, DIS	R_{DIS_PD}		100		kΩ	
Logic High Input Threshold	V_{INA_H}, V_{INB_H}, V_{DIS_H}		1.7	2	V	
Logic Low Input Threshold	V_{INA_L}, V_{INB_L}, V_{DIS_L}	0.8	1.1		V	
Input Hysteresis	V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}		0.6		V	
Output Side Characteristic						
Logic High Output Voltage	V_{VDDA} - V_{OUTA_H}, V_{VDDB}-V_{OUTB_H}		150	300	mV	$I_{OUTA, OUTB}$=-50mA, $V_{INA,INB}$=High
Logic Low Output Voltage	V_{OUTA_L} – V_{VEEA}, V_{OUTB_L}– V_{VEEB}		30	65	mV	$I_{OUTA, OUTB}$=-50mA, $V_{INA,INB}$=LOW
Output Sink Resistance	R_{OUTA_L}, R_{OUTB_L}		0.6		Ω	$I_{OUTA, OUTB}$ = 50mA
Output Source Resistance	R_{OUTA_H}, R_{OUTB_H}		3		Ω	$I_{OUTA, OUTB}$ = -50mA
Peak Output Sink Current	I_{OUTAH}, I_{OUTBH}		5		A	$V_{INA, INB}$=Low, pulse width<10us
Peak Output Source Current	I_{OUTAL}, I_{OUTBL}		5		A	$V_{INA, INB}$=High, pulse width<10us
Active Miller Clamp						
Low Level Clamp Voltage	$V_{CLAMPA,CLAMPB}$		60	110	mV	$I_{CLAMPA,CLAMPB}$=100mA, $V_{INA,INB}$=Low, refer to VEEA, VEEB
Clamp Low-level Current	$I_{CLAMPA, CLAMPB}$		5		A	
Clamp Threshold Voltage	$V_{CLAMPA\_TH, CLAMPB\_TH}$		2.1	2.5	V	refer to VEEA, VEEB
Clamp Delay - Falling	T_{AMC_DLY}		46		ns	
Short Circuit Clamping						
VOUT Short Circuit Clamping Voltage	V_{CLP_OUT}		1	1.5	V	$V_{INA,INB}$=Low, $I_{OUTA,OUTB}$=0.5A, pulse width<=10us, refer to VDDA, VDDB
VCLAMP Short Circuit Clamping Voltage	V_{CLP_CLAMP}		1.2	1.8	V	$V_{INA, INB}$=Low, $I_{OUTA, OUTB}$=0.5A, pulse width<=10us, refer to VDDA, VDDB
			0.7	1	V	$V_{INA,INB}$=High, $I_{CLAMPA,CLAMPB}$=20mA, refer to VDDA, VDDB
Active Pull Down						
Active Pulldown Voltage on CLAMP	V_{ACTPD}		2.5		V	VDDI, VDDA/B=OPEN, $I_{CLAMPA, CLAMPB}$=500mA

6.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V for NSI6602MB/C, Ta=-40°C to 125°C. Unless otherwise noted, typical values are at Ta=25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width	t_{PWmin}		30	60	ns	
Propagation Delay	t_{PDHL}, t_{PDLH}	50	80	110	ns	Cload=100pF
Pulse Width Distortion $\lvert t_{PDLH}-t_{PDHL}\rvert$	t_{PWD}		2	25	ns	Cload=100pF
Channel to Channel Delay Matching	t_{DMLH}, t_{DMHL}			10	ns	
Programmed Deadtime	t_{DT}	160	200	240	ns	t_{DT}(ns)=10*R(kΩ); Test for R = 20kΩ
Output Rise Time (20% to 80%)	t_R		15		ns	$C_{OUTA/B}$=1.8nF
Output Fall Time (80% to 20%)	t_F		15		ns	$C_{OUTA/B}$=1.8nF
Shutdown Time from Disable True	t_{DIS}		70	110	ns	
Recovery Time from Disable False	t_{EN}		70	110	ns	
VDDI Power-up Time Delay (Time from VDDI = VDDI_ON to OUTA/B = INA/B)	t_{start_VDDI}		8.5	15	us	INA or INB tied to VDDI
VDDA,VDDB Power-up Time Delay (Time from VDDA, VDDB = VDDA_ON, VDDB_ON to OUTA/B = INA/B)	t_{start_VDDA}, t_{start_VDDB}		50	80	us	INA or INB tied to VDDI; $C_{OUTA/B}$=1.8nF
Common Mode Transient Immunity	CMTI	100	150		V/ns	verified by design

6.3. Typical Performance Characteristics

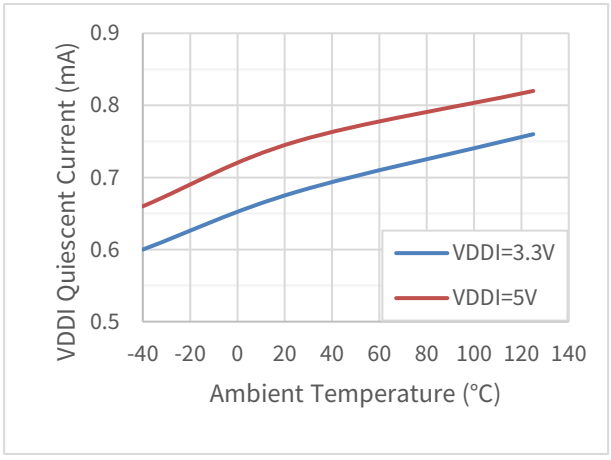


Figure 6.1 VDDI Quiescent Current vs Temperature

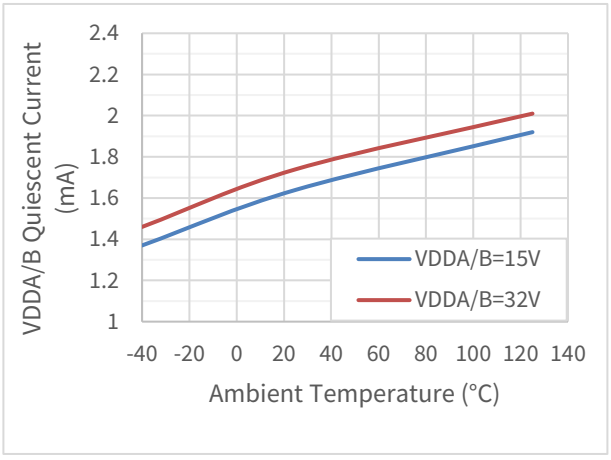


Figure 6.2 VDDA/B Quiescent Current vs Temperature

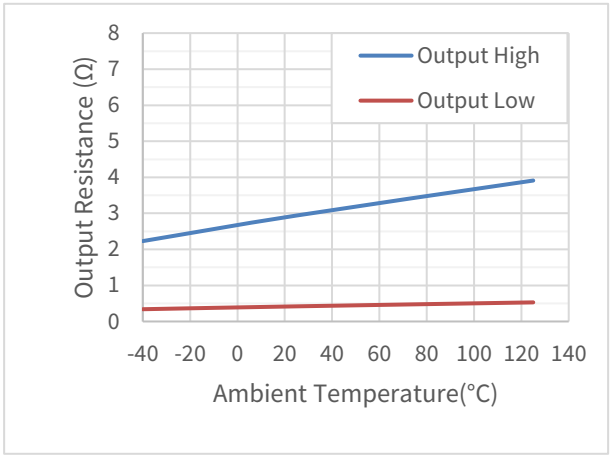


Figure 6.3 Output Resistance vs Temperature

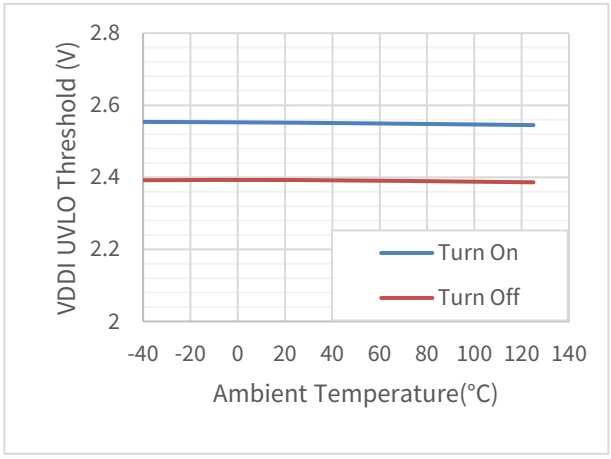


Figure 6.4 VDDI UVLO Threshold vs Temperature

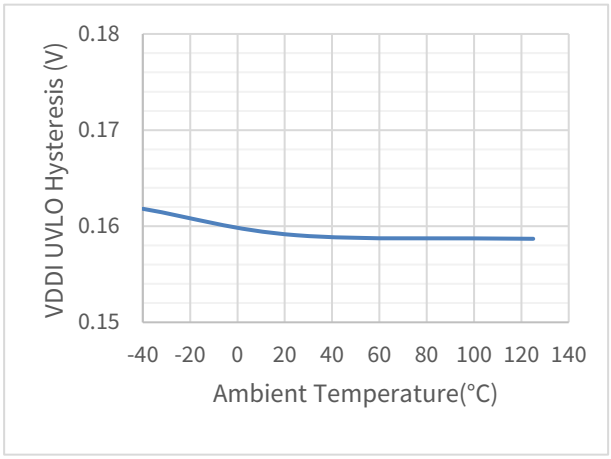


Figure 6.5 VDDI UVLO Hysteresis vs Temperature

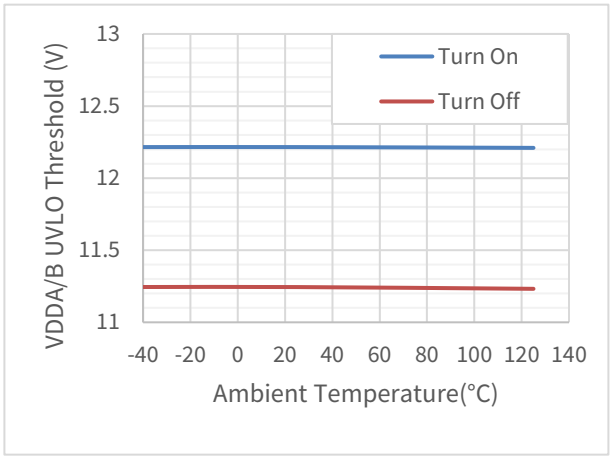


Figure 6.6 6602MC VDDA/B UVLO Threshold vs Temperature

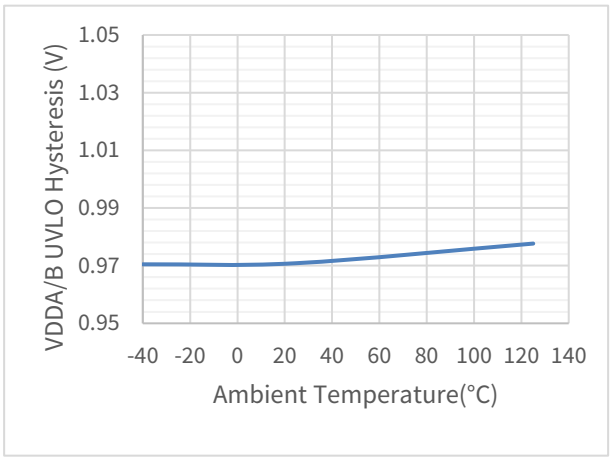


Figure 6.7 6602MC VDDA/B UVLO Hysteresis vs Temperature

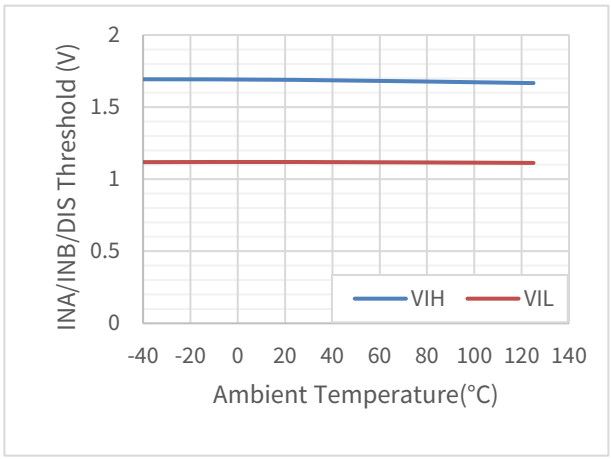


Figure 6.8 INA/INB/DIS Threshold vs Temperature

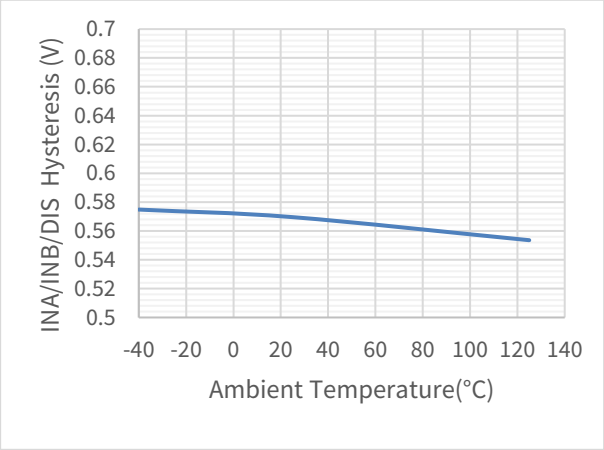


Figure 6.9 INA/INB/DIS Hysteresis vs Temperature

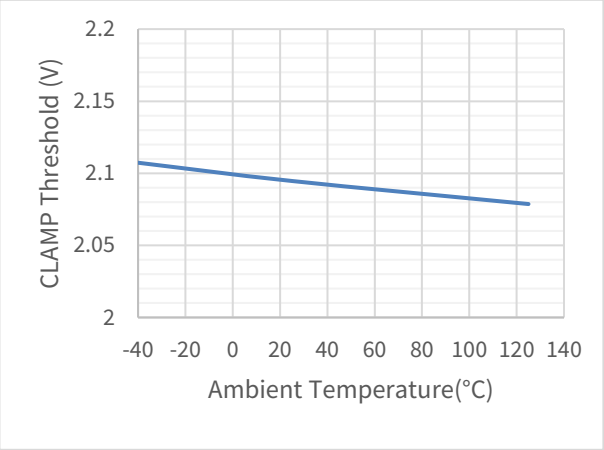


Figure 6.10 CLAMP Threshold Voltage vs Temperature

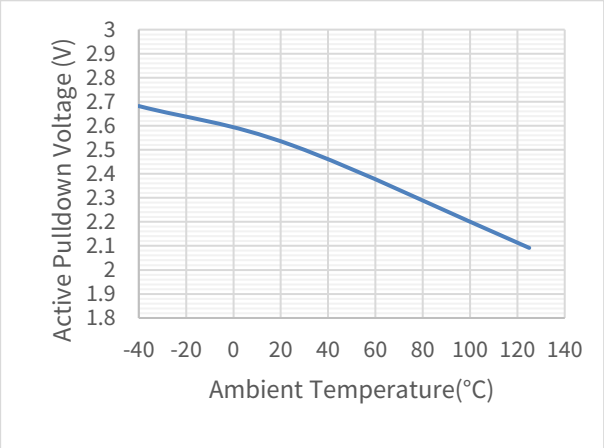


Figure 6.11 Active Pulldown Voltage vs Temperature

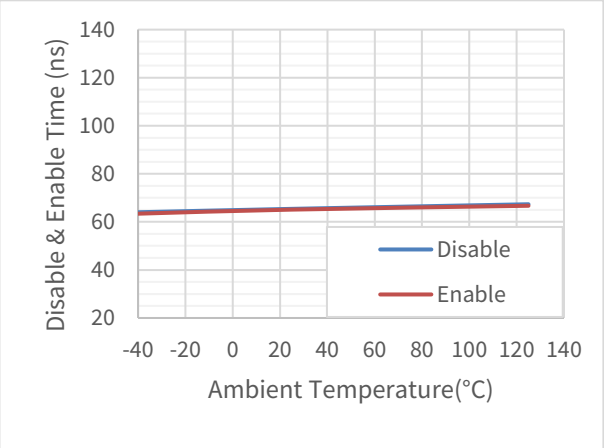


Figure 6.12 Disable & Enable Time vs Temperature

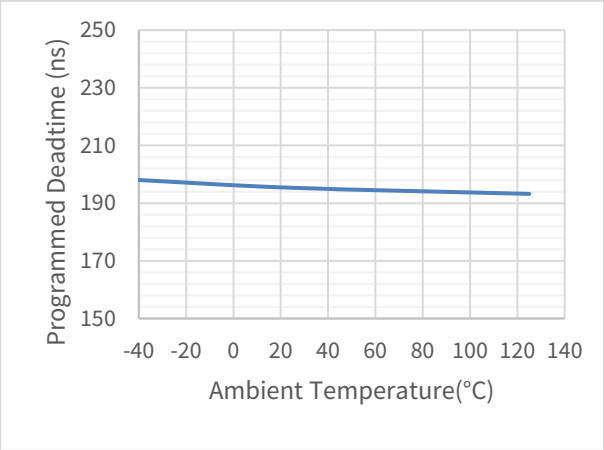


Figure 6.13 Deadtime (RDT=20kΩ) vs Temperature

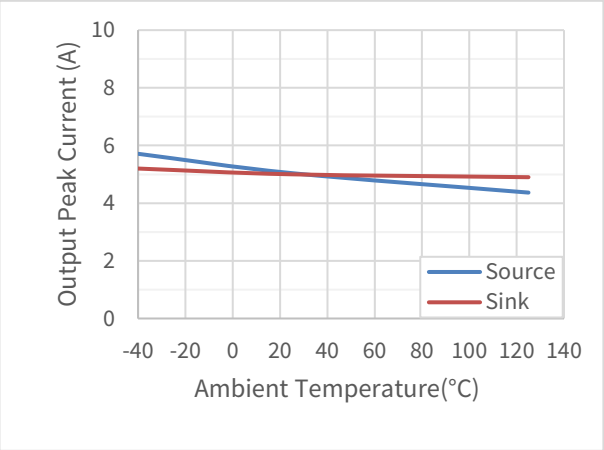


Figure 6.14 Output Peak Current vs Temperature

6.4. Parameter Measurement Information

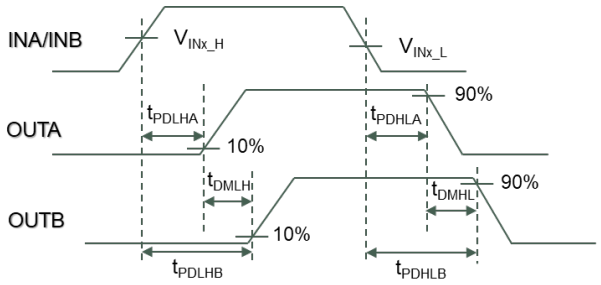


Figure 6.15 Propagation Delay and Channel to Channel Delay Match Time, connect DT to VDDI

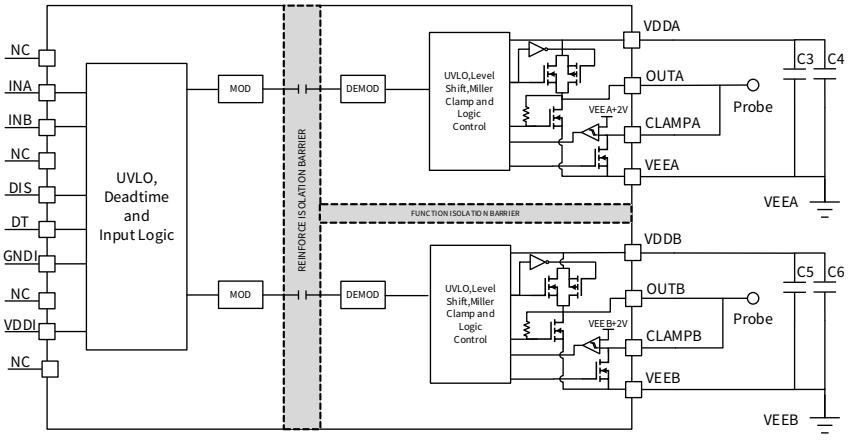


Figure 6.16 Channel to Channel Delay Match Test Circuit

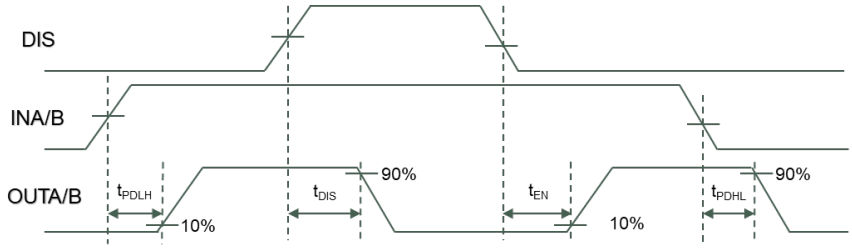


Figure 6.17 Disable Time and Enable Time

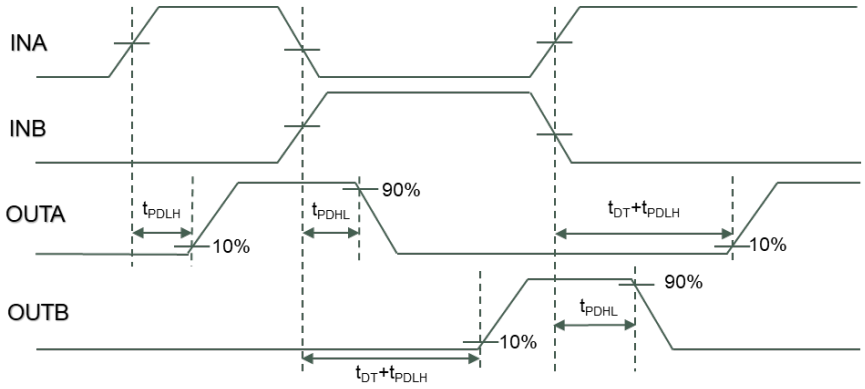


Figure 6.18 Deadtime, Determined by RDT

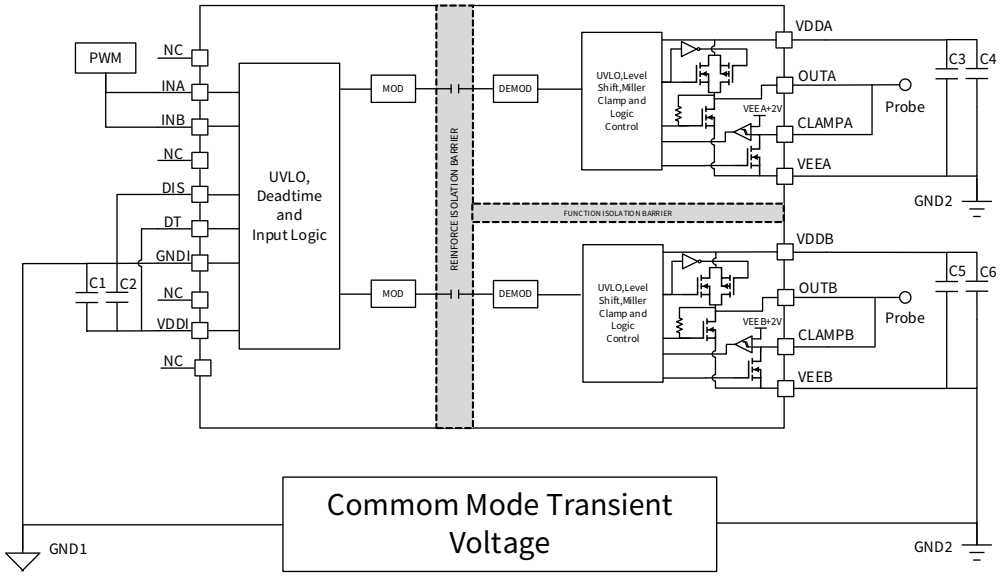


Figure 6.19 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	mm	Shortest terminal-to-terminal distance across the package surface
Distance Through Insulation	DTI	32	μm	internal gap
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

7.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms		I to IV	
	For Rated Mains Voltage ≤ 300Vrms		I to IV	
	For Rated Mains Voltage ≤ 600Vrms		I to IV	
	For Rated Mains Voltage ≤ 1000Vrms		I to III	
Climatic Category			40/125/21	
Pollution Degree	per DIN VDE 0110, Table 1		2	
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	V_{peak}
Apparent Charge	Method B ,routine test(100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, $V_{pd(m)}$=V_{IORM}×1.875,t_{ini}=t_m=1s	q_{pd}	<5	pC
	Method A, after Environmental Tests Subgroup 1,$V_{pd(m)}$=V_{IORM}×1.6, t_{ini}=60s, t_m=10s			pC
	Method A,after Input and Output Safety Test Subgroup 2 and Subgroup 3,$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s			pC

Description	Test Condition	Symbol	Value	Unit
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	8000	V_{peak}
Maximum Impulse Voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{IMP}	6000	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	V_{peak}
Isolation Resistance	V_{IO}=500V at T_A=T_S=25°C	R_{IO}	$>10^{12}$	Ω
	V_{IO}=500V at T_A=T_S=150°C		$>10^{9}$	Ω
	V_{IO}=500V at 100°C≤T_A≤125°C		$>10^{11}$	Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1.2	pF
Insulation Specification per UL1577				
Withstand Isolation Voltage	V_{TEST} = 1.2 × V_{ISO}, t = 1 sec, 100% production test	V_{ISO}	5700	V_{rms}

1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

7.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI6602Mx

Description	Test Condition	Side	Value	Unit
Safety Supply Power	$R_{\theta JA}$ = 97 °C/W[1)], T_J = 150 °C, T_A = 25 °C	Input	12	mW
		Driver A, Driver B	638	mW
		Total	1288	mW
Safety Supply Current	$R_{\theta JA}$ = 97 °C/ W[1)], VDDA/B = 12V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	53.1	mA
	$R_{\theta JA}$ = 97 °C/ W[1)], VDDA/B = 25V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	25.5	mA
Safety Temperature[2)]			150	°C

1) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

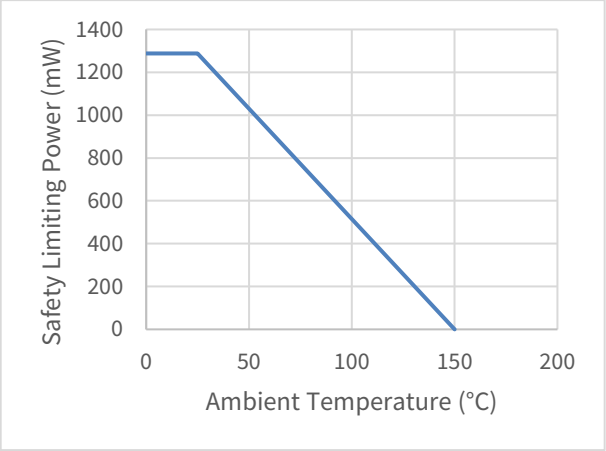


Figure 7.1 NSI6602Mx Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI6602Mx

7.4. Safety-Related Certifications

The NSI6602Mx are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-17: 2017-01	Certified by CQC11-471543-2012 GB4943.1-2022
Single Protection, 5700Vrms Isolation voltage	Single Protection, 5700Vrms Isolation voltage	Reinforced insulation at V_{IORM}=1414V_{peak} V_{IOTM}=8000V_{peak} V_{IOSM}=10000V_{peak}	Reinforced insulation
E500602	E500602	File (pending)	CQC23001378663

8. Function Description

8.1. Overview

NSI6602M is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies. NSI6602M has some useful protections, such as under voltage lock-out (UVLO) for both input and output supply, a disable pin, dead-time control, active miller clamp, short circuit clamping, active pull down, and default low output as input is floating. The functional circuit block diagram is shown as below:

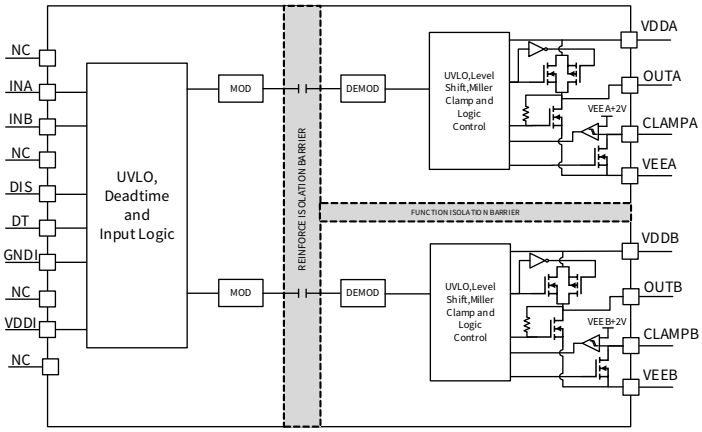


Figure 8.1 Functional Block Diagram

8.2. Under Voltage Lock Out (UVLO)

The NSI6602M has an internal under voltage lock out (UVLO) protection on the both input and output supply circuit blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDDI or VDDA/VDDB is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins.

The VDDI and VDDA/B ULVO protections have hysteresis (V_{VDD_HYS}) to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

8.3. Input and Output Logic Table

When the device is power up, setting the DIS pin high can shut down both outputs simultaneously. Left open or grounding the DIS pin can allow the device operating normally.

Table 8.1 Output status vs. Input and Power status

VDDI status	VDDA/B status	DIS	IN		OUT		NOTE[1)]
			A	B	A	B	
PU	PU	L or O	L	H	L	H	If Deadtime function is used, output transits to high after the deadtime expires.
PU	PU	L or O	H	L	H	L	
PU	PU	L or O	H	H	H	H	DT pin is pulled to VDDI.
PU	PU	L or O	H	H	L	L	DT is left open or programmed with R_{DT}.
PU	PU	L or O	L	L	L	L	
PU	PU	L or O	O	O	L	L	
PU	PU	H	X	X	L	L	
PU	PD	X	X	X	L	L	Active pull-down
PD	PU	X	X	X	L	L	Active pull-down

1) PD= Power Down; PU= Power Up; H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant;

8.4. Programmable Deadtime (DT pin)

8.4.1. Pulling the DT Pin to VDDI

This allows outputs match inputs completely and no deadtime is asserted.

8.4.2. DT Pin Left Open or Connected to a Programming Resistor between DT and GND Pins

If the DT pin is left open, the deadtime duration (t_{DT}) is set to <35ns. t_{DT} can be programmed by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined from Equation 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

The recommended value of R_{DT} is between from 1kΩ to 200kΩ. The steady state voltage at DT pin is about 0.8 V, and the DT pin current will be less than 10uA when R_{DT} =100kΩ. It is also recommended to parallel a ceramic capacitor, for example 2.2nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 7.2:

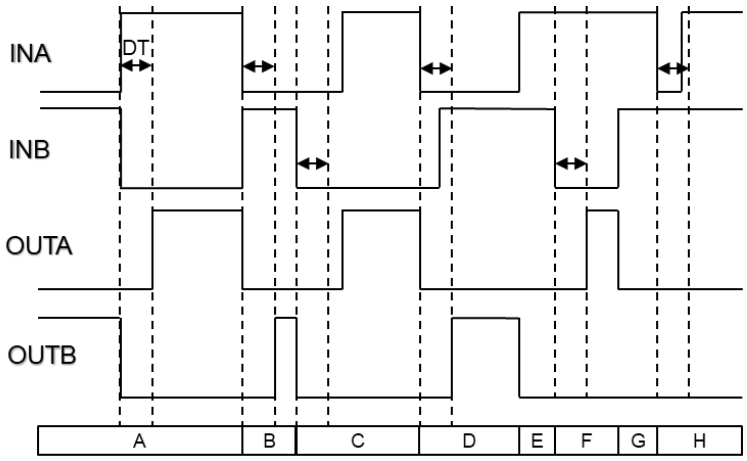


Figure 8.2 Input and Output Logic with the Programmed Deadtime

Condition	*Result*
A: INA goes high, and INB goes low.	OUTB goes low immediately, then OUTA goes high after the programmed deadtime which is assigned at INB goes low.
B: INA goes low, and INB goes high.	OUTA goes low immediately, then OUTB goes high after the programmed deadtime which is assigned at INA goes low.
C: INB goes low, then INA goes high after deadtime.	OUTB goes low immediately, then OUTA goes high immediately when INA goes high.
D: INA goes low, then INB goes high before deadtime.	OUTA goes low immediately, then OUTB goes high after deadtime
E: INA goes high, INB is still high.	OUTB goes low immediately and OUTA keeps low.
F: INA is still high, INB goes low.	OUTA goes high after deadtime while INB is low and OUTB keeps low.
G: INA is still high, INB goes high after deadtime	OUTA goes low immediately and OUTB keeps low.
H: INA goes low then goes high before deadtime while INB is still high.	OUTA keeps low and OUTB keeps low because deadtime control.

8.5. Active Pull Down

This function helps to pull the IGBT or MOSFET gate to the off-state when VCC2 is not connected to the power supply. This feature prevents the false turn-on of OUT and CLAMP pins by clamping the output to approximately 2V.

8.6. Short Circuit Clamping

Short circuit is used to clamp the deriver output voltage as well as to pull the miller clamp pins CLAMPA or CLAMPB to a bit higher than their drive-side supply pins respectively. This function helps to protect the gate of a MOSFET or IGBT from overvoltage breakdown. The short circuit clamping is implemented by adding an additional circuit between the dedicated pins and the drive-side supply. The internal diode circuitry can conduct 500mA current to the supply for 10us.Use of external schottky diode may be added to improve the current capability and tighter clamping.

8.7. Active Miller Clamp

The active miller clamp function helps to prevent the false turn-on of the power switches caused by the miller current in applications, such as half bridge configuration, where switched off IGBT turns to dynamically turn-on during turn on period of the opposite IGBT.

It usually happens when a unipolar power supply is used. To avoid such false turn-on of switches a miller clamp allows sinking the miller current across a low impedance path in this dv/dt situation. During turn-off the gate voltage is monitored and the power-switch gate voltage is clamped to less than 2V referred to VEE2. The clamp is designed for a miller current in the same range as the nominal output current.

8.8. ESD Protection

Figure 7.3 shows the multiple diodes involved in the ESD protection part of NSI6602Mx.

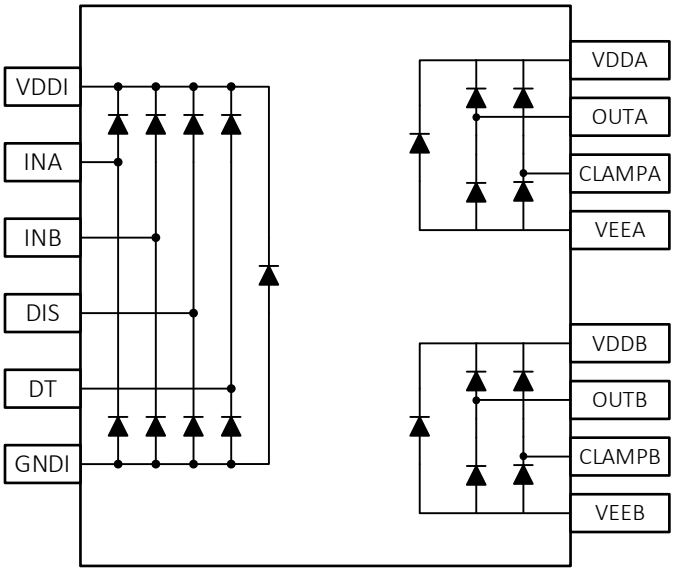


Figure 8.3 ESD Structure

9. Application Note

9.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSi6602M which could be used in several popular power converter topologies such as half-bridge/full bridge/LLC isolated topologies, buck-boost topologies and 3-phase motor drive applications.

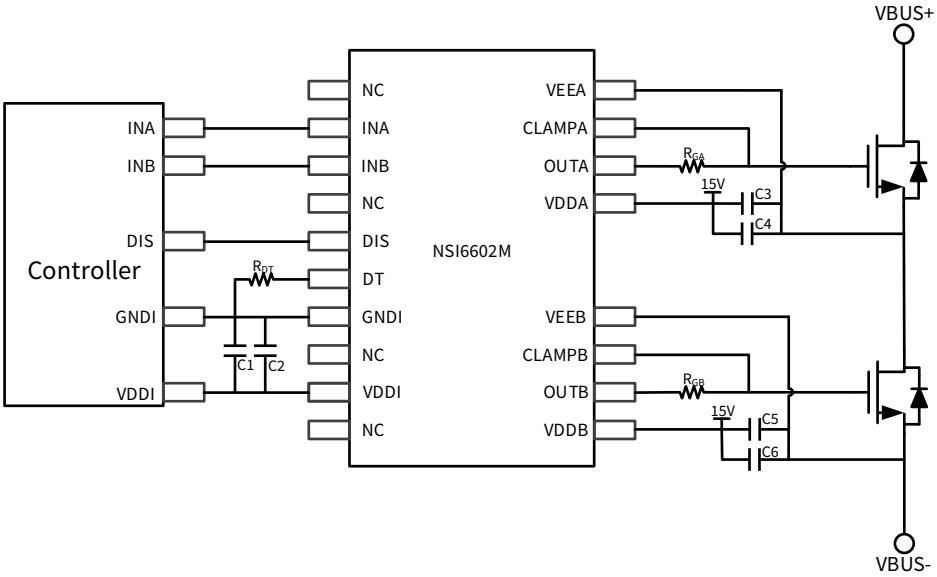


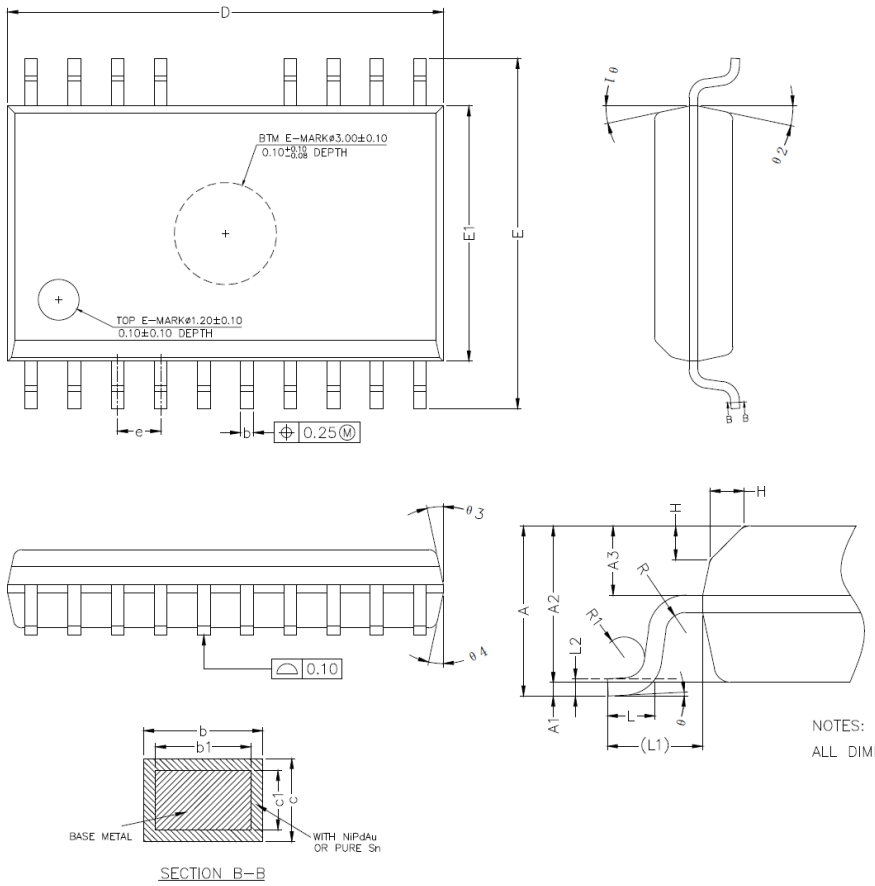
Figure 9.1 Typical Half-Bridge Application Schematic

9.2. PCB Layout

PCB layout is important to get optimal performance. Some key guidelines are:

- Low-ESR and low-ESL bypass capacitors should be placed close to the device between pin VDDI to GND and pin VDDA/B to GNDA/B.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6602M close to power transistor.
- Place large amount of copper connecting to VDDA/B pin and GNDA/B pin for thermal dissipation.
- To ensure isolation performance between primary and secondary side, the space under the device should keep free from any plane, trace, pad or via.

10. Package information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	0.20	0.30
A2	2.20	2.30	2.40
A3	0.97	1.02	1.07
b PURE Sn	0.33	–	0.46
NiPdAu	0.32	–	0.43
b1	0.32	0.37	0.42
c PURE Sn	0.23	–	0.32
NiPdAu	0.22	–	0.29
c1	0.22	0.25	0.28
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.17	1.27	1.37
H	0.40	0.50	0.60
L	0.55	0.70	0.85
L1	1.40REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 10.1 SOW18 Package Shape and Dimension

11. Ordering Information

Part No.	*Isolation Rating(kV_{RMS})*	*Driver-side UVLO TYP.*	*Temperature*	*Auto-motive*	*Package Drawing*	*MSL*	*SPQ*
NSI6602MB-DSWTR	5.7	9V	-40 to 125℃	NO	SOW18	2	1000
NSI6602MC-DSWTR	5.7	12V	-40 to 125℃	NO	SOW18	2	1000

12. Tape and Reel Information

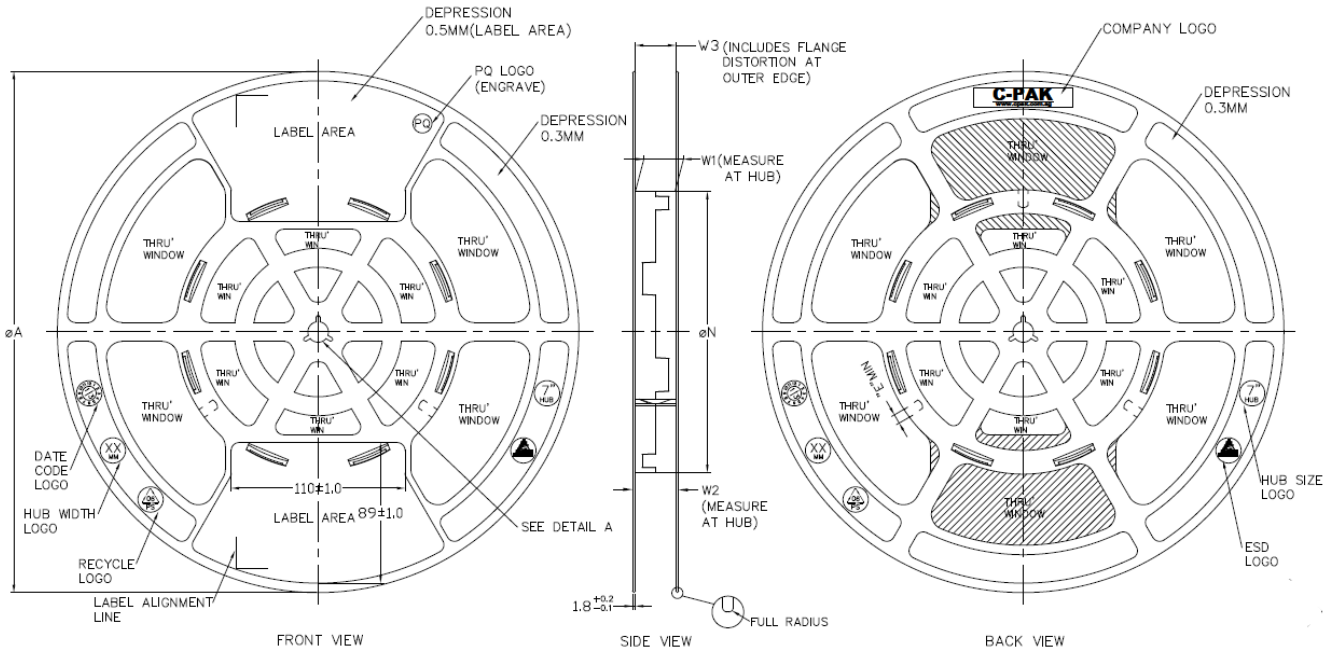


Figure 12.1 Tape Information

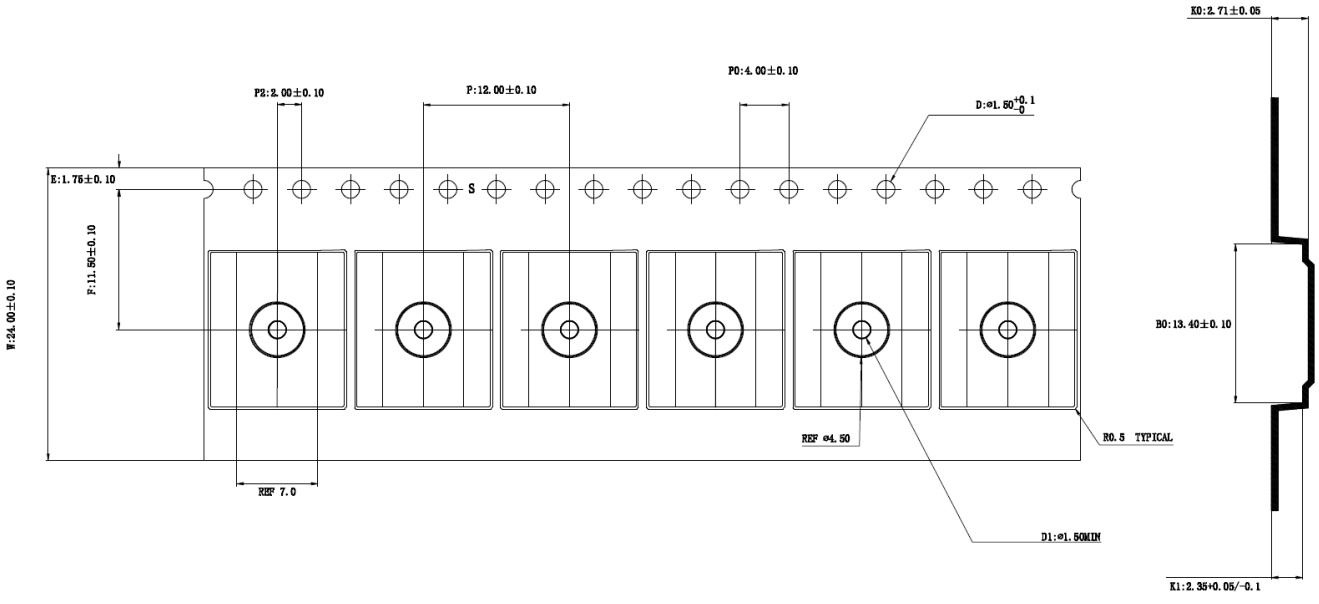


Figure 12.2 Reel Information

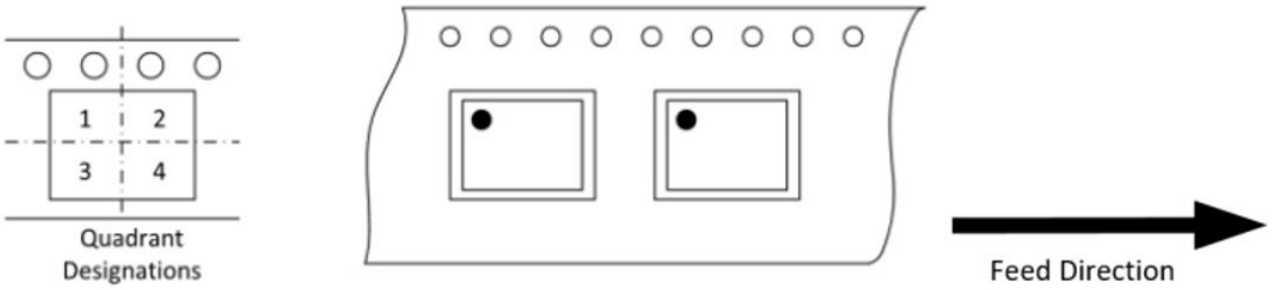


Figure 13.3 Quadrant Designation for Pin1 Orientation in Tape

13. Revision History

Revision	Description	Date
1.0	Initial version	2024/4/29

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