NSI7258-Q1
1700-V 50mA Solid-State Relay
Datasheet (EN) 1.0

Product Overview

The NSI7258-Q1 is a single-channel solid-state relay (SSR), which is pin-compatible for popular photo MOSFET. The SSR turns ON with a minimum input current of 5.5mA. It can conduct 30mA current at ON state, with resistance less than 250Ω. The SSR turns off with an input voltage of 0.5V or less. It can withstand 1000V voltage at OFF state, with less than 1μA leakage current.

The NSI7258-Q1 uses NOVOSENSE's high reliability isolation technology. While the input circuit imitates the characters of LEDs, it has performance advantages compared to standard photo MOSFET, including better reliability and aging performance, higher working temperature, shorter turn-on and turn-off delay. As a result, the NSI7258-Q1 is suitable to replace photo MOSFET in high reliability system.

Key Features

- AEC Q-100 Qualified for Grade 1: TA from –40 °C to 125 °C
- Normally open (1-Form-A) solid state relay
- Up to 5000Vrms Insulation voltage
- Breakdown voltage: 1700V
- OFF state leakage current: <1μA at 1000V
- ON state resistance: <250Ω at 10mA load current
- Input forward threshold current: <5.5mA
- Turn on time: <0.3ms
- Turn off time: <0.05ms
- RoHS-compliant Packages: SOW12
- Creepage and clearance ≥ 8mm (input-output)
- Creepage and clearance ≥ 5.91mm (between drain pins of MOSFETs)
- Meets CISPR32 Class B and CISPR 25 Class 5 EMI limits without ferrite beads on a 2-layer PCB

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-11:2017-01

Applications

- Battery Management System (BMS)
- Electric Vehicle Chargers

Device Information

Part Number	Package	Body Size
NSI7258-Q1SWLR	SOW12	10.30 × 7.50mm

Functional Block Diagrams

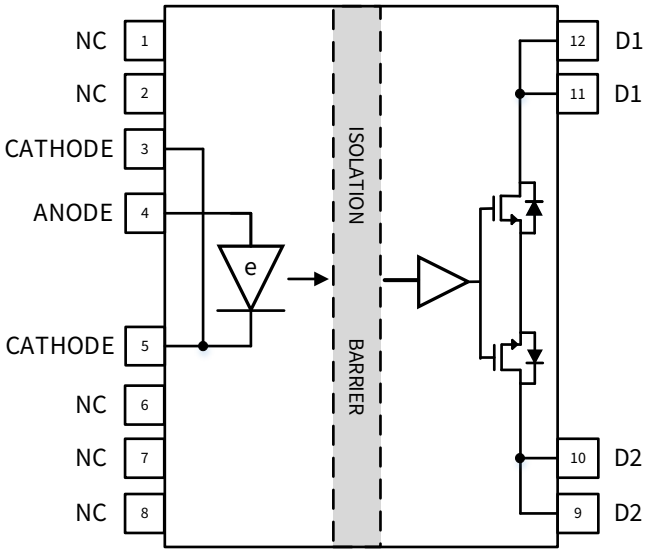


Figure 1. NSI7258 Block Diagram

INDEX

1. Pin Configuration and Functions

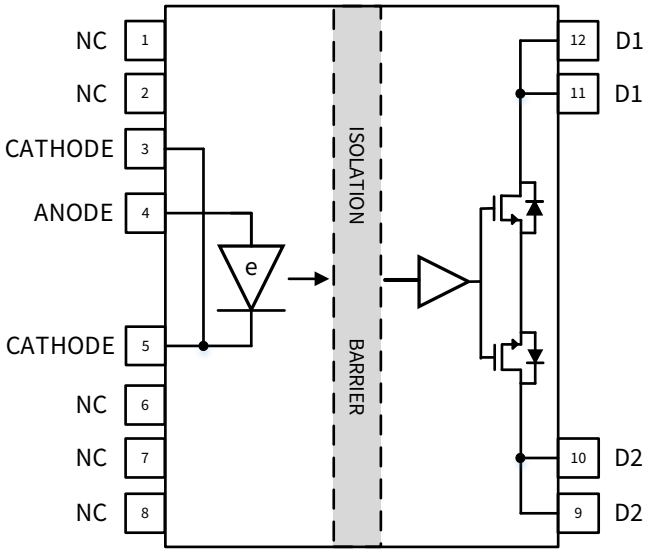


Figure 1.1 NSI7258-Q1 Package

Table 1.1 NSI7258-Q1 Pin Configuration and Description

NSI7258 PIN NO.	*SYMBOL*	*FUNCTION*
1, 2, 6, 7, 8	NC	No Connection
3, 5	CATHODE	Cathode of LED Emulator (Internally connected)
4	ANODE	Anode of LED Emulator
9, 10	D2	Drain 2 (Internally connected)
11, 12	D1	Drain 1 (Internally connected)

Note a: NSI7258-Q1 can work properly as long as either one of Pin3 and Pin5 is connected to external circuit.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input Current	I_F			30	mA	
Reverse Input Voltage	V_R			6.5	V	
Output Withstand Voltage	V_O			1700	V	
Output Load Current	I_O			50	mA	
Avalanche Current(1)	I_{AVA}			0.6	mA	
Ambient Temperature	T_A	-40		125	°C	
Operating Junction Temperature	T_J	-40		150	°C	
Storage Temperature	T_{stg}	-55		150	°C	

(1) t_m = 1 min, duty cycle = 0.1%, cumulative of 5 minutes over lifetime, Guaranteed by bench characterization.

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±2.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1.0	kV

4. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input current (ON)	I_{Fon}	7		20	mA	
Input voltage (OFF)	V_{Foff}	-5		0.5	V	
Operating Temperature	T_A	-40		125	°C	
Output withstand voltage	V_o			1000	V	
Output load current	I_o			30	mA	

5. Thermal Information

Parameters	Symbol	SOW12	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	70	°C /W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	36.1	°C /W
Junction-to-board thermal resistance	$R_{\theta JB}$	24.7	°C /W
Junction–to-top characterization parameter	Ψ_{JT}	10.3	°C /W
Junction-to-board characterization parameter	Ψ_{JB}	23.3	°C /W

6. Specifications

6.1. Electrical Characteristics (DC)

(I_{Fon}=7mA to 20mA, V_{Foff} =-5V to 0.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at T_A=25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Input Forward Threshold Current Low to High	I_{FON}		3.9	5.5	mA	I_O=2mA
Input Forward Voltage	V_F	1.6	1.8	2.1	V	I_F=10mA
Output Withstand Voltage	V_{O_OFF}	1700			V	I_O=100μA
Output Leakage Current	I_{O_OFF}			1	μA	V_O=1000V
Output Resistance	R_{ON}		80	250	Ω	I_O=10mA
Common Mode Transient Immunity	CMTI		100		kV/μs	(Ref Fig 6.9)

6.2. Switching Specifications (AC)

(I_{Fon}=7mA to 20mA, V_{Foff} =-5V to 0.5V, T_A=-40°C to 125°C. Unless otherwise noted, Typical values are at T_A=25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Turn-On Time	t_{ON}		0.106	0.3	ms	V_{DD}=40V, R_{LOAD}=20k (Ref Fig 6.10)
Turn-Off Time	t_{OFF}		0.006	0.05	ms	V_{DD}=40V, R_{LOAD}=20k (Ref Fig 6.10)

6.3. Typical Performance Characteristics

(Unless otherwise noted, T_A=25°C)

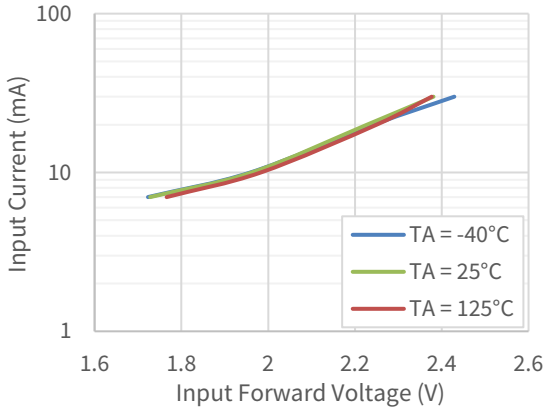


Fig 6.1 Input Current vs. Input Forward Voltage

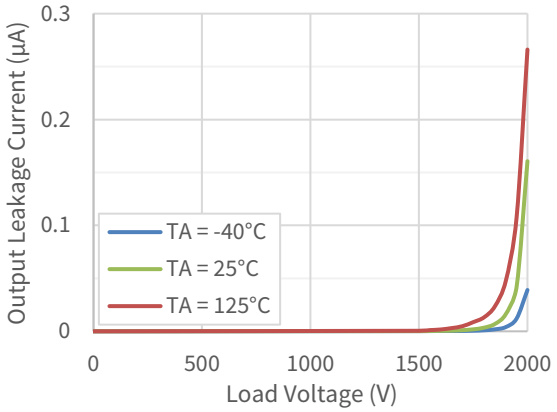


Fig 6.2 Output Leakage Current vs. Load Voltage

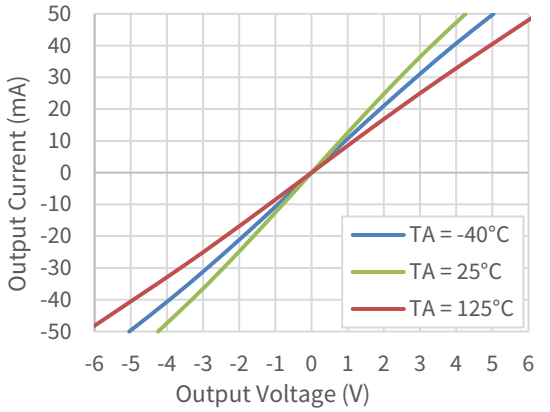


Fig 6.3 Output Current vs. Ambient Temperature

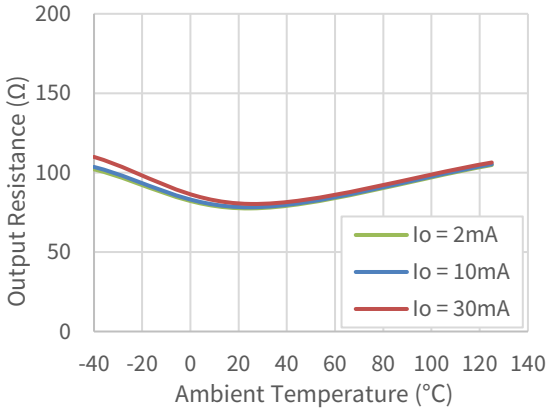


Fig 6.4 Typical On-Resistance vs. Ambient Temperature

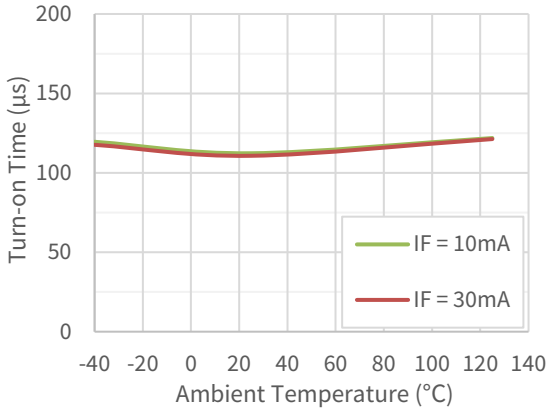


Fig 6.5 Turn-on Time vs. Ambient Temperature

(Test Condition: V_{DD} = 40V, R_{LOAD} = 20kΩ)

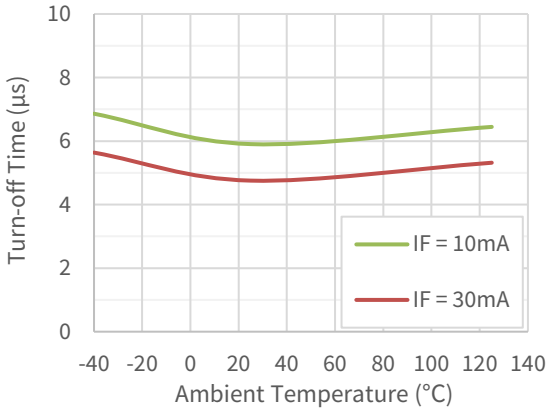


Fig 6.6 Turn-off Time vs. Ambient Temperature

(Test Condition: V_{DD} = 40V, R_{LOAD} = 20kΩ)

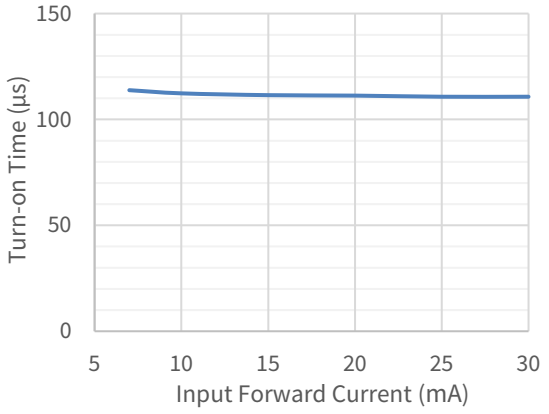


Fig 6.7 Turn-on Time vs. Input Forward Current
(Test Condition: V_{DD} = 40V, R_{LOAD} = 20kΩ)

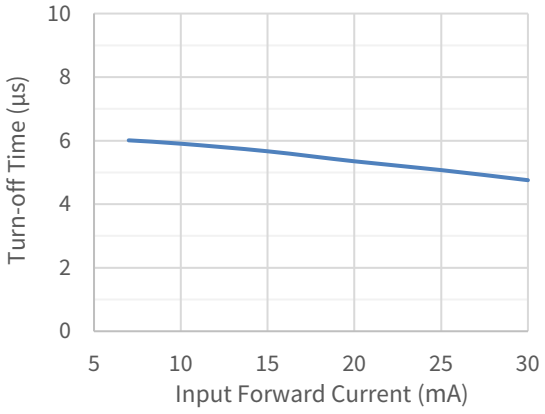


Fig 6.8 Turn-off Time vs. Input Forward Current
(Test Condition: V_{DD} = 40V, R_{LOAD} = 20kΩ)

6.4. Parameter Measurement Information

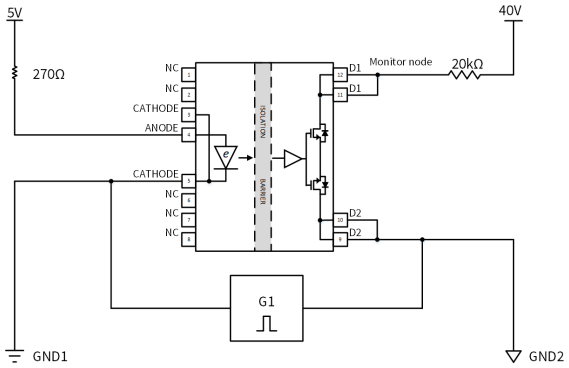


Figure 6.9 Common Mode Transient Immunity Test Circuit

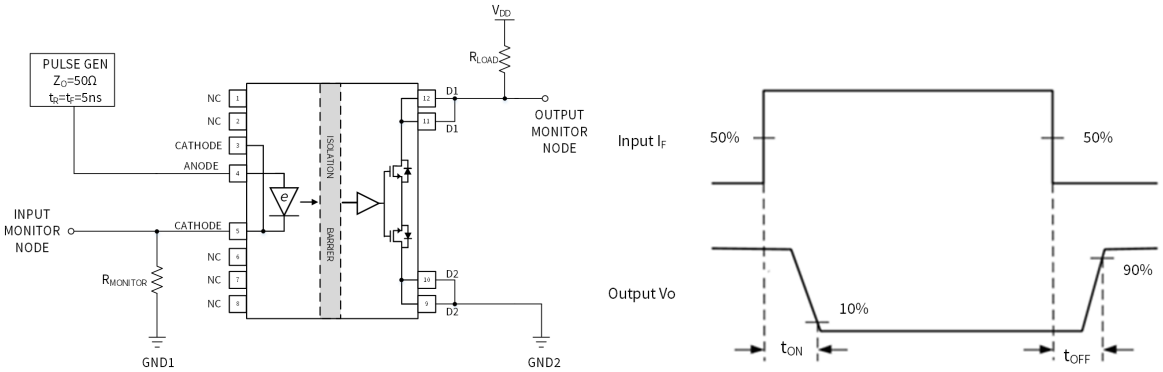


Figure 6.10 Switching Characteristics Test Circuit and Waveform

7. High Voltage Feature Description

7.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value* *SOW12*	*Unit*	*Comments*
Minimum External Clearance	CLR	8	mm	IEC 60664-1:2007
Minimum Externa Creepage	CPG	8	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	13	um	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

7.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms		I to IV	
	For Rated Mains Voltage ≤ 300Vrms		I to IV	
	For Rated Mains Voltage ≤ 600Vrms		I to IV	
	For Rated Mains Voltage ≤ 1000Vrms		I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110			2	
Maximum repetitive isolation voltage		V_{IORM}	1414	V_{PEAK}
Maximum working isolation voltage	AC voltage	V_{IOWM}	1000	V_{RMS}
	DC voltage		1414	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2*V_{IORM}$, t_m = 10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.3*V_{IORM}$, t_m=10s			
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2*V_{IOTM}$, t_{ini} = 1s $V_{pd(m)}=1.5*V_{IORM}$, t_m=1s（method b1）or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$(method b2)			
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	7071	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	5439	V_{PEAK}

Description	Test Condition	Symbol	Value	Unit
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	7071	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25°C	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100°C ≤ T_{amb} ≤ 125°C	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	1.6	pF
Maximum safety temperature		Ts	150	°C
UL1577				
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	5000	V_{RMS}

7.3. Regulatory Information

The NSI7258-Q1 is approved by the organizations listed in table.

UL		TUV	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Basic Insulation V_{IORM}=1414Vpeak V_{IOTM}=7071Vpeak V_{IOSM}=7071Vpeak	Basic insulation
E500602	E500602	R 50632636	CQC24001426160

8. Application Note

8.1. Typical Application Circuit

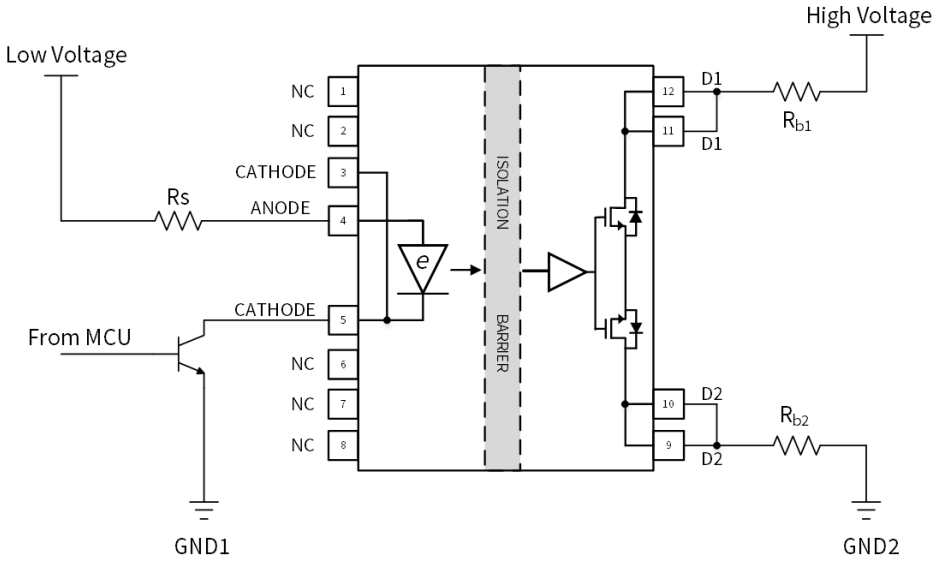


Figure 8.1 Typical application circuit

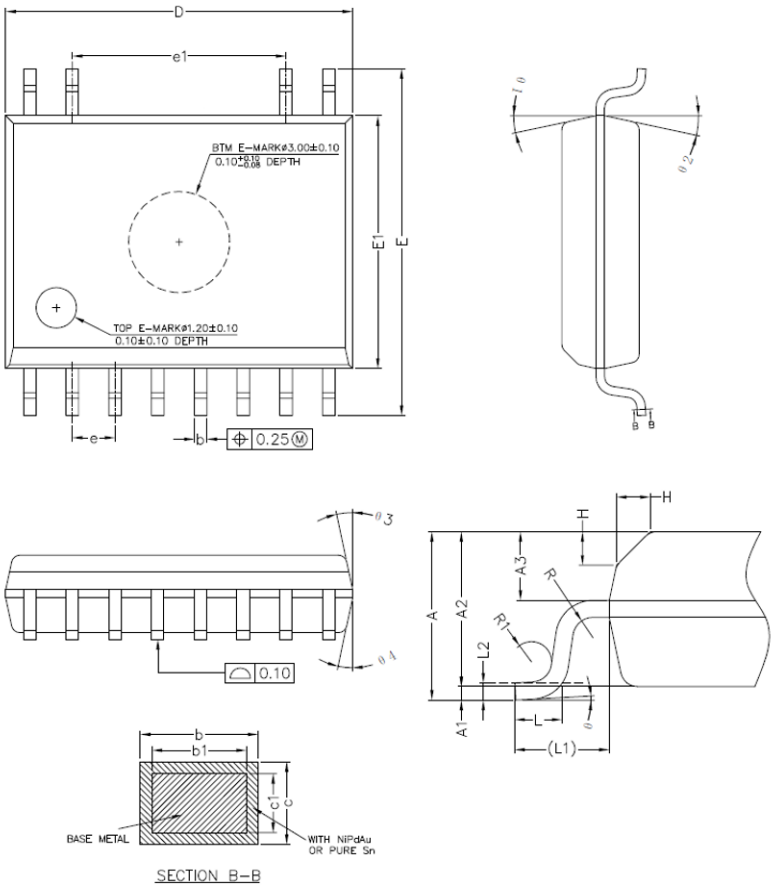
The NSI7258-Q1 is a single-channel solid-state relay, which is pin-compatible for popular photo MOSFET. It uses NOVOSENSE's high reliability isolation technology, which has performance advantages compared to standard photo MOSFET including better reliability and aging performance, higher working temperature, shorter turn-on and turn-off delay. The SOW12 Package allows the NSI7258-Q1 to support 0.6 mA output avalanche current (AC sinusoidal wave, T_m=1min, duty cycle < 0.1%, cumulative of 5 minutes over lifetime, T_A=25°C), with voltage clamped at more than 2000V.

The input circuit of NSI7258-Q1 imitates the characters of photodiode and delivers energy through the on-chip power transfer block to drive two inner back-to-back high-voltage SiC MOSFETs. When current is driven into the input side, the gate of the MOSFETs is charged and switches MOSFETs on.

A typical application circuit(Figure 8.1) shows NSI7258-Q1's input side(low voltage side) being controlled by the MCU to switch the output(high voltage side). Rs is used as current limiting resister to control the input forward current. NOVOSENSE's high reliability isolation technology protects the low voltage side of the circuit from the high voltage side.

Pins 3 to 5, 8 to 9 and 15 to 16 are internally connected. In routing the PCB layout, using either of the internally-connected pins or shorting the pins is acceptable.

9. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	0.20	0.30
A2	2.20	2.30	2.40
A3	0.97	1.02	1.07
b PURE Sn	0.33	–	0.47
NiPdAu	0.33	–	0.44
b1	0.33	0.38	0.43
c PURE Sn	0.22	–	0.32
NiPdAu	0.22	–	0.29
c1	0.22	0.25	0.28
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.17	1.27	1.37
e1	6.25	6.35	6.45
H	0.40	0.50	0.60
L	0.55	0.70	0.85
L1	1.40REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 9.1 SOW12 Package Shape and Dimension in millimeters

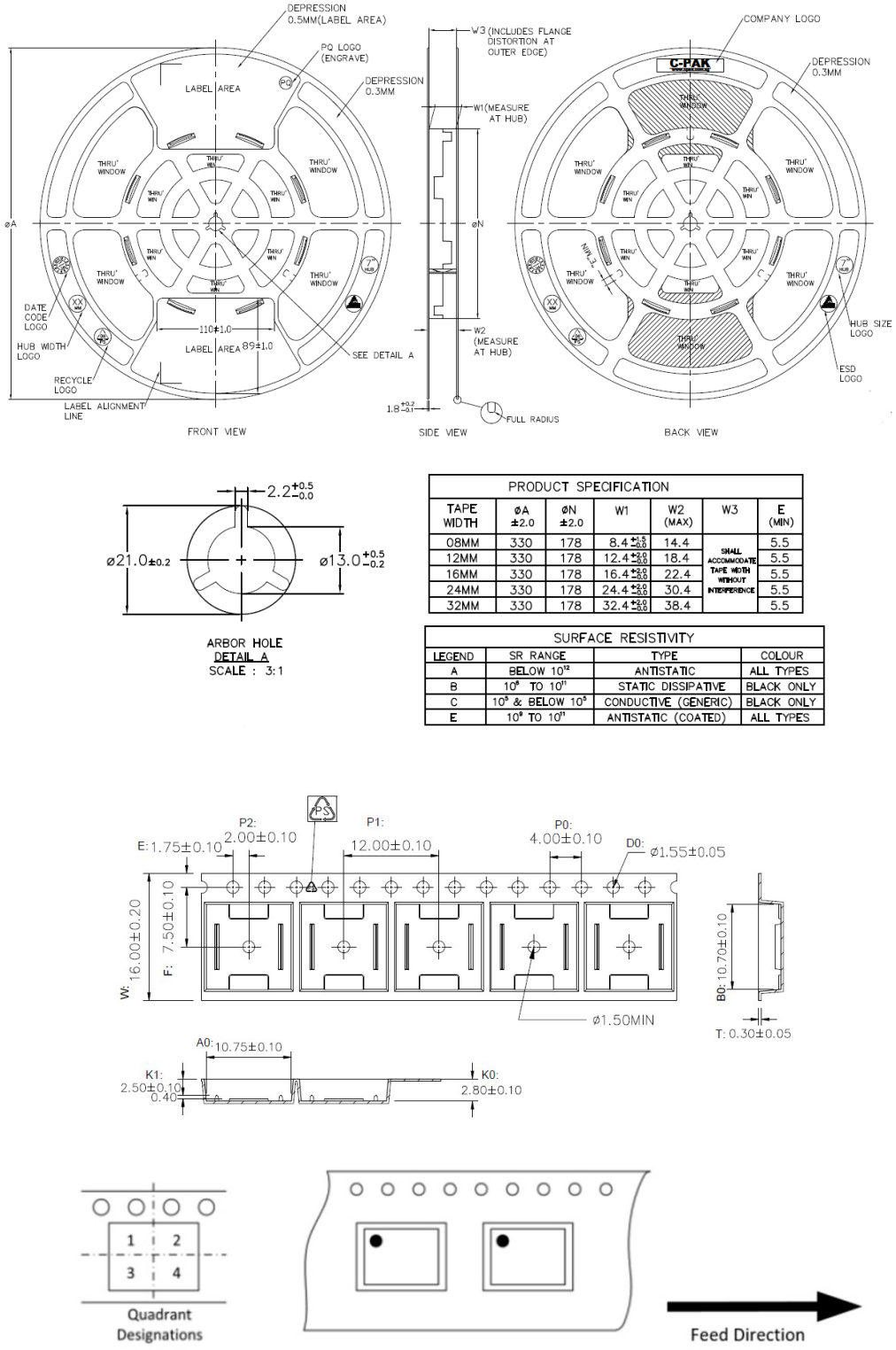
10. Ordering Information

Part Number	*Isolation Rating (kV)*	*Number of Channels*	*Recommended withstand voltage (V)*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NSI7258-Q1SWLR	5	1	1000	-40 to 125°C	3	SOIC12	SOW12	1000

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*
NSI7258-Q1	Click here	Click here	Click here

12. Tape and Reel Information



PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SMALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{8} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Tape and Reel Information of SOW12

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/8/30

IMPORTANT NOTICE

The information given in this document (the "Document") shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE's products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE's products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an "AS IS" basis, and is intended only for skilled developers designing with NOVOSENSE's products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE's products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd