NEWSIGHT IMAGING
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3D Machine Vision
NSI9000
CMOS Image Sensor

Event-driven 3D global shutter CIS
Resolution: 1024x480 pixels
Supports any rectangular sub-resolution
2D, 3D & Multi-triangulation

Extended range compared to iTOF
Flexibly programable per application
Dynamic event detection
Range-gated imaging
High Dynamic Range (HDR) 3D solution

Overview

The NSI9000 is an advanced, event-driven, 3D CMOS image sensor chip specifically designed to meet the rigorous demands of applications requiring rapid event detection and real-time response. This makes it ideal for use in a variety of fields, including LiDAR, Industry 4.0 automation, and automotive safety systems, where quick and accurate data processing is critical.

Key features of the NSI9000 include:

- **Event Recognition:** Integrated directly into the pixel array, with frame rate adjustment to match the event rate, significantly reducing redundant data.
- **Pixel Specifications:** Features a 1024x480 pixel array with 5µm x 5µm pixels, designed for global shutter operation and column parallel output.
- **Synchronous Array Operation:** Supports the synchronized operation of multiple NSI9000 sensors, ideal for complex setups like LiDAR systems.
- **High Sensitivity:** Built using CMOS technology with extremely high sensitivity pixels, allowing for the capture of longer distances compared to other market sensors.
- **Configuration Interface:** Configurable via a serial interface supporting both a simple synchronous serial mode and a standard I^2C mode with a 16-bit dedicated protocol.
- **Video Output:** Delivers parallel data output in a 12-bit stream over a dedicated bus capable of supporting up to 100 MHz speed.
- **Advanced Features:** Includes programmable frame rates, multiline triangulation, eTOF 3D distance measurement per pixel, automatic exposure control to prevent saturation from close/bright objects while enhancing sensitivity to distant/dark objects, automatic peak detection for triangulation, and per-frame configuration for immediate event-based reactions.

The NSI9000's high-performance capabilities make it an excellent choice for advanced surveillance systems, automotive safety features, LiDAR applications, and Industry 4.0 automation, where precise and swift event detection is paramount.

Specifications:

Parameter	Value
Array format	1024x480 global shutter pixels 5µm x 5µm
A/D converter	Up to 12 bits precision (selectable 8-12)
Scanning resolutions	Any sub rectangular of the array
Configurations	Up to 32 pre-loaded configurations Can switch between them at frame resolution
Supply Voltage	3.3 V (Analog) and 1.8 V (Digital)
Operating temperature	-20 to 85 degrees Celsius
Input clock frequency	Up to 100 MHz
Package	88 pin OLGA type package
Interfaces	Proprietary serial + Enhanced I2C serial interface Parallel video output
3D eTOF support	Solid state 3D mapping up to 50 meters outdoor and 100 meters indoor
Frame rate	up to 208 fps full resolution, up to 100K fps one line camera mode
Readout control	Synchronous pixel clock + RDY signal
Power consumption (estimated)	< 500mW typical operation @ 47MHz, 10% duty cycle

Table 1 - Specifications

Key Features:

The NSI9000 features a state-of-the-art event driven global shutter array architecture, allowing extremely high sensitivity, while keeping low power consumption. The following are the product highlights.

- **Sensor Array**
  - Matrix of 1024x480 global shutter pixels of 5µm x 5µm
- **General**
  - Integrated configurable direct A/D converter with 12 bits precision
  - Per-frame configuration and scenario scheduler
  - Optional automatic exposure control
  - Optional automatic Triangulation peak detection per each line (center of mass algorithm support in HW)
  - Solid state eTOF support (Enhanced Time of Flight)
  - Multi-Triangulation support, up to 480 concurrent vertical points (using a line laser)
  - Integrated Bandgap reference
  - Integrated CDS for temporal noise reduction
  - Output speed/ internal processing at up to 100 MHz
  - 3 configurable operation modes:
    - Full frame data out with programmable frame rate up to 208 fps
    - Event driven frame data out:
      - Guaranteed configurable minimum Frame rate.
      - Detected event (per each half row/per pixel) aggregated from all pixels in the half row.
    - Camera mode, acquiring programmable number of frames upon command.
  - Event detection (per pixel) by comparing with a pre-configured threshold.
  - Dynamic threshold configuration support
  - Configurable Window of Interest.
  - Stop/resume video mode
  - Optional shut down of frame clock (between frames) for decreasing power consumption

- Optional frame data out inversion
- Double buffer mode for high frame rate
- Tristate on data out pins for multiple parallel sensor connections

- **Interfaces**
  - Sensor data out:
    - Parallel 12bit synchronous frame data at speeds up to 100MHz
  - Sensor configuration:
    - Proprietary serial interface
    - Enhanced I^2C serial interface
- **Input MCLK clock frequency:** up to 100 MHz
- **Operating voltage:** 3.3v (analog) and 1.8v (digital)
- **Technology:** 0.18 µm
- **Operation temperature:** -20 to 85 degrees Celsius

Package: 88 pin OLGA type package

Pin Diagram

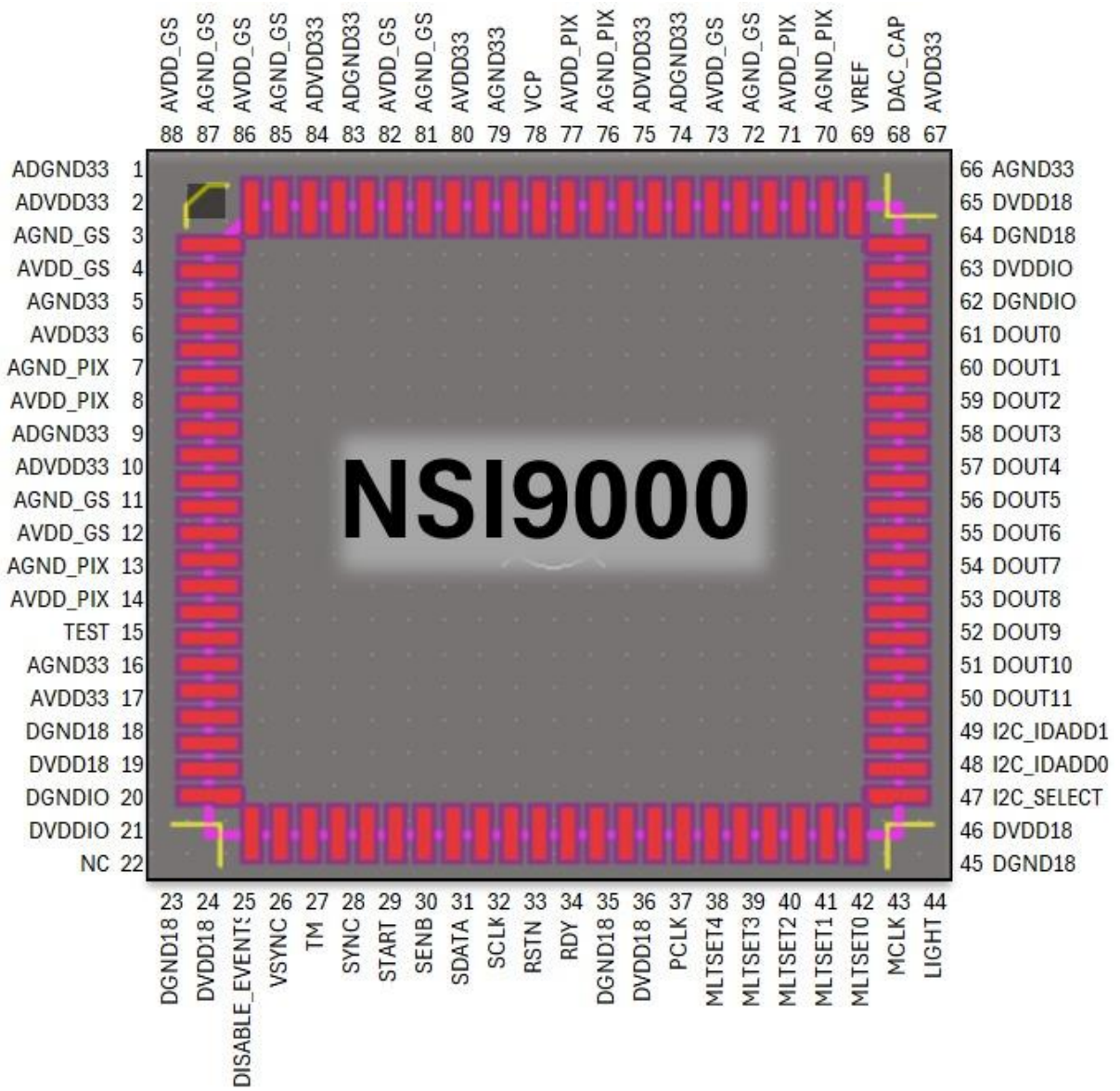

Figure 1 – Pin Diagram

NSI9000 Pins Description

PAD Name	#	I/O	Signal type	Description
Power PADS				
DVDD18	19,24,36,46,65	P	Power	Digital power supply (1.8 V)
DGND18	18,23,35,45,64	P	Power	Digital ground
DVDDIO	21,63	P	Power	Digital I/O power supply (3.3 V)
DGNDIO	20,62	P	Power	Digital I/O ground
AVDD33	6,17,67,80	P	Power	Analog power supply (3.3 V)
AGND33	5,16,66,79	P	Power	Analog ground
AVDD_GS	4,12,73,82,86,88	P	Power	Analog power supply Global Shutter (3.3V)
AGND_GS	3,11,72,81,85,87	P	Power	Analog Global Shutter ground
AVDD_PIX	8,14,71,77	P	Power	Analog Pixel power supply (3.3 V)
AGND_PIX	7,13,70,76	P	Power	Analog Pixel ground
ADVDD33	2,10,75,84	P	Power	Analog digital domain power supply (1.8 V)
ADGND33	1,9,74,83	P	Power	Analog digital domain ground
Serial Interface				
I2C_SELECT	47	I	Control	Select I2C interface (high) or NSI9000 propriety serial interface (low)
I2C_IDADD0	48	I	Control	I2C base address (bit 0)
I2C_IDADD1	49	I	Control	I2C base address (bit 1)
SCLK	32	I	Control	Serial interface clock, used both for NSI propriety serial interface and I2C interface

PAD Name	#	I/O	Signal type	Description
SDATA	31	I/O	Control	Serial interface data, synchronous to SCLK
SENB	30	I	Control	Serial enablepin, used only for NSI proprietary serial interface. Synchronous to SCLK. In I2C mode : 0: frequency above 5mhz 1: frequency less then 5mhz
Control Inputs				
MCLK	43	I	Control	Master clock
RSTN	33	I	Control	Active low reset
START	29	I	Control	Start/Stop conversion signal (synchronized internally). A Start pulse for all modes, in Continuous video mode also used as the Stop Pulse for sake of stop/resume functionality.
TM	27	I	Test	Tristate all output pins
DISABLE_EVENTS	25	I	Control	Disable event mode from external pin.
Control Outputs				
LIGHT	44	O	Control	Light Illumination Pulse
SYNC	28	O	Control	Exposure indication for additional sensors synchronization
Parallel Data Outputs				
PCLK	37	O	Control	Output data synchronized clock
RDY	34	O	Control	Parallel Data output row valid, synchronous to PCLK output rising edge.
VSYNC	26	O	Control	Parallel Data output frame valid, synchronous to PCLK output rising edge.
DOUT00	61	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT01	60	O	Digital	Digital output video data, synchronous to PCLK output rising edge.

PAD Name	#	I/O	Signal type	Description
DOUT02	59	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT03	58	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT04	57	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT05	56	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT06	55	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT07	54	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT08	53	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT09	52	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT10	51	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT11	50	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
Analog Test PADs				
DAC_CAP	68	A	Test	Ramp DAC cap input (should be connected to 1uF capacitor)
TEST	15	A	Test	Analog test pad
VREF	69	A	Test	Input for external DAC ramp, output of internal DAC ramp
VCP	78	A	power	Analog voltage for charge pump circuit
Digital Test PADs				
MLTSET0	42	I/O	Digital	Multiset External Control bit 0
MLTSET1	41	I/O	Digital	Multiset External Control bit 1
MLTSET2	40	I/O	Digital	Multiset External Control bit 2

PAD Name	#	I/O	Signal type	Description
MLTSET3	39	I/O	Digital	Multiset External Control bit 3
MLTSET4	38	I/O	Digital	Multiset External Control bit 4

Parallel Output Interface

The NSI9000 output manager block is responsible for transmitting the digital values, which represent the light levels sensed by each pixel, to the system. This process occurs within the configured Window of Interest (WOI), encompassing up to 480 rows (plus 1 test row) and 1024 columns. During the transmission of the frame (a complete array of pixel data), the VSYNC pin remains high. The RDY signal stays high while data is sent for each row but drops low during the inter-row gaps. The 12-bit DOUT bus, along with the VSYNC and RDY signals, is synchronized with the PCLK clock pin.

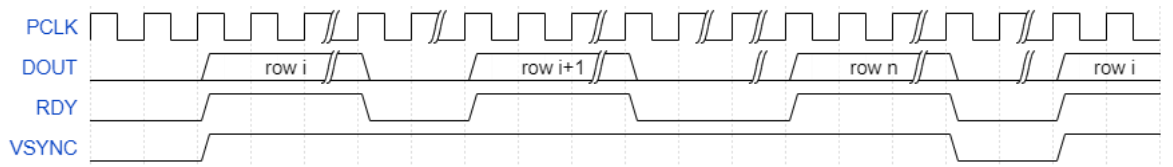

Figure 2 - parallel output bus basic scheme

The RDY and VSYNC signals can be extended to start one clock cycle before the data begins. This feature allows for synchronization with the PCLK before data transmission starts, or for slow data capture by an MCU. Additionally, the RDY and VSYNC signals can be extended to stay high for up to 127 clock cycles after the data on the DOUT bus ends. This feature ensures an integer number of 2x data length when working with a full frame that includes extra data (e.g., peak, index, or multiset data), ensuring compatibility with digital camera protocols. Note that these extensions (before and after the data) are not supported in event mode.

The DOUT data can be inverted to the more intuitive values, with dark values set to 0 and light values set to the maximum value. There is also a STOP_PCLK mode, in which the PCLK is turned off when RDY is low, and an option to extend the PCLK to remain active for one clock cycle after RDY goes low.

The NSI9000 also handles the transmission of the multiset number and the internal peak detection results to the system. The peak data consists of six 10-bit words, while the multiset data consists of one 10-bit word. After each row of pixel data, the multiset and peak information is transmitted on the DOUT bus, occupying its 10 least significant bits (LSBs). The multiset information appears first, followed by the six 10-bit peak data words at the end.

The NSI9000 also supports serial drive data on DOUT0 for peak and multiset information. Additionally, it can add a prefix of the row index for each row sent, using one 9-bit word on the LSBs of the DOUT bus. The row number ranges from 0 to 480, with the test row located at row 0.

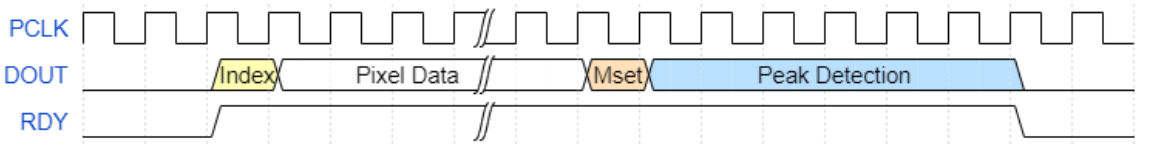

Figure 3 - Row Components of output data

In normal mode, each row is fully transmitted within one RDY pulse in a single sequence, with the amount of data determined by the configured start and end columns. For example, if the start column is 6 and the end column is 8, the data width would be 3 clock cycles.

However, in event mode, the output manager ignores the start and end column configurations and sends a full half-row, prefixed with the half-row index, totaling 513 cycles. This occurs for each half-row that contains an event. The event block must scan up to a 512-bit buffer, bit by bit, to locate the next event row. If events are detected in both halves of a row, the left half-row is sent first, with a gap of 1 SYS_CLK cycle separating the two half-rows of the same row.

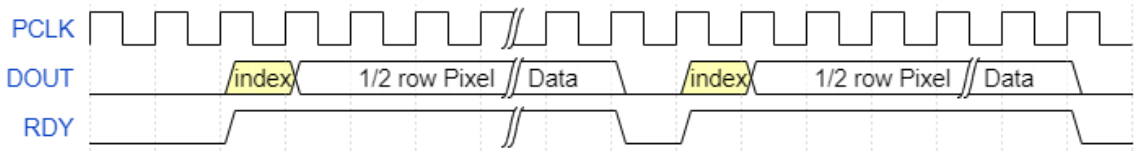

Figure 4 - Event Mode output timing

The index contains:

- The half-row index (0 for left, 1 for right) on DOUT09.
- The row number on DOUT08-DOUT00.

The output manager also performs the following if configured:

- AEX (Auto Exposure) functionality.
- Moving Average.

Serial Interface

The serial interface is used for programming the NSI9000 device and setting up the operational modes and the timing of the internal pixel control signals. The serial interface also allows reading the NSI9000 configuration. When the “I2C_SELECT” pin is driven low, the chosen protocol will be the synchronous serial interface which uses 3 signals: SCLK, SDATA and SENB.

Serial Interface Signals

Signal name	Direction	Description
SENB	IN	Serial Enable: This signal must be asserted for the serial interface to function. The signal allows several NSI9000 devices to share the same SCLK and SDATA lines.
SCLK	IN	Serial interface clock signal
SDATA	IN/OUT	Bidirectional serial address and data line synchronous to SCLK

The protocol uses frames of 32 bits, 15 address bits, one direction bit and 16 data bits. The SDATA signal is sampled and driven by the NSI9000 device on the rising edge of the SCLK signal.

Serial Interface – Write Operation

A write operation starts with driving SENB high. 15 bits of address are sent to the NSI9000 on the SDATA line, MSB first. Direction bit "0", indicating a write operation, follows the address bits. 16 bits of data are sent to the NSI9000 device, MSB first. When SENB is asserted low, the transfer ends.
If SENB goes low in the middle of a transfer, the transfer is terminated and ignored.
Data is latched in the NSI9000 interface on the rising edges of SCLK, so good practice is to drive the data using the falling edges of SCLK.

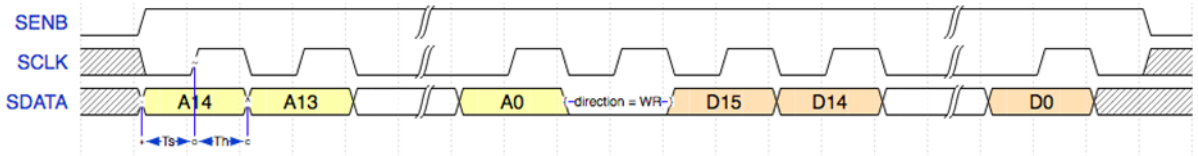

Figure 5 - Serial Interface Write Transaction

Serial Interface – Read Operation

A read operation starts with driving SENB high. 15 bits of address are sent to the NSI9000 on the SDATA line, MSB first. Direction bit "1", indicating a read operation, follows the address bits. The driver releases the SDATA signal, to allow the NSI9000 device to drive the data out of the device. 16 bits of data are read from the NSI9000 device. When SENB is asserted low, the transfer ends.

If SENB goes low in the middle of a transfer, the transfer is terminated and ignored.
Data is driven by the NSI9000 interface on the rising edges of SCLK, so good practice is to sample the data externally using the falling edges of SCLK.

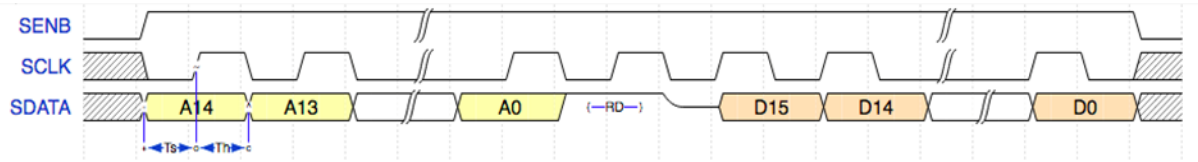

Figure 6 - Serial Interface Read Transaction

Enhanced I²C Interface

The I2C bus protocol was invented in 1982 by Philips Semiconductor, and later enhanced by Texas Instruments. The I2C bus protocol is a Multi-Master/Multi-Slave serial bus, widely used for connecting low speed peripherals to processors and MCUs. The packet size of a standard I2C is 7-bits for address and 8-bits for data, as follows:

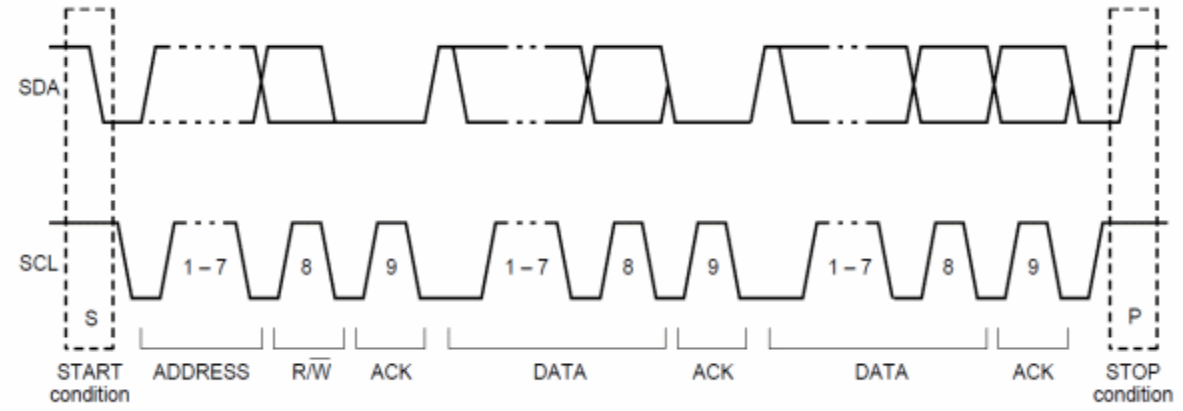

Figure 7 - A complete I2C data transfer (courtesy of NXP semiconductors)

The NSI9000 registers can be configured using the enhanced I2C bus protocol. When the "I2C_SELECT" pin is driven high, the chosen protocol will be the I2C, and the "SCLK" and "SDATA" pins will be used to configure the chip.
The I2C implemented in NSI9000 supports only the enhanced 16-bit data and addresses, by using an encapsulation protocol over the standard I2C.

Standard I2C Write Transaction

The master sends a “start” bit followed by the slave address and a “write” bit (“0”). After receiving an ACK from the slave, the master sends an 8-bit register address. After receiving an ACK from the slave, the master sends the 8-bit data to be written to the register. This transaction can continue with more write operations. The slave increments the address for each data byte received. The sequence ends with the master sending a “stop” bit.

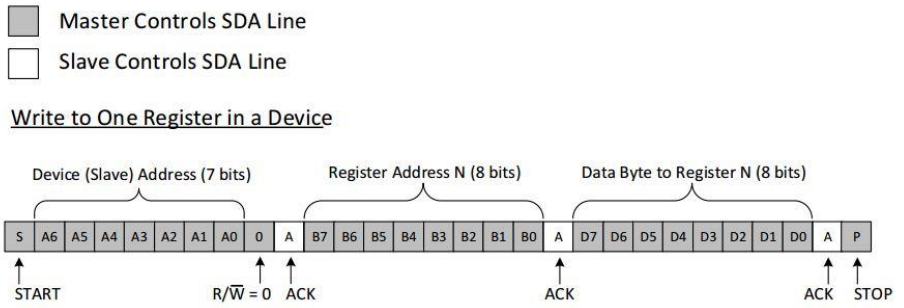

Figure8 - Write transaction to a device register (courtesy of Texas Instruments)

Standard I2C Read Transaction

The master sends a “start” bit followed by the slave address and a “write” bit (“0”). After receiving an ACK from the slave, the master sends an 8-bit register address. After receiving an ACK from the slave, the master sends again a “start” bit followed by the slave address and a “read” bit (“1”). The slave sends the 8-bit data from the register. This transaction can continue with more read operations. The slave increments the address for each data byte transmitted. The sequence ends with the master sending a “NACK” + “stop” bit.

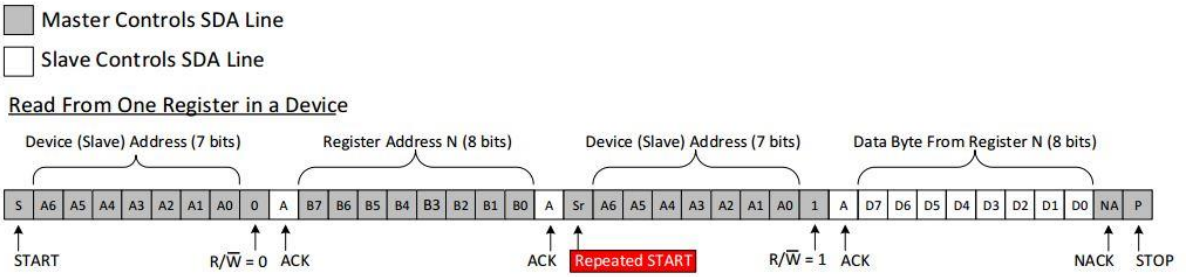

Figure9 - Read transaction to a device register (courtesy of Texas Instruments)

Enhanced I2C Write Transaction

The master sends a “start” bit followed by the NSI9000 address and a “write” bit (“0”). After receiving an ACK from the chip, the master sends the *upper* 8-bit address of the register. After receiving an ACK from the chip, the master – instead of sending the 8-bit data to be written to the register – sends the *lower* 8-bit address of the register, followed by two 8-bit data write transactions.

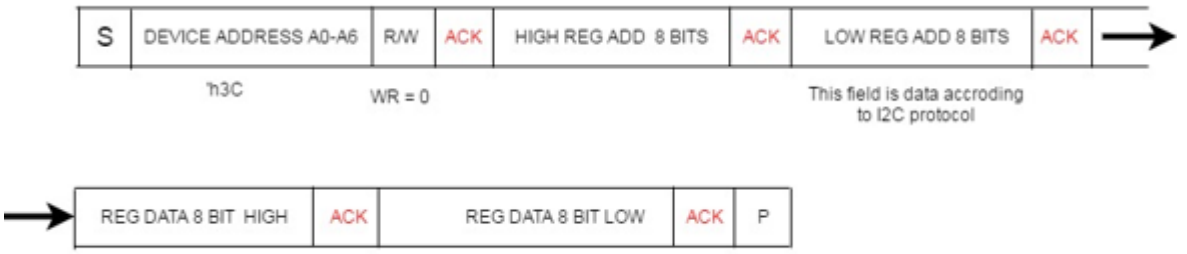

Figure10 - Enhanced I2C Write Transaction

Enhanced I2C Read Transaction

The master sends a “start” bit followed by the NSI9000 address and a “write” bit (“0”). After receiving an ACK from the chip, the master sends the *upper* 8-bit address of the register. After receiving an ACK from the chip, the master sends the *lower* 8-bit address of the register. The master sends again a “start” bit followed by the chip address and a “read” bit (“1”). The chip sends the upper 8-bit data from the addressed register, followed by the lower 8-bit data. The sequence ends with the master sending a “NACK” + “stop” bit.

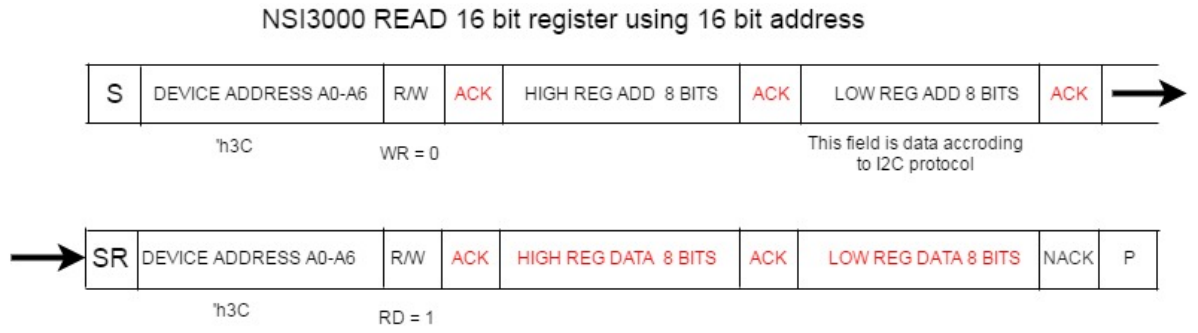

Figure11 - Enhanced 16-bit read transaction from a sensor register

Timing Characteristics

Parameter	Min	Type	Max	Unit
MCLK – Operating frequency			100	MHz
SCLK – Serial input clock frequency	MCLK/8			MHz
SDATA, SENB setup time (before SCLK)			4	ns
SDATA, SENB hold time (after SCLK)	0.5			ns
SDATA delay (after SCLK)			4	ns
DOUT delay (after PCLK)			3	ns
RDY delay (after PCLK)			3	ns
VSYNC delay (after PCLK)			3	ns

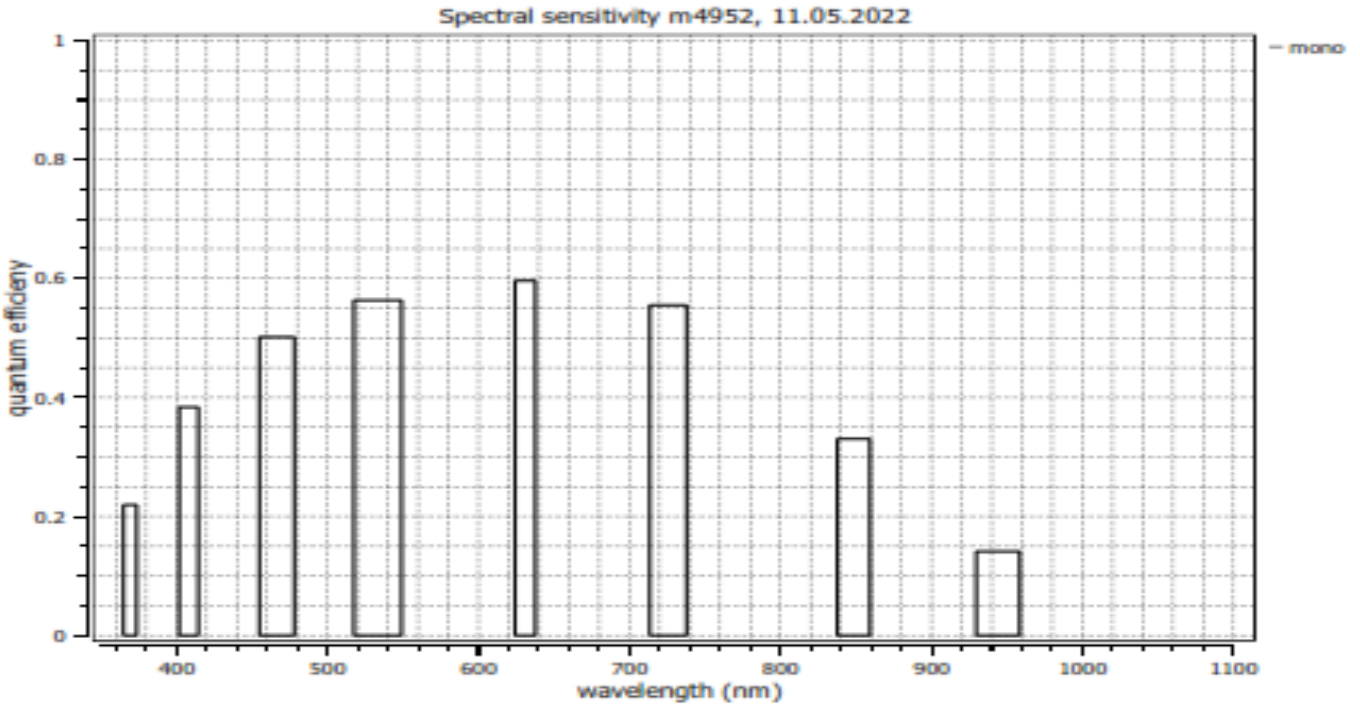

Figure12 - Technology measured QE (Tower 180n)