

# NSS40300MDR2G

## Dual Matched 40 V, 6.0 A, Low $V_{CE(sat)}$ PNP Transistor

These transistors are part of the ON Semiconductor e<sup>2</sup>PowerEdge family of Low  $V_{CE(sat)}$  transistors. They are assembled to create a pair of devices highly matched in all parameters, including ultra low saturation voltage  $V_{CE(sat)}$ , high current gain and Base/Emitter turn on voltage.

Typical applications are current mirrors, differential amplifiers, DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

### Features

- Current Gain Matching to 10%
- Base Emitter Voltage Matched to 2 mV
- This is a Pb-Free Device

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	-40	Vdc
Collector-Base Voltage	$V_{CBO}$	-40	Vdc
Emitter-Base Voltage	$V_{EBO}$	-7.0	Vdc
Collector Current - Continuous	$I_C$	-3.0	A
Collector Current - Peak	$I_{CM}$	-6.0	A
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

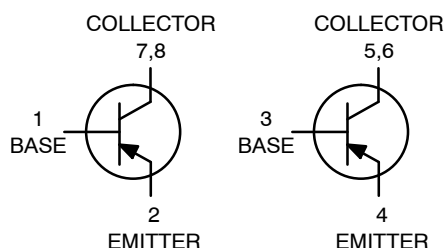
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



ON Semiconductor®

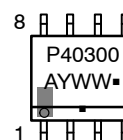
<http://onsemi.com>

**40 VOLTS**  
**6.0 AMPS**  
**PNP LOW  $V_{CE(sat)}$  TRANSISTOR**  
**EQUIVALENT  $R_{DS(on)}$  80 mΩ**



SOIC-8  
CASE 751  
STYLE 29

### DEVICE MARKING



P40300 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NSS40300MDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSS40300MDR2G

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
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### SINGLE HEATED

Total Device Dissipation (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	576	mW
		4.6	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	217	$^\circ\text{C}/\text{W}$
Total Device Dissipation (Note 2) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	676	mW
		5.4	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	185	$^\circ\text{C}/\text{W}$

### DUAL HEATED (Note 3)

Total Device Dissipation (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	653	mW
		5.2	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	191	$^\circ\text{C}/\text{W}$
Total Device Dissipation (Note 2) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	783	mW
		6.3	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	160	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ 10 mm<sup>2</sup>, 1 oz. copper traces, still air.
2. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.
3. Dual heated values assume total power is the sum of two equally powered devices.

# NSS40300MDR2G

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage (I <sub>C</sub> = -10 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	-40	-	-	Vdc
Collector–Base Breakdown Voltage (I <sub>C</sub> = -0.1 mA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	-40	-	-	Vdc
Emitter–Base Breakdown Voltage (I <sub>E</sub> = -0.1 mA, I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	-7.0	-	-	Vdc
Collector Cutoff Current (V <sub>CB</sub> = -40 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	-	-0.1	μAdc
Emitter Cutoff Current (V <sub>EB</sub> = -6.0 Vdc)	I <sub>EBO</sub>	-	-	-0.1	μAdc

### ON CHARACTERISTICS

DC Current Gain (Note 4) (I <sub>C</sub> = -10 mA, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -500 mA, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -1.0 A, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -2.0 A, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -2.0 A, V <sub>CE</sub> = -2.0 V) (Note 5)	h <sub>FE</sub>     h <sub>FE(1)</sub> /h <sub>FE(2)</sub>	 250 220 180 150 0.9	 380 340 300 230 0.99	 - - - - -	     
Collector–Emitter Saturation Voltage (Note 4) (I <sub>C</sub> = -0.1 A, I <sub>B</sub> = -0.010 A) (I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.100 A) (I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.010 A) (I <sub>C</sub> = -2.0 A, I <sub>B</sub> = -0.200 A)	V <sub>CE(sat)</sub>	 - - - -	 -0.013 -0.075 -0.130 -0.135	 -0.017 -0.095 -0.170 -0.170	 V    
Base–Emitter Saturation Voltage (Note 4) (I <sub>C</sub> = -1.0 A, I <sub>B</sub> = -0.01 A)	V <sub>BE(sat)</sub>	-	-0.780	-0.900	V
Base–Emitter Turn–on Voltage (Note 4) (I <sub>C</sub> = -0.1 A, V <sub>CE</sub> = -2.0 V) (I <sub>C</sub> = -0.1 A, V <sub>CE</sub> = -2.0 V) (Note 6)	V <sub>BE(on)</sub>  V <sub>BE(1)</sub> - V <sub>BE(2)</sub>	 - -	 -0.660 0.3	 -0.750 2.0	 V mV
Cutoff Frequency (I <sub>C</sub> = -100 mA, V <sub>CE</sub> = -5.0 V, f = 100 MHz)	f <sub>T</sub>	100	-	-	MHz
Input Capacitance (V <sub>EB</sub> = -0.5 V, f = 1.0 MHz)	C <sub>ibo</sub>	-	250	300	pF
Output Capacitance (V <sub>CB</sub> = -3.0 V, f = 1.0 MHz)	C <sub>obo</sub>	-	50	65	pF

### SWITCHING CHARACTERISTICS

Delay (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA)	t <sub>d</sub>	-	-	60	ns
Rise (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA)	t <sub>r</sub>	-	-	120	ns
Storage (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA)	t <sub>s</sub>	-	-	400	ns
Fall (V <sub>CC</sub> = -30 V, I <sub>C</sub> = -750 mA, I <sub>B1</sub> = -15 mA)	t <sub>f</sub>	-	-	130	ns

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

5. h<sub>FE(1)</sub>/h<sub>FE(2)</sub> is the ratio of one transistor compared to the other transistor within the same package. The smaller h<sub>FE</sub> is used as numerator.

6. V<sub>BE(1)</sub> - V<sub>BE(2)</sub> is the absolute difference of one transistor compared to the other transistor within the same package.

TYPICAL CHARACTERISTICS

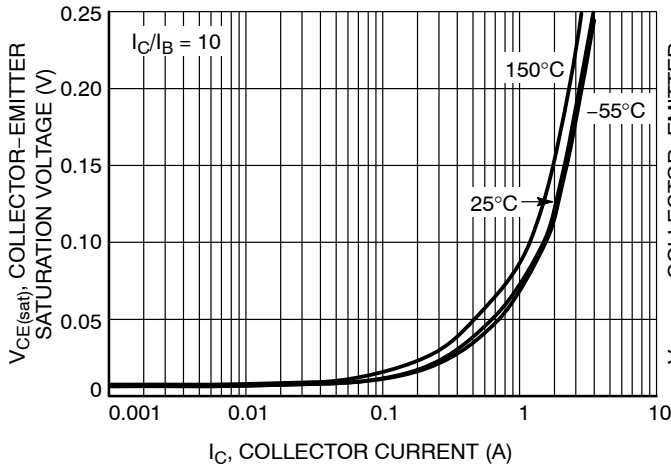


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

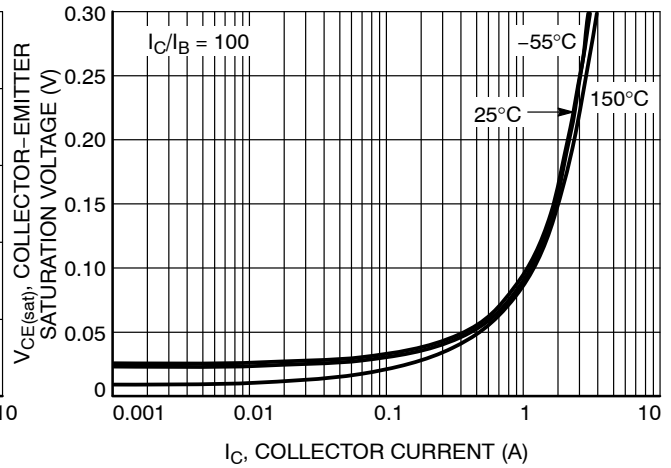


Figure 2. Collector Emitter Saturation Voltage vs. Collector Current

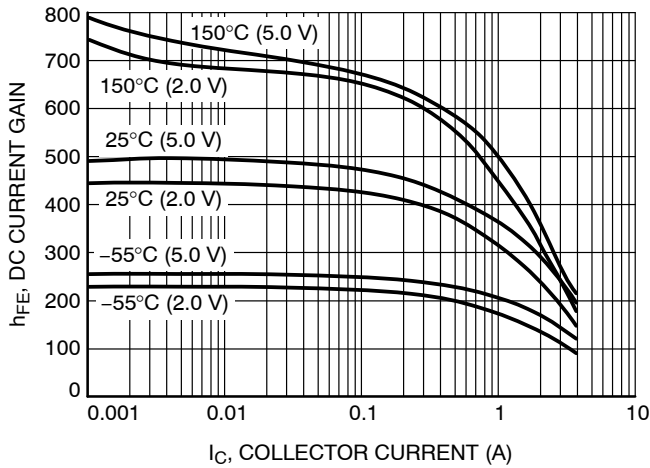


Figure 3. DC Current Gain vs. Collector Current

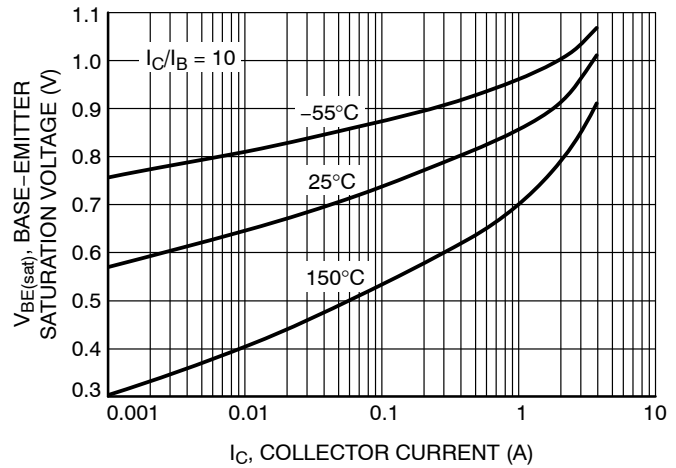


Figure 4. Base Emitter Saturation Voltage vs. Collector Current

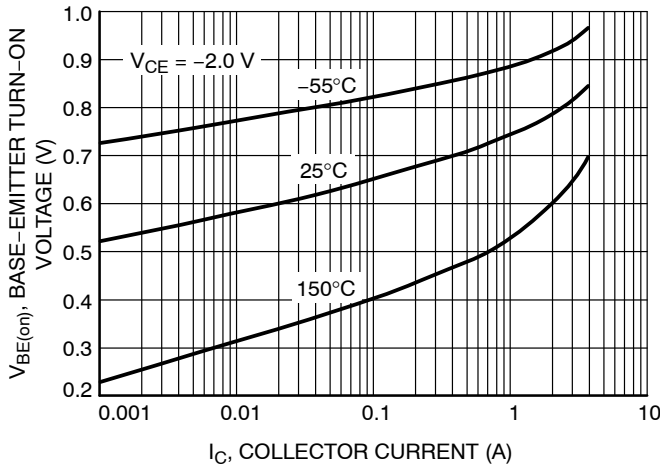


Figure 5. Base Emitter Turn-On Voltage vs. Collector Current

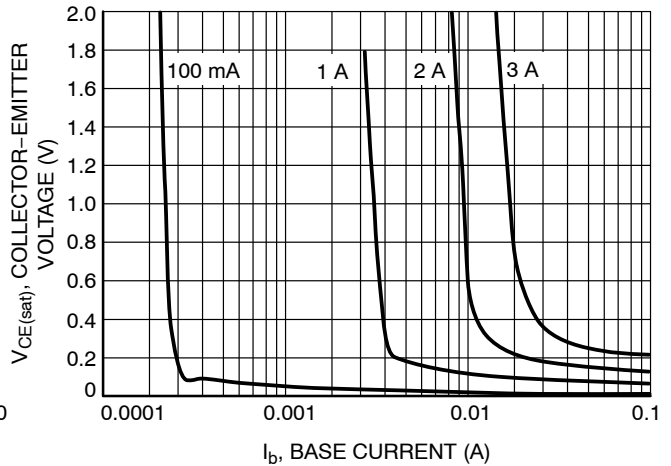
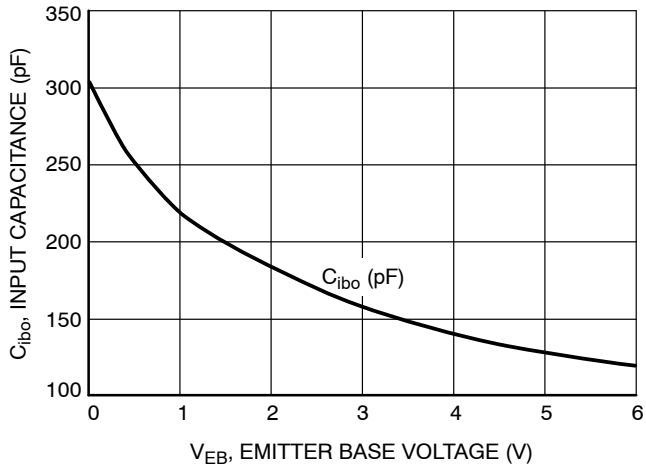


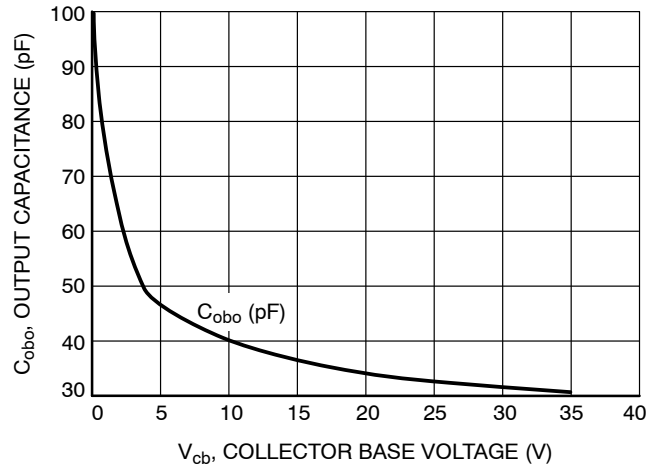
Figure 6. Saturation Region

# NSS40300MDR2G

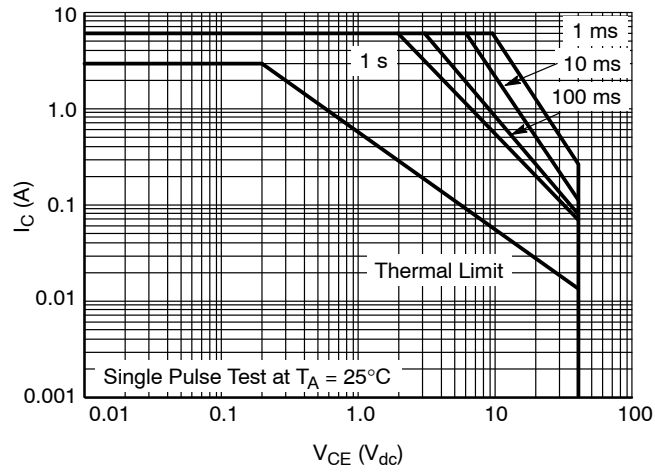
## TYPICAL CHARACTERISTICS



**Figure 7. Input Capacitance**



**Figure 8. Output Capacitance**

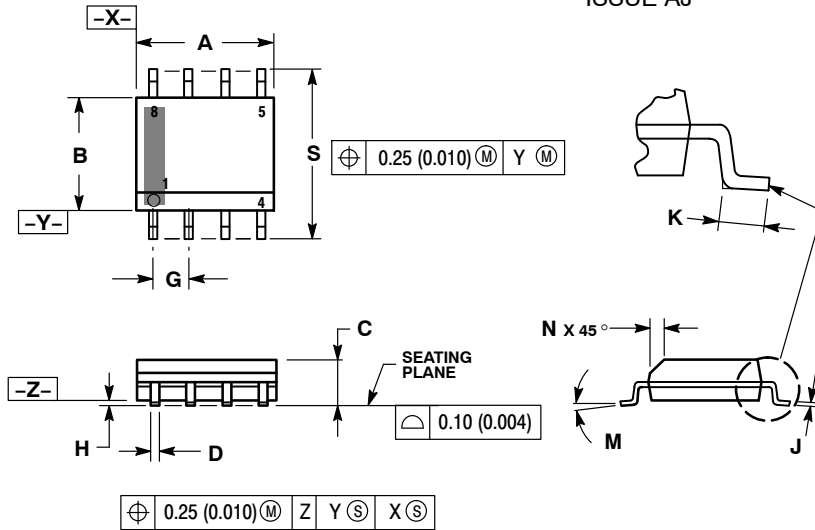


**Figure 9. Safe Operating Area**

# NSS40300MDR2G

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AJ

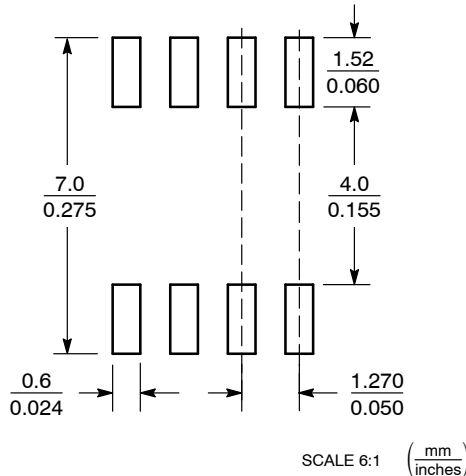


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



**STYLE 29:**

- PIN 1. BASE, DIE #1
- EMITTER, #1
- BASE, #2
- EMITTER, #2
- COLLECTOR, #2
- COLLECTOR, #1
- COLLECTOR, #1
- COLLECTOR, #1

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NSS40300MD/D