NST103

Low-Power Temperature Sensor with SMBus and I²C Interface

Datasheet (EN) 1.2

Product Overview

The NST103 is a 1.5V to 3.6V micropower digital temperature sensor with a 1°C resolution. The device is specified at the full temperature range of -40 °C to 125 °C.

The NST103 communicates through a flexible 2-wire digital interface which is compatible with SMBus and I²C and supports 8 device addresses. The device offers a typical accuracy of 1°C, it is highly linear and does not require complex calculations or lookup tables to derive temperature.

NST103 has a four-ball wafer chip-scale package (DABGA), making it suitable for on-board and off-line applications in the automotive, industrial, and consumer markets. applications in the IoT.

Key Features

- High Accuracy over – 40 °C to 125 °C
  - -10 °C ~ 100 °C: 1°C (Typ)
  - -40 °C ~ 125 °C: 3°C (Max)
- Supports up to 8 Device Addresses
- Supply Operation Range from 1.5V to 3.6V
- Operating Current: 3μA (Typ) at 0.25Hz Conversion Cycle
- Shutdown Current: 1.0 μA (Typ)
- Digital Interface: SMBus, I²C
- 4-Ball WCSP (DSBGA) Package

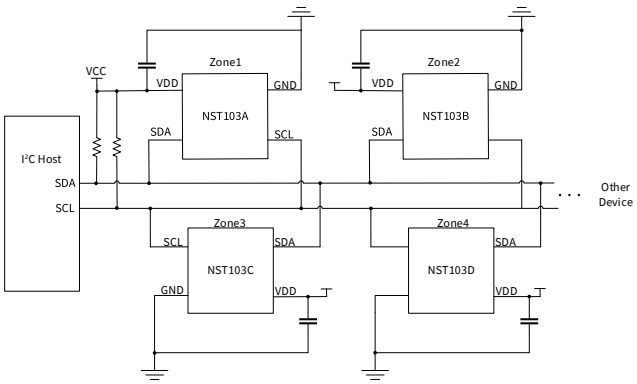
Applications

- Computer Peripheral Thermal Protection
- Industrial Internet of Things (IoT)
- Notebook Computers
- Mobile Phone
- Solid State Disk
- Servers
- Set Top Boxes
- Low Power Environmental
- Sensors

Device Information

Part Number	*Package*	*Body Size*
NST103x-CWLR	DSBGA (4)	0.75mm × 0.75mm

Typical Application



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1. PIN CONFIGURATION AND FUNCTIONS

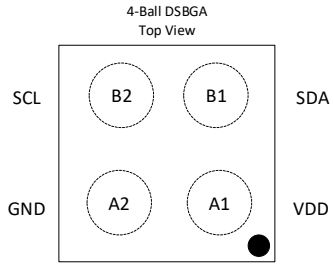

Figure 1.1 NST103 Package

Table 1.1 NST103 Pin Configuration and Description

Pin No.	*Symbol*	*Type*	*Function*
A1	VDD	Power	Supply voltage, 1.5 V to 3.6 V
A2	GND	GND	Ground
B1	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.
B2	SCL	I	Serial clock; requires a pullup resistor.

2. ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage Pin (VDD)	VDD	-0.3		3.6	V	
Voltage at SCL and SDA Pins	SCL, SDA	-0.3		(VDD + 0.3) and ≤ 3.6	V	
Storage Temperature	T_{stg}	-60		150	°C	
Operation Temperature	$TB_{operation}$	-55		150	°C	
Maximum Junction Temperature				150	°C	
ESD Susceptibility	HBM	±5			KV	
Maximum Surge Isolation Voltage	CDM	±2			KV	

3. RECOMMENDED OPERATING CONDITIONS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD	1.5		3.6	V	
Operation Temperature Range	T_A	-40		125	℃	

4. SPECIFICATIONS

4.1. Electrical Characteristics

At T_A = +25°C and VDD = +1.5V to +3.6V, unless otherwise noted.

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply						
Supply Voltage Range	VDD	1.5	3.3	3.6	V	
Operation Current	I_{CONV}		30		μA	
Shutdown Current	ISD		0.5	1	μA	Serial bus inactive
			10		μA	Serial bus active, SCL frequency = 400 kHz
Temperature Range and Resolution						
Temperature Range		-40		125	° C	
Resolution			1		°C	
Accuracy		-2	±1	2	°C	from -10°C to 100°C
		-3	±1	3	°C	from -40°C to 125°C
Conversion Time	T_{CONV}		26	35	ms	
Time out Time	$T_{TIMEOUT}$		30	40	ms	
Thermal Response						
Thermal Response Time			0.12		s	Stirred oil thermal response time to 63% of final value
Drift						
Drift				1	LSB	

4.2. I²C Timing Characteristics

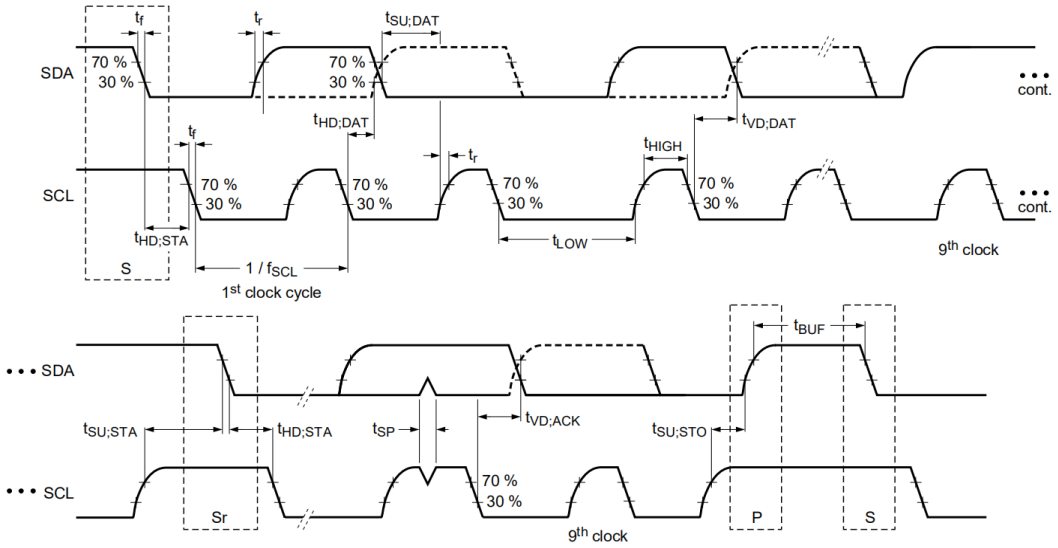

Figure 4.1 Two-Wire Timing Diagram

Parameters	Symbol	FAST MODE		HIGH-SPEED MODE		Unit	Comments
SCL Operating Frequency	f_{SCL}	0.001	0.4	0.001	2.8	MHz	
Bus-free Time	t_{BUF}	1300		160		ns	Between STOP and START Conditions
Hold Time after Repeated START Condition	t_{HDSTA}	600		160		ns	After This Period, The First Clock Is Generated
Repeated START Condition Setup Time	t_{SUSTA}	600		160		ns	
Setup Time	t_{SUSTO}	600		160		ns	STOP Condition
Data Hold Time	t_{HDDAT}	100	900	25	105	ns	
Data Setup Time	t_{SUDAT}	100		25		ns	
SCL Clock Low Period	t_{LOW}	1300		210		ns	
SCL Clock High Period	t_{HIGH}	600		60		ns	
Data Fall Time	t_{FD}		300		80	ns	
Data Rise Time	t_{RD}		300			ns	
			1000			ns	SCLK ≤ 100 kHz
Clock Fall Time	t_{FC}		300		40	ns	
Clock Rise Time	t_{RC}		300		40	ns	

The NST103 of temperature sensor are SMBus, and I²C interface-compatible. The device support various operations as Table 4.1. The following list provides bus definitions. Parameters for Figure 4.1 are defined in the Timing Requirements. Bus definitions are:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A high-to-low transition of SDA with SCL high is a START condition which must precede any other command (see Figure 4.1).

Stop Data Transfer: A low-to-high transition of SDA with SCL high is a STOP condition. The termination of each data transfer can be done with a RESTART or STOP.

Data Transfer: The amount of data bytes transferred between START and STOP is controlled by the master and is unlimited. The receiver acknowledges the transfer of data.

Acknowledge: All addresses and data words are serially transmitted to and from the device in 8-bit words. The device sends a zero to acknowledge that it has received each word when the address is matched. This happens during the ninth clock cycle. The data transfer can be terminated by the host generating a not-acknowledge during the host receiving data.

Table 4.1 NST103 I²C operations

NO	I²C Operations	Figures
1	Two-Wire Timing Diagram for Read Byte Format	Figure 4.2
2	Two-Wire Timing Diagram for Write Byte Format	Figure 4.3
3	Two-Wire Timing Diagram MDA Read Byte Format	Figure 4.4
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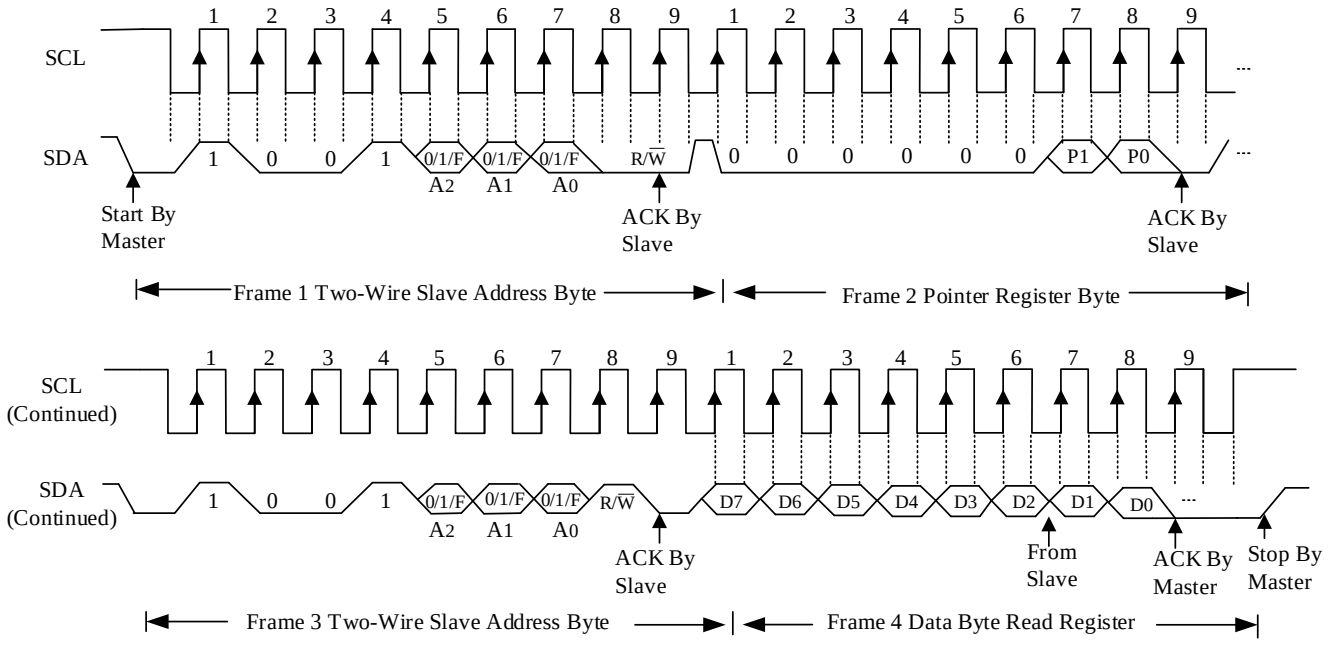


Figure 4.2 Two-Wire Timing Diagram for Read Byte Format

(1) Slave address 1110xxx is shown. see Table 5.3.

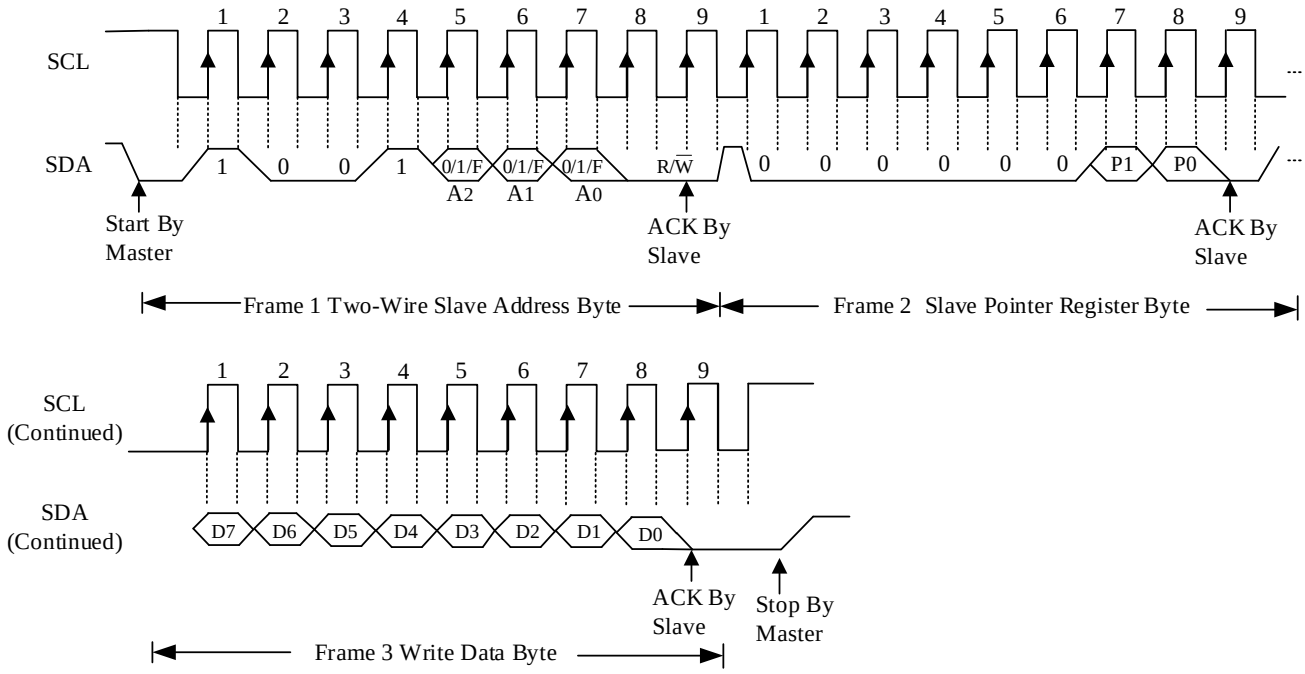


Figure 4.3 Two-Wire Timing Diagram for Write Byte Format

(2) Slave address 1110xxx is shown. see Table 5.3.

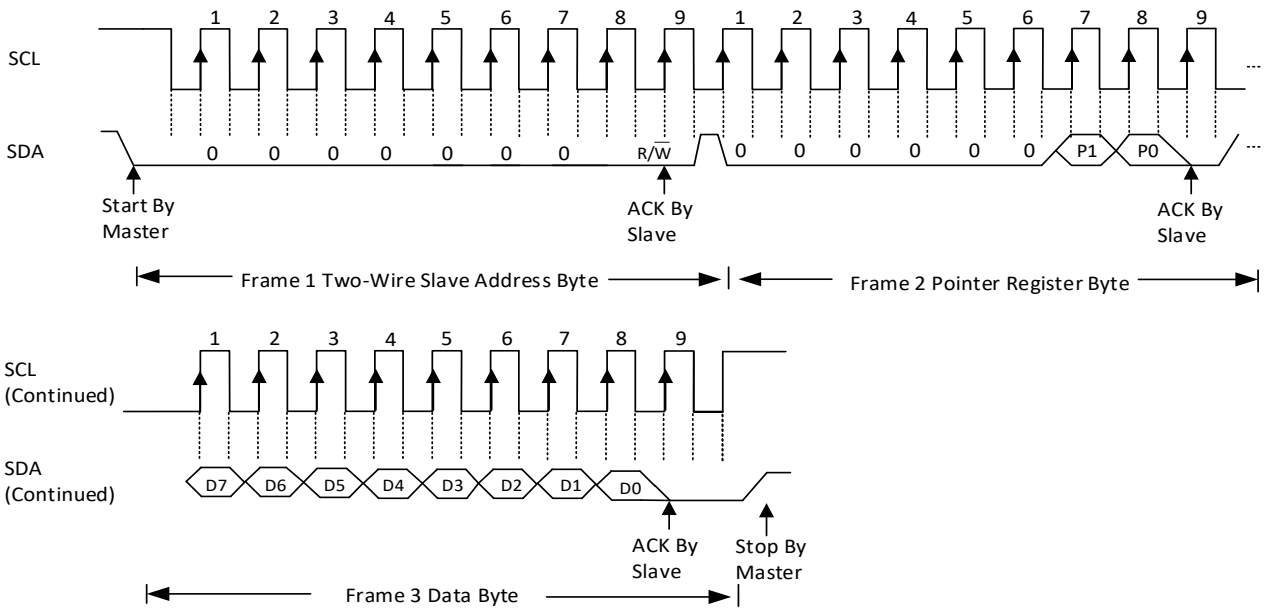


Figure 4.4 Two-Wire Timing Diagram MDA Read Byte Format

(1) All NST103 devices on the bus acknowledge the byte.

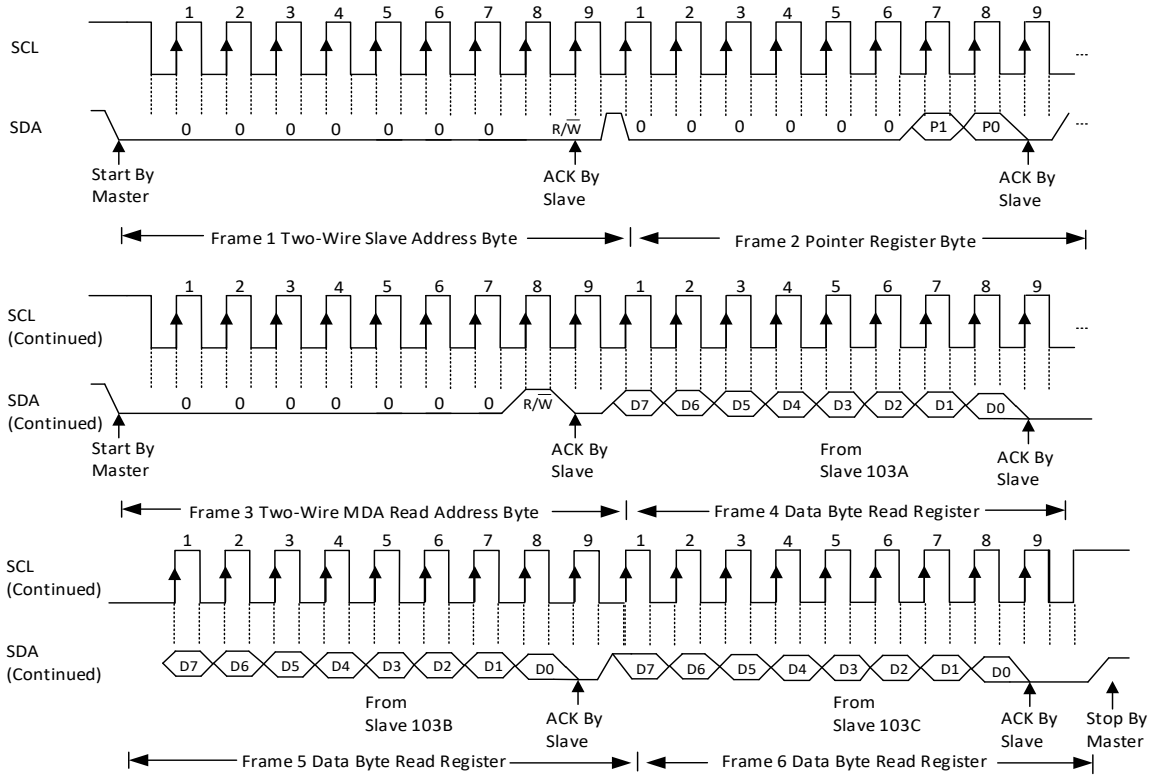


Figure 4.5 Two-Wire Timing Diagram MDA Write Byte Format Using Figure 8.1 (Typical Application)

(1) All NST103 devices on the bus acknowledge the byte.

(2) The master must issue an acknowledge for each byte read to read all of the NST103 devices on the bus.

(3) Three NST103 devices used in this case; up to eight devices can be used (see Table 5.3).

5. FUNCTION DESCRIPTION

5.1. Overview

The NST103 is a 1.5V to 3.6V micropower digital temperature sensor and include a PNP-BJT type temperature sensor and 12-bit ADC (∑-ΔADC). The device is specified at the full temperature range of -40 °C to 125 °C with a 1°C resolution.

The NST103 communicates through a flexible 2-wire digital interface which is compatible with SMBus and I^2C and supports 8 device addresses. The serial interface offers multiple device access (MDA) commands that Support the host to synchronously multi-point temperature data.

NST103 has a four-ball wafer chip-scale package (DABGA), making it suitable for on-board and off-line applications in the automotive, industrial, and consumer markets. applications in the IoT.

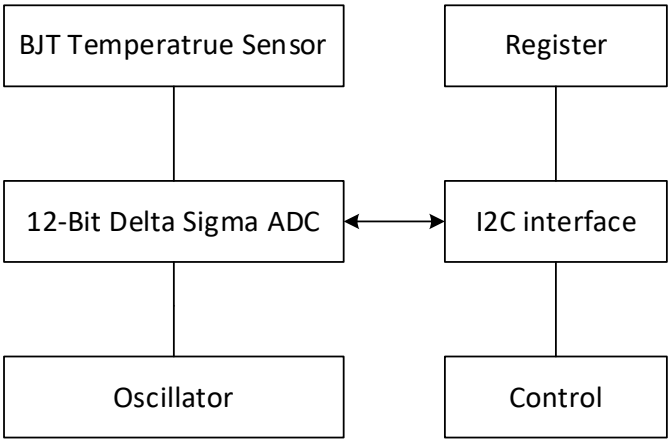


Figure 5.1 NST103 Functional Block Diagram

5.2. Digital Functionality

5.2.1. Continuous Conversion Mode

The default mode of the NST103 after power-up is continuous conversion mode. In continuous conversion mode, the ADC performs temperature conversions continuously and saves the result of each conversion to the temperature register, overwriting the result of the previous conversion.

As soon as the NST103 is powered up or a general call reset is completed, a temperature transition is immediately performed, as shown in Figure 5.2. The time for each temperature transition is 26ms (typical). The current during temperature conversion is 30μA (+25°C typically). The current of delay during two conversions is 1μA (+25 °C typically).

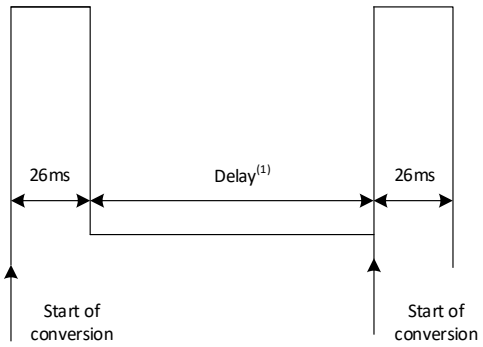


Figure 5.2 Conversion Start

(1) Delay is set by CR1 and CR0.

(2) The NST103 device provides four conversion rates, which are controlled by CR1 and CR0 in the configuration register, the default conversion rate is 0.25Hz. Table 5.1 shows the conversion rates corresponding to the configuration of CR1 and CR0.

Table 5.1. Conversion Rate Settings

CR1	*CR0*	*Conversion Rate*
0	0	0.25 Hz (default)
0	1	1 Hz
1	0	4 Hz
1	1	8 Hz

5.2.2. Shutdown Mode

For power-sensitive applications, the NST103 offers a low-power shutdown mode. M1 and M0 bits in the configuration register controls shutdown mode. When M1 and M0 are changed to '00' as Table 5.2 shows, the conversion in progress will be completed and the result stored in the temperature register, after which the NST103 will go into a low-power standby state. The 2-wire digital interface remains operational in shutdown. In this mode, the typical power consumption is only 0.5μA.

Table 5.2. Mode Settings

M1	*M0*	*Mode*
0	0	Shutdown Mode
0	1	One-Shot Mode
1	0	Continuous Mode

5.2.3. One-Shot Mode

The NST103 supports a one-shot temperature measurement mode when continuous temperature monitoring is not required. First set the chip into shutdown mode, and then write ‘01’ to bits M1 and M0 to wake up the chip once and perform a temperature conversion. When temperature conversion is in progress, M1 and M0 bit is ‘01’. After the single conversion is complete, the device returns to the Shutdown state. At the end of the conversion, the M1 and M0 bit reads ‘00’.

Using one-shot mode can achieve faster conversion frequency, temperature conversion takes 26ms typically, however, reading the temperature value needs less than 20us. Therefore, using the one-shot mode can achieve 30 times faster than the fastest temperature conversion rate in the continuous mode.

5.2.4. Temperature Watchdog Function

The NST103 has a watchdog function, which can monitor the device temperature and compare the temperature results with the values set in the temperature limit registers (T_{HIGH} and T_{LOW}) to monitor whether the device temperature is within these set limits. As long as the temperature value detected by NST103 is higher than the value set in the T_{HIGH} register, the flag high bit (FH) of the configuration register is set to 1. As long as the detected temperature value is lower than the value in the T_{LOW} register, the flag low bit (FL) is set to 1. If both the high and low flag bits are 0, the temperature is between the temperature range set by the temperature limit register, which can be shown in Figure 5.3.

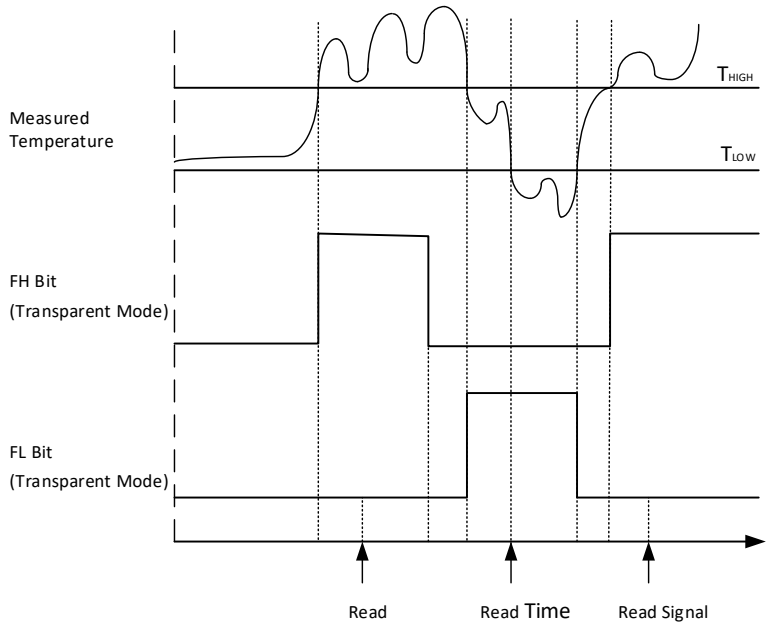


Figure 5.3 Temperature Flag Functional Diagram

5.3. I²C Interface

NST103 is compatible with SMBus and I²C interfaces, and transmits information to the master. NST103 has eight slave addresses, which can support the simultaneous use of four NST103 slaves on the bus, data on the I²C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 2.8 Mbit/s in the High-speed mode. All data bytes are transferred MSB-firstly.

5.3.1. I²C Bus Address

NST103 has eight versions, each version has unique address byte, includes 7 bits address and 1 read / write direction bit. as shown in Table 5.3. These addresses can be used as position or temperature zone indicators.

Table 5.3. Device Slave Addresses

Product	*Slave Address*	*Slave*	*Zone*
NST103A	1110000	0x70	Zone1
NST103B	1110001	0x71	Zone2
NST103C	1110010	0x72	Zone3
NST103D	1110011	0x73	Zone4
NST103E	1110100	0x74	Zone5
NST103F	1110101	0x75	Zone6
NST103G	1110110	0x76	Zone7
NST103H	1110111	0x77	Zone8

5.3.2. Writing and Reading Operation

Writing operation is triggered by sending the slave address in write mode (R/W=0), then the master sends pointer register, and send the data byte afterwards. The transaction is ended by a STOP condition. The details of this sequence are shown in Figure 4.1.

During writing operation, NST103 is used as the slave receiver. The master transfers the slave address byte firstly, including 7 address bits and 1bit write direction bits, NST103 acknowledges after receiving the valid address. the second byte transmitted by master is the pointer register address, then NST103 acknowledges and the next byte of data is written to the pointer register. The master can terminate communication by generating a STOP condition. The details of this sequence are shown in Figure 4.3.

To be able to read registers, firstly the register address must be sent in write mode (R/W=0), then either a stop or a repeated start condition must be generated. When the slave is addressed as read mode (R/W=1), then the slave sends out 1 byte data. After reading the data the master needs to generate the NACK and stop condition to end the transaction. The details of this sequence are shown in Figure 4.2.

If repeated reads from the same register are required, it is not necessary to send the pointer register byte repeatedly because the NST103 remembers the pointer register value until it is changed by the next write operation.

5.3.3. High-Speed (Hs) Mode

The NST103 supports bus operation above 400 kHz, requiring that the master device must switch the bus to high-speed mode operation by issuing a high-speed mode master code (00001XXX) in the first byte after the START condition. The NST103 does not acknowledge this byte, the NST103 switches the input filter of SCL, SDA and output filter of SDA to high-speed mode, allowing data transfer up to 2.8 MHz. After issuing the master code for high-speed mode, the master will transmit a two-wire slave address to initiate the data transfer operation. The bus will continue to operate in high-speed mode until a stop signal appears on the bus. Once the stop signal is received, the SCL, SDA input filter and SDA output filter of the NST103 switch to the fast mode.

5.3.4. General Call

The NST103 provides the general call function. when the general call address (0 000 000) sent by host is received and the R/W bit is 0, the device replies to the command. If the second byte is 00000110, the NST103 latches the state of its address pins and resets its internal registers to the value at power-up.

5.3.5. I^2C Timeout

The NST103 resets the I^2C interface when the SCL or SDA is continuously pulled low for 30ms (typical) between the START and STOP signals, the NST103 release the SDA and SCL line and waits for the master to initiate a START condition. To avoid activating the timeout function, the SCL operating frequency must be maintained at a rate of at least 1kHz.

5.3.6. Multiple Device Access

The NST103 supports Multiple Device Access (MDA). On the same I^2C bus, the master can communicate with multiple NST103 devices. The MDA command include the MDA read address (00000001) and the MDA write address (00000000), and NST103 responds the MDA command. On the same I^2C bus, NST103 with the same I^2C address cannot be used, otherwise, MDA cannot work normally, see Table 5.3.

5.3.6.1. Multiple Device Access Write

The master send the MDA read command on the I^2C bus, then send the register of the pointer of NST103. All of the NST103 will ack the command, and the next data byte will be written to the registers. When the NST103 receives the data byte, they store and acknowledge the transmitted byte. All the NST103 devices will store the data byte; see Figure 4.5.

5.3.6.2. Multiple Device Access Read

In the MDA read transaction, the master sends the MDA write command on the I^2C bus, then send the register of the pointer of NST103.Then the master sends the MDA read command, all the NST103 will ack the command successively. The NST103 will send the data on the I^2C bus, in the order of NST103A to NST103H.The master must ack each byte of data. Otherwise, the communication will be terminated. Up to eight NST103 devices can be on the same bus and respond to MDA commands; see Table 5.3.

5.4. ON-CHIP Registers

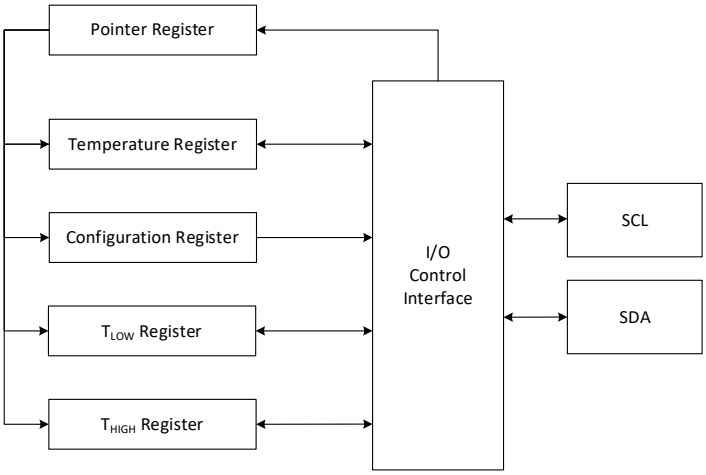


Figure 5.4 On-chip Register Structure

5.4.1. Pointer Register

Figure 5.4 shows the on-chip register structure of the NST103. The Pointer Register of the device is used to address a given data register. As Table 5.4, The Pointer Register uses the two bits to identify which of the data registers should respond to a read or write command. During a write command, P2 through P7 must always be 0. Table 5.5 shows the data registers are pointed to by the pointer register in four cases of P1-P0. After power on reset, the default value of the pointer register is 0, pointing to the temperature register.

Table 5.4. Pointer Register Byte

P7	*P6*	*P5*	*P4*	*P3*	*P2*	*P1*	*P0*
0	0	0	0	0	0	Pointer Addresses	

Table 5.5. Pointer Addresses

P1	*P0*	*TYPE*	*REGISTER*
0	0	R only default	Temperature register
0	1	R/W	Configuration register
1	0	R/W	T_{LOW} register
1	1	R/W	T_{HIGH} register

5.4.2. Temperature Register

The read-only register for storing the results of each completed temperature conversion, which consists of 1bytes in the format shown in Table 5.6. Read Temperature operations is performed MSB firstly. Following power up or reset, the temperature register reads 0°C until the first conversion is completed. The NST103 output 8 bits of data in binary format, 1 LSB equals 1°C. A positive full-scale input produces an output code of 7Fh and the negative full-scale input exceeds -40°C, for example, the output code of C9h corresponding to -55°C, but the accuracy lower than -40°C is not guaranteed. Table 5.7 summarizes the ideal output codes for different input temperature.

Table 5.6 Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	T2	T1	T0

Table 5.7 8-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111	7F
127	0111 1111	7F
100	0110 0100	64
80	0101 0000	50
75	0100 1011	4B
50	0011 0010	32
25	0001 1001	19
0	0000 0000	00
-1	1111 1111	FF
-25	1110 0111	E7
-55	1100 1001	C9

For positive temperatures (for example, 25°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code, left-justified format. Denote a positive number with MSB = 0.

Example: (25°C)/(1°C/count) = 25 = 19h = 0001 1001

For negative temperatures (for example, -25°C):

Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = 1.

Example: (| – 25°C|)/(1°C/count) = 25 = 19h = 0001 1001

Twos complement format: 1110 0110 + 1 = 1110 0111

5.4.3. Configuration Register

The configuration register of the NST103 is an 8-bit read and write register used to store the control bits which can control the NST103 into different operation modes, the read and write operation is executed with MSB priority. Table 5.8 lists the configuration register format, power-up and reset values. All registers are updated byte by byte.

Table 5.8 Configuration and Power-Up and Reset Format

D7	D6	D5	D4	D3	D2	D1	D0
ID	CR1	CR0	FH	FL	NA	M1	M0
0	0	0	0	0	0	1	0

5.4.4. Temperature Limit Registers

The temperature limit values in the T_{HIGH} and T_{LOW} registers have the same format as the temperature values in the temperature registers, see Table 5.7. Table 5.9 and Table 5.10 describe the format for the T_{HIGH} and T_{LOW} registers. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 60°C and T_{LOW} = – 10°C.

Table 5.9 T_{LOW} Register

D7	D6	D5	D4	D3	D2	D1	D0
L7	L6	L5	L4	L3	L2	L1	L0
1	1	1	1	0	1	1	0

Table 5.10 T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0
0	0	1	1	1	1	0	0

6. APPLICATION NOTE

6.1. Noise Reduction

The NST103 is a micropower digital temperature sensor which lead to very low noise on the supply bus. Applying an RC filter to the VDD pin of the NST103 can further reduce any noise which can influence the performance of NST103. R_F in Figure 6.1 should be less than 5kΩ and C_F should be greater than 10nF.

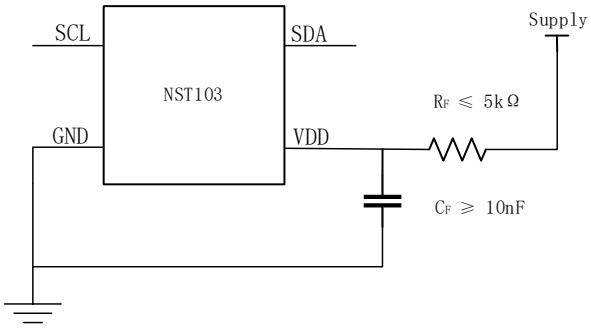


Figure 6.1 Noise Reduction

6.2. Typical Application Circuit

The NST103 is compatible with both SMBus and I²C interfaces. The NST103 has eight slave addresses, allowing up to eight NST103 devices on one bus. Although a bypass capacitor of 0.01μF is recommended. The sensing device for the NST103 device is the device itself. The thermal path is through the solder pads as well as the package. The low thermal resistance of the metal results in the pads providing the primary thermal path.

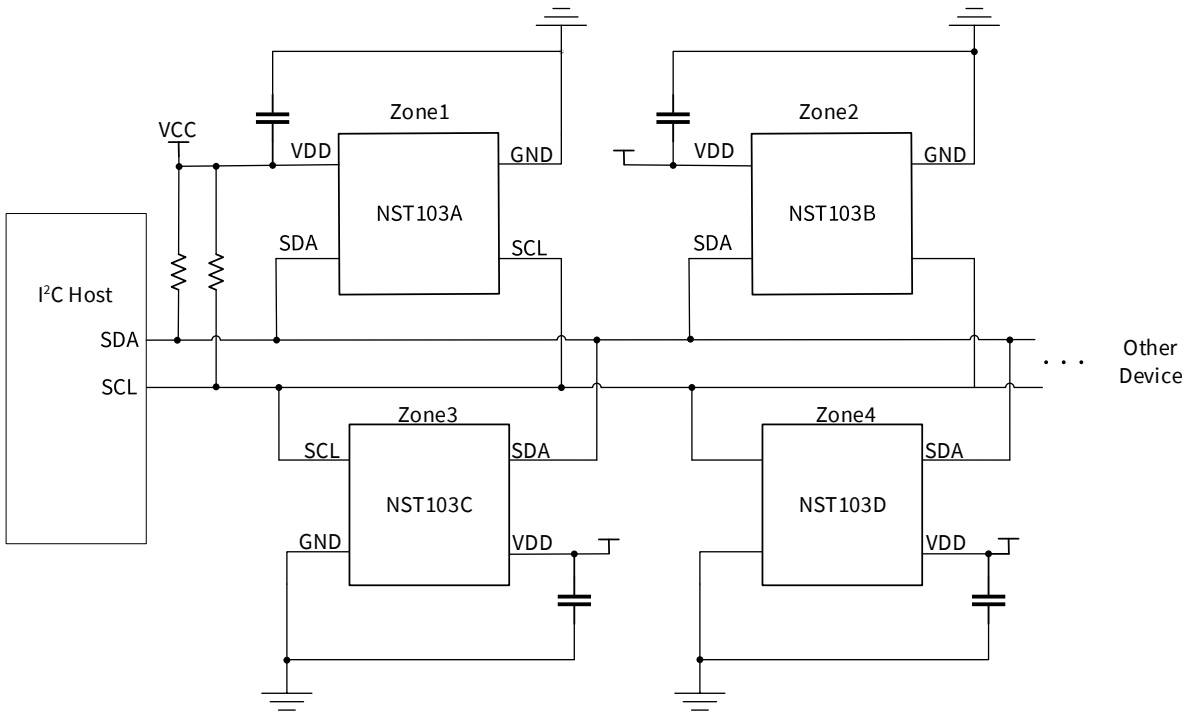
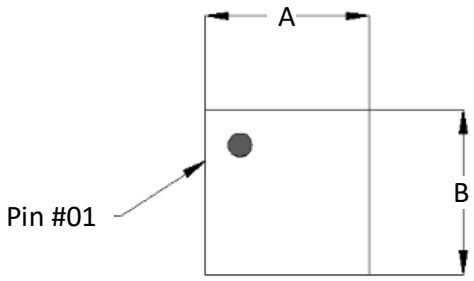
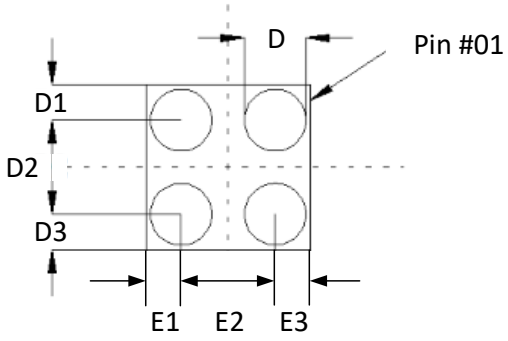


Figure 6. 2 Application Diagram

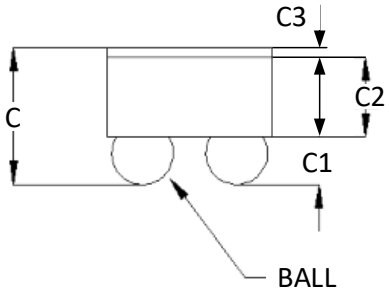
7. PACKAGE INFORMATION



Top View



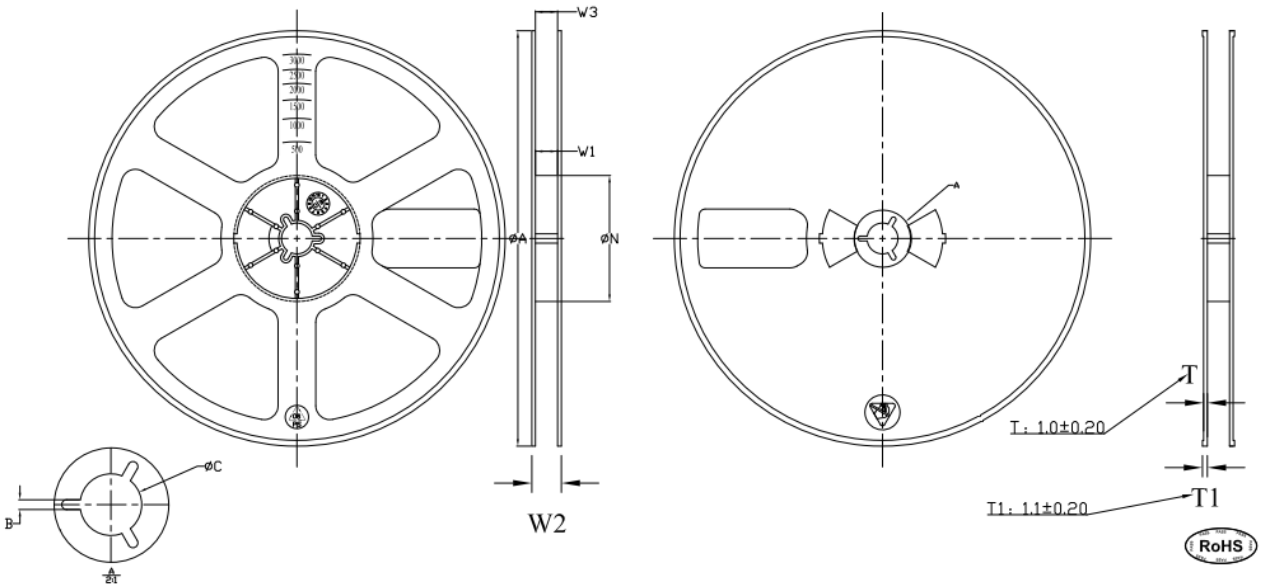
Bottom View



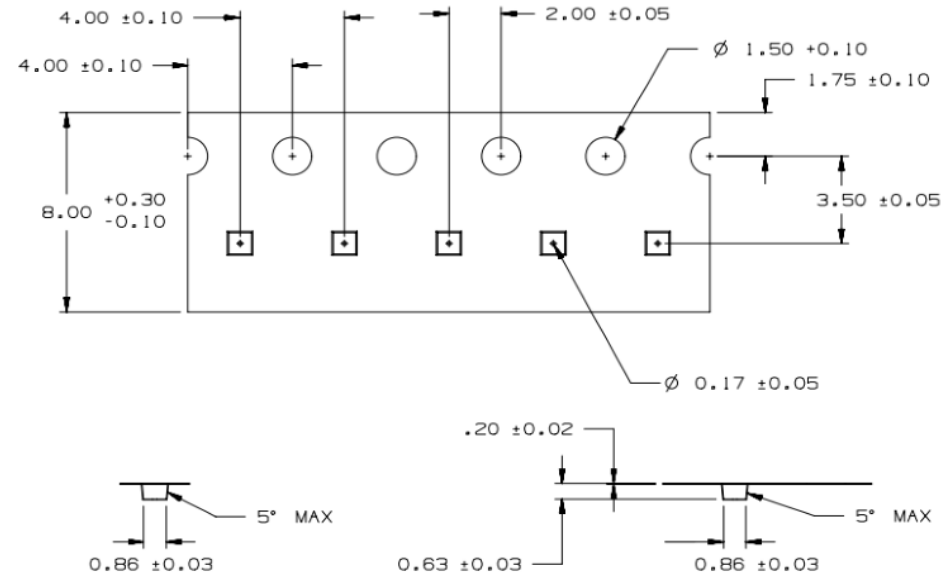
Symbol	DimenSions In Millimeters		DimenSions In Inches	
	NOM	Toler.	NOM	Toler.
A	0.750	±0.020	0.030	±0.001
B	0.750	±0.020	0.030	±0.001
C	0.538	±0.049	0.021	±0.002
C1	0.213	±0.021	0.008	±0.001
C2	0.300	±0.025	0.012	±0.001
C3	0.025	±0.003	0.001	±0.000
D	0.262	±0.026	0.010	±0.001
D1	0.175	NA	0.007	NA
D2	0.400	NA	0.016	NA
D3	0.175	NA	0.007	NA
E1	0.175	NA	0.007	NA
E2	0.400	NA	0.016	NA
E3	0.175	NA	0.007	NA

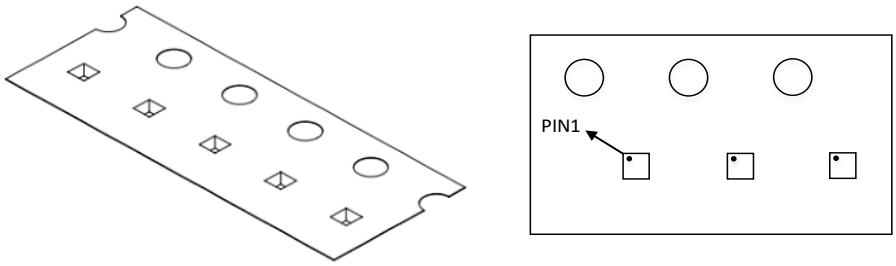
Figure 7.1 DSBGA (4) Package Shape and Dimension in millimeters and (inches)

8. TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS							
TAPE WIDTH	øA±1.0	øN±0.5	W1±0.5	W2 MAX	$W3^{+3}_{-1}$	$øC^{+0.3}_{-0.2}$	$B^{+0.3}_{-0.3}$
DPR-11D-B*	178	54	9.5	15.0	9.4	13.2	2.2





9. ORDERING INFORMATION

Type	MSL	Pack Qty/Container	Marking(1, 2)	Description
NST103A-CWLR	1	3000ea/Reel	03A YWW	DSBGA-4 package
NST103B-CWLR	1	3000ea/Reel	03B YWW	DSBGA-4 package
NST103C-CWLR	1	3000ea/Reel	03C YWW	DSBGA-4 package
NST103D-CWLR	1	3000ea/Reel	03D YWW	DSBGA-4 package
NST103E-CWLR	1	3000ea/Reel	03E YWW	DSBGA-4 package
NST103F-CWLR	1	3000ea/Reel	03F YWW	DSBGA-4 package
NST103G-CWLR	1	3000ea/Reel	03G YWW	DSBGA-4 package
NST103H-CWLR	1	3000ea/Reel	03H YWW	DSBGA-4 package

(1) The marking relates to the logo, the lot trace code information.

(2) If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

10. REVISION HISTORY

Revision	Description	Date
0.1	Initial Version	2020/6/5
0.2	Optimize text presentation	2021/08/16
0.3	Released Version.	2021/08/30
1.2	Update functional description. Optimize text presentation	2022/09/05

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