NT1819NAAE2S
Absorptive High Isolation SPDT Switch

FEATURES

- Operation voltage: 3.3 V typ. (2.5 to 5.0 V)
- Low control voltage: 1.8 V typ.
- Low insertion loss:
  0.70/0.80/0.85/0.90/1.2 dB typ.
  @0.7/3.85/4.7/6.0/7.125 GHz
- High isolation:
  70/62/60/55/51 dB typ.
  @0.7/3.85/4.7/6.0/7.125 GHz, PC-P1/P2
  70/61/60/58/55 dB typ.
  @0.7/3.85/4.7/6.0/7.125 GHz, P1-P2
- High linearity: $P_{-0.1dB}$ = +31 dBm typ.
- Switching time: 250 ns typ.
- Small package: 3.0 x 3.0 mm typ.
- Frequency range: 0.2 to 7.125 GHz
- Operation current: 200 μA typ.
- No DC blocking capacitor requirement unless external DC bias
- RoHS compliant, Halogen free, MSL1

APPLICATIONS

- Cellular base transceiver station (small/macro cell, etc.)
- Other wireless communication applications

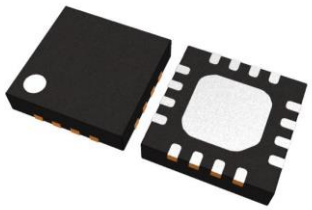
GENERAL DESCRIPTION

The NT1819NAAE2S is an absorptive high isolation SPDT switch suitable for 5G cellular infrastructure and so on.

This switch features high isolation characteristics between RF terminals and achieves 60 dB isolation at 3.85 GHz and 50 dB isolation at 7.125 GHz. It is available for various applications needed high isolation between circuits or devices.

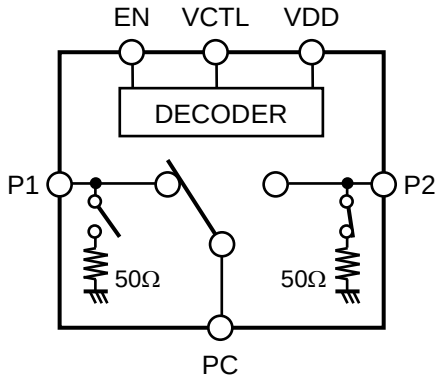
The P1 terminal and P2 terminal of NT1819NAAE2S are terminated into 50Ω at unused state. Therefore, it is prevented for miss-match when another circuit is connected to this switch.

The NT1819NAAE2S adopts compact 3 x 3 mm QFN3030-16-NA surface mount package, so this switch can contribute to small mounting area.



QFN3030-16-NA
3.0 × 3.0 × 0.75 (mm)

BLOCK DIAGRAM



■ PRODUCT NAME INFORMATION

NT1819 NA A E2 S

Description of configuration

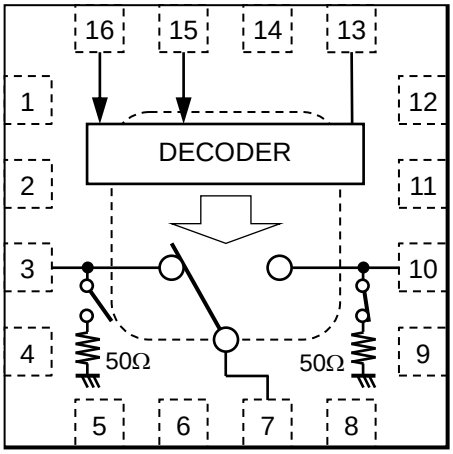
Composition	Item	Description
NA	Package code	Indicates the package. Refer to the order information.
A	Version	Indicates the product version. “A” is initial version.
E2	Packing	Refer to the packing specifications.
S	Grade	Indicates the quality grade. “S” means general-purpose and consumer application. Operating temperature range: -40ºC to +105ºC, Test temperature: +25ºC

■ ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	PLATING COMPOSITION	WEIGHT (mg)	QUANTITY (pcs/reel)
NT1819NAAE2S	QFN3030-16-NA	Yes	Yes	SnBi	17	1,500

■ PIN DESCRIPTIONS

(Top View)



QFN3030-16-NA Pin configuration

Pin No.	Pin Name	Description
1	GND	Ground terminal
2	GND	Ground terminal
3	P1	RF terminal 1
4	GND	Ground terminal
5	NC(GND)	No connect terminal (need to connect Ground plane)
6	NC(GND)	No connect terminal (need to connect Ground plane)
7	PC	Common RF terminal
8	NC(GND)	No connect terminal (need to connect Ground plane)
9	GND	Ground terminal
10	P2	RF terminal 2
11	GND	Ground terminal
12	GND	Ground terminal
13	VDD	Voltage supply terminal
14	NC(GND)	No connect terminal (need to connect Ground plane)
15	VCTL	Control signal input terminal
16	EN	Control signal input terminal
Exposed PAD		Need to connect Ground plane

Please refer to "APPLICATION CIRCUIT" for details.

■ TRUTH TABLE

"H" = V_{CTL}(H), "L" = V_{CTL}(L)

ON PATH	VCTL	EN
PC-P1	H	L
PC-P2	L	L
All OFF	H	H
	L	H

■ ABSOLUTE MAXIMUM RATINGS

General conditions: T_a = +25°C, Z_s = Z_l = 50Ω

	Symbol	Ratings	Unit
Supply voltage	V_{DD}	6.0	V
Control voltage	V_{CTL}	6.0	V
RF input power	P_{IN}	+34 *1	dBm
		+27 *2	
Power dissipation	P_D *3	1400	mW
Operating temperature range	T_{opr}	−40 to +105	°C
Storage temperature range	T_{stg}	−55 to +150	°C

*1 V_{DD} = 3.3 V, ON port

*2 V_{DD} = 3.3 V, OFF port

*3 4-layer FR4 PCB with through-hole (101.5 x 114.5 mm), T_j = +150°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

*1 Calculate the power consumption of the IC from the operating conditions and calculate the junction temperature with the thermal resistance.

Please refer to "*THERMAL CHARACTERISTICS*" for the thermal resistance under our measurement board conditions.

■ THERMAL CHARACTERISTICS

Parameter	Measurement Result
Thermal Resistance (θja)	θja = 89.3 °C/W

θja: Junction-to-Ambient Thermal Resistance

■ ELECTROSTATIC DISCHARGE RATINGS

	Conditions	Pin No.	Pin Name	Protection Voltage	
				Ground	VDD
HBM	C = 100 pF, R = 1.5 kΩ	1	GND	COM.	±2000 V
		2	GND	COM.	±2000 V
		3	P1	±2000 V	±2000 V
		4	GND	COM.	±500 V
		5	NC(GND)	-	-
		6	NC(GND)	-	-
		7	PC	±2000 V	±2000 V
		8	NC(GND)	-	-
		9	GND	COM.	±500 V
		10	P2	±2000 V	±2000 V
		11	GND	COM.	±2000 V
		12	GND	COM.	±2000 V
		13	VDD	±2000 V	COM.
		14	NC(GND)	-	-
		15	VCTL	±2000 V	±2000 V
		16	EN	±2000 V	±2000 V

	Conditions	Protection Voltage
CDM	Field Induced CDM	±1000 V

ELECTROSTATIC DISCHARGE RATINGS
The electrostatic discharge tests are done based on JEDEC JS-001 and JS-002. In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

■ RECOMMENDED OPERATING CONDITIONS

	Symbol	Value	Unit
Supply voltage	V_{DD}	2.5 to 5.0	V
Control voltage (High)	V_{CTL}(H)	1.35 to 5.0	V
Operating temperature range	T_a	-40 to +105	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS 1 (DC)

General conditions: T_a = +25°C, Z_s = Z_l = 50Ω

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}	VDD terminal	2.5	3.3	5.0	V
Operating current	I_{DD}	No RF input, V_{DD} = 3.3 V	-	200	350	μA
Control voltage (High)	V_{CTL}(H)	VCTL terminal, EN terminal	1.35	1.8	5.0	V
Control voltage (Low)	V_{CTL}(L)	VCTL terminal, EN terminal	0	-	0.45	V
Control current	I_{CTL}	V_{CTL}(H) = 1.8 V	-	5	10	μA

■ ELECTRICAL CHARACTERISTICS 2 (RF)

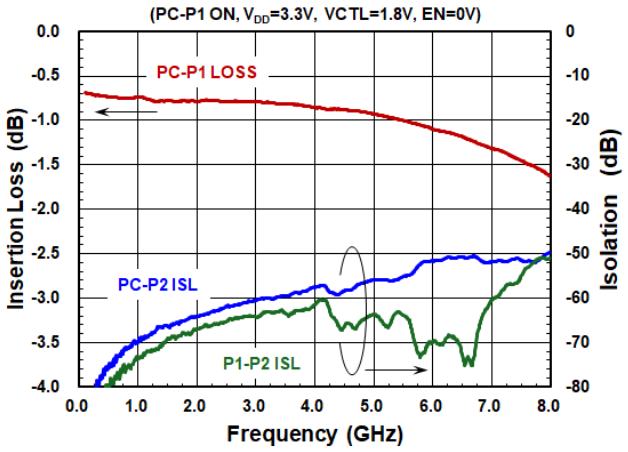
General conditions: V_{DD} = 3.3 V, V_{CTL}(H) = 1.8 V, V_{CTL}(L) = 0 V, T_a = +25°C, Z_s = Z_l = 50Ω, with application circuit

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Insertion loss	LOSS	f = 0.7 GHz	-	0.70	0.90	dB
		f = 1.9 GHz	-	0.75	0.95	
		f = 2.7 GHz	-	0.80	1.00	
		f = 3.85 GHz	-	0.80	1.00	
		f = 4.7 GHz	-	0.85	1.15	
		f = 6.0 GHz	-	0.90	1.20	
		f = 7.125 GHz	-	1.20	1.60	
Isolation 1 (PC-P1/PC-P2)	ISL1	f = 0.7 GHz	65	70	-	dB
		f = 1.9 GHz	60	64	-	
		f = 2.7 GHz	58	62	-	
		f = 3.85 GHz	56	62	-	
		f = 4.7 GHz	55	60	-	
		f = 6.0 GHz	50	55	-	
		f = 7.125 GHz	47	51	-	
Isolation 2 (P1-P2)	ISL2	f = 0.7 GHz	67	70	-	dB
		f = 1.9 GHz	65	70	-	
		f = 2.7 GHz	60	65	-	
		f = 3.85 GHz	56	61	-	
		f = 4.7 GHz	55	60	-	
		f = 6.0 GHz	52	58	-	
		f = 7.125 GHz	50	55	-	
Return loss 1 (ON terminal)	RL1	f = 0.7 GHz	18	25	-	dB
		f = 1.9 GHz	18	23	-	
		f = 2.7 GHz	18	23	-	
		f = 3.85 GHz	16	22	-	
		f = 4.7 GHz	16	20	-	
		f = 6.0 GHz	12	18	-	
		f = 7.125 GHz	9	12	-	
Return loss 2 (OFF terminal)	RL2	f = 0.7 GHz	18	25	-	dB
		f = 1.9 GHz	18	25	-	
		f = 2.7 GHz	18	25	-	
		f = 3.85 GHz	16	23	-	
		f = 4.7 GHz	16	20	-	
		f = 6.0 GHz	12	20	-	
		f = 7.125 GHz	11	20	-	
Input power at 0.1 dB compression point	$P_{-0.1dB}$	f = 0.7 to 7.125 GHz	+29	+31	-	dBm
Switching time	T_{SW}	50% VCTL to 10% / 90% RF	-	250	400	ns

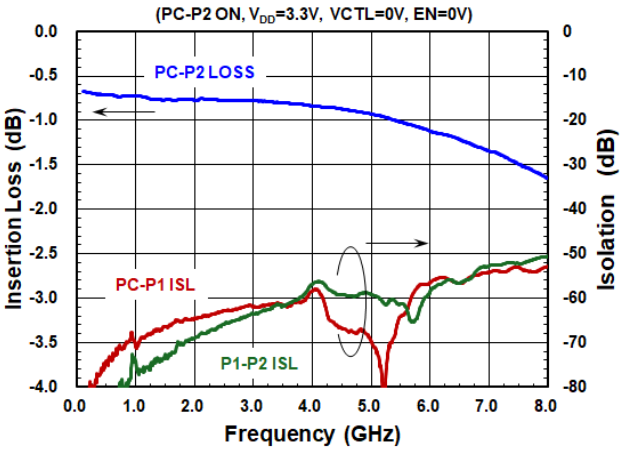
■ TYPICAL CHARACTERISTICS

General conditions: V_{DD} = 3.3 V, V_{CTL}(H) = 1.8 V, V_{CTL}(L)=0V, T_a = +25°C, Z_S = Z_I = 50Ω, with application circuit
(Typical Characteristics are intended to be used as reference data; they are not guaranteed.)

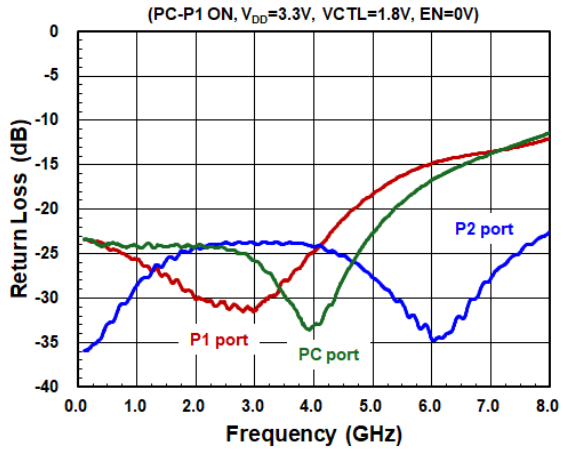
Insertion Loss, Isolation vs Frequency



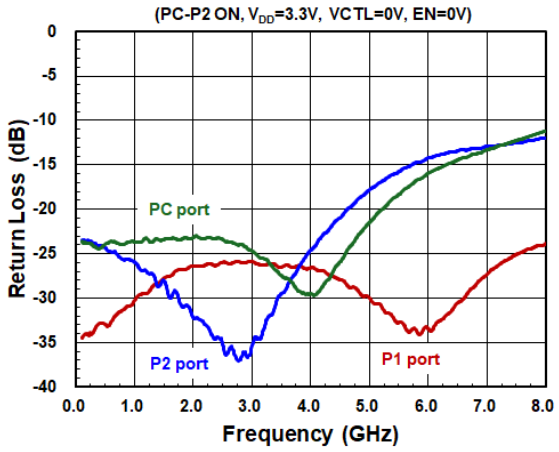
Insertion Loss, Isolation vs Frequency



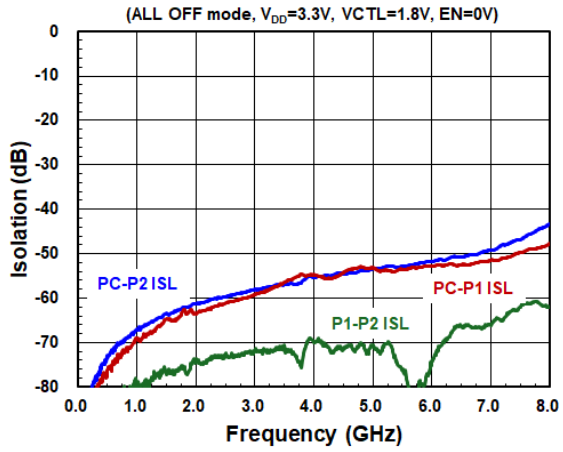
Return Loss vs Frequency



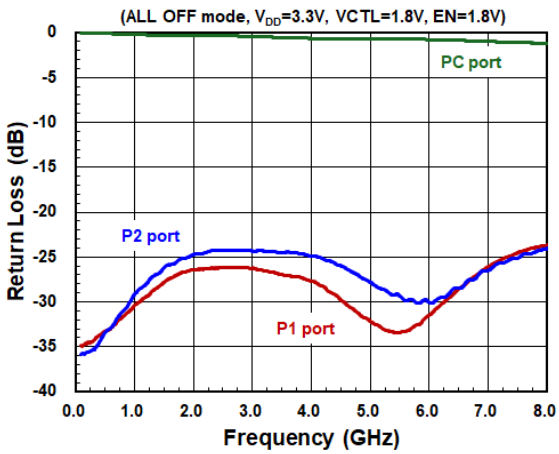
Return Loss vs Frequency



Isolation vs Frequency



Return Loss vs Frequency



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General conditions: V_{DD} = 3.3 V, V_{CTL}(H) = 1.8 V, V_{CTL}(L)=0V, T_a = +25°C, Z_S = Z_I = 50Ω, with application circuit
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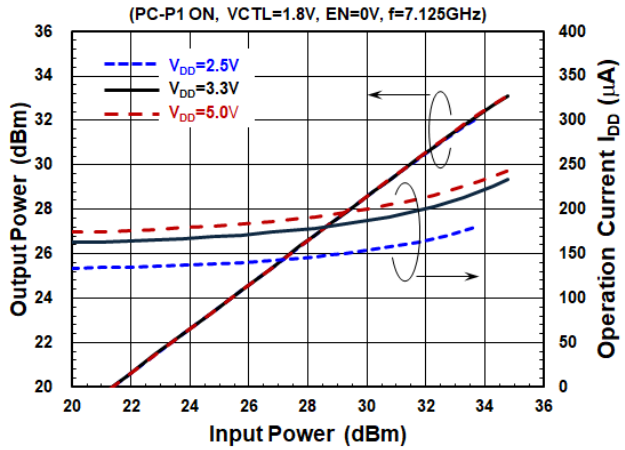
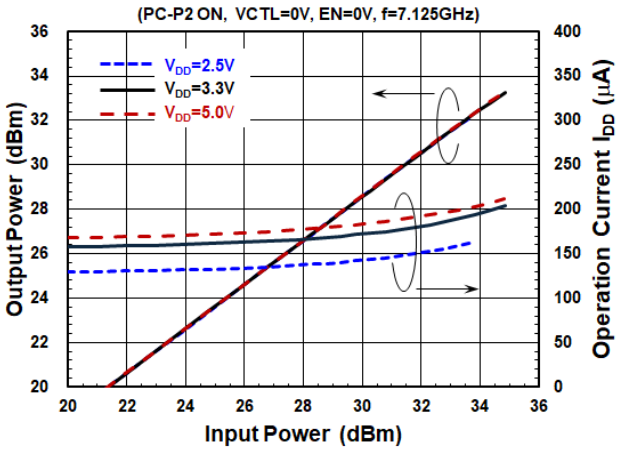
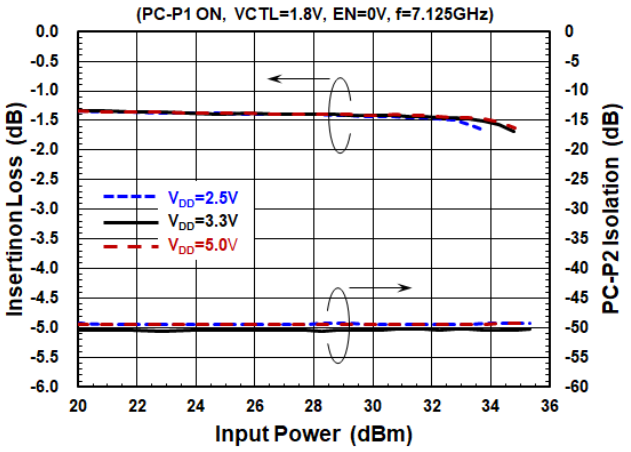
Output Power, IDD vs Input Power



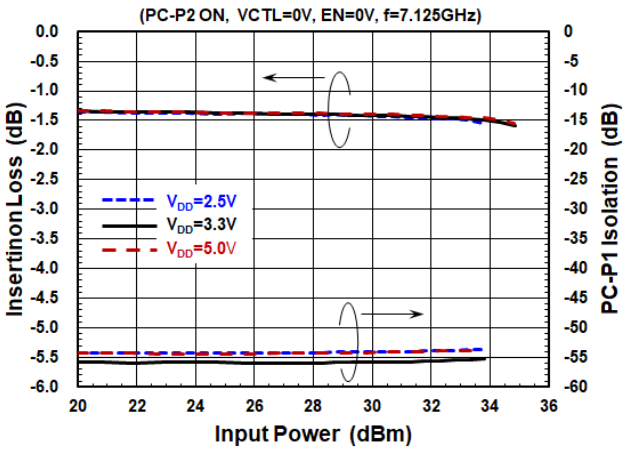
Output Power, IDD vs Input Power



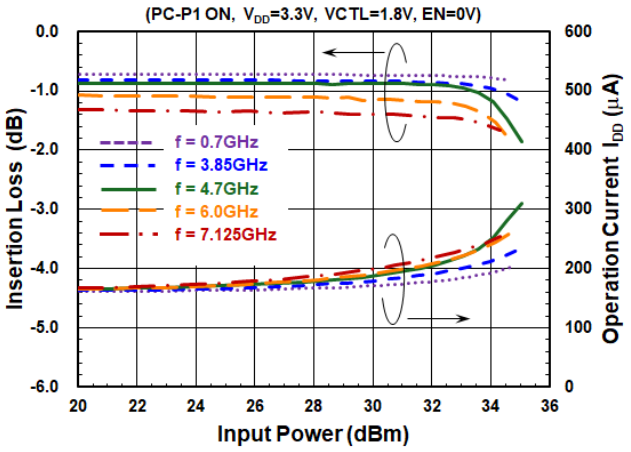
Insertion Loss, Isolation vs Input Power



Insertion Loss, Isolation vs Input Power



Insertion Loss, I_{DD} vs Input Power



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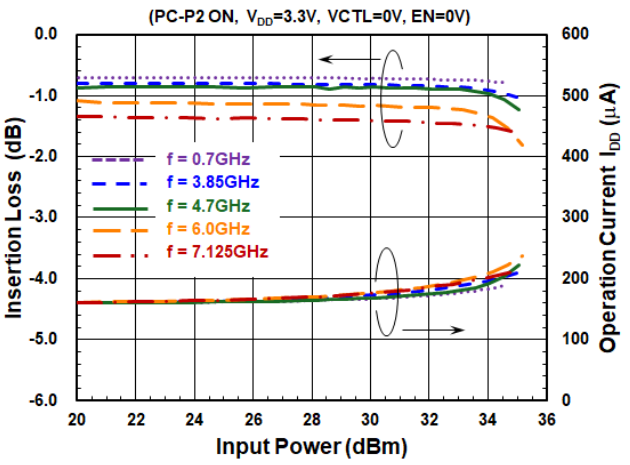

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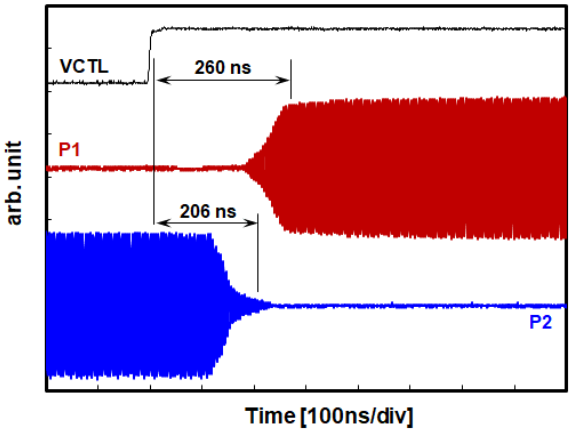
Switching Time

(V_{DD}=3.3V, V_{CTL}(H)=1.8V, V_{CTL}(L)=0V, EN=0V)



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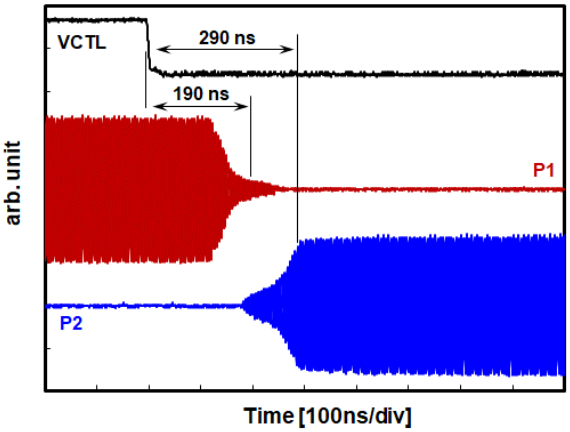
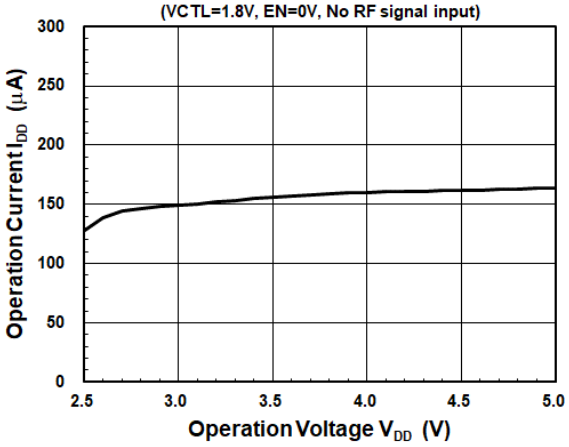


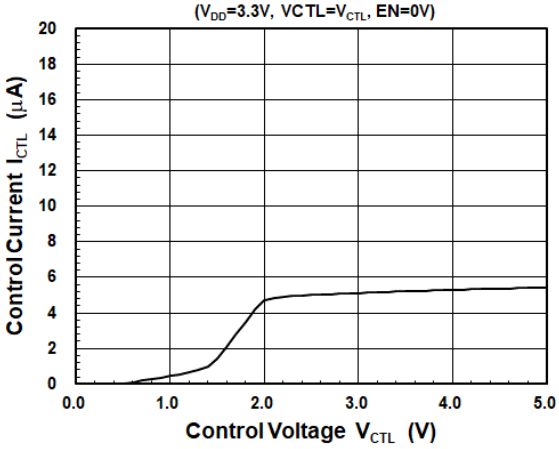
Operation Current vs Operation Voltage

(VCTL=1.8V, EN=0V, No RF signal input)



Control Current vs Control Voltage

(V_{DD}=3.3V, VCTL=V_{CTL}, EN=0V)



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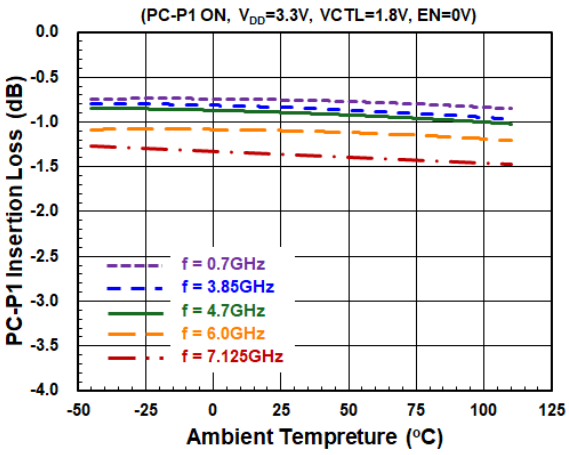
Insertion Loss vs Ambient Temperature



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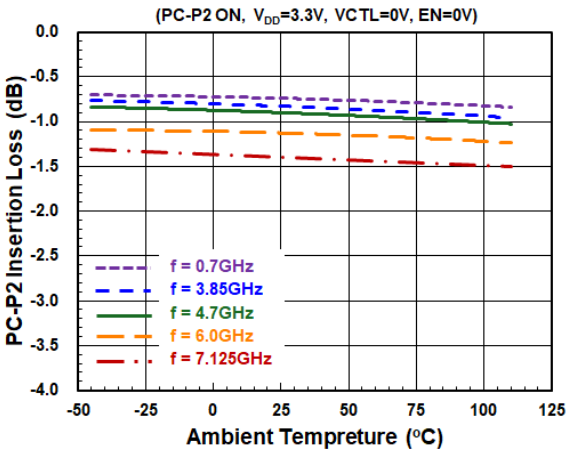
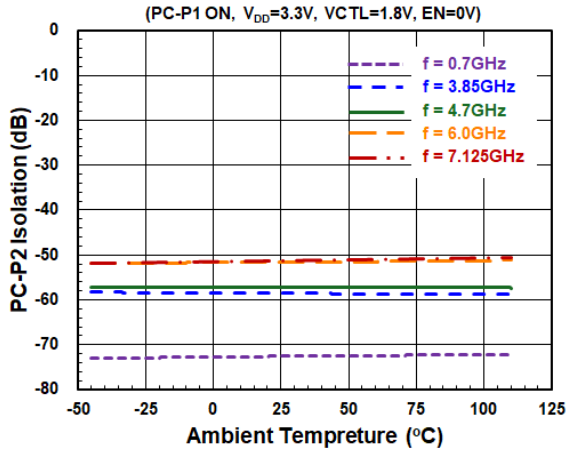
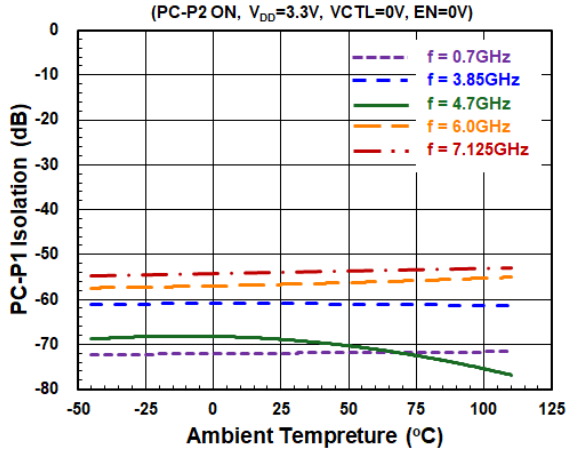


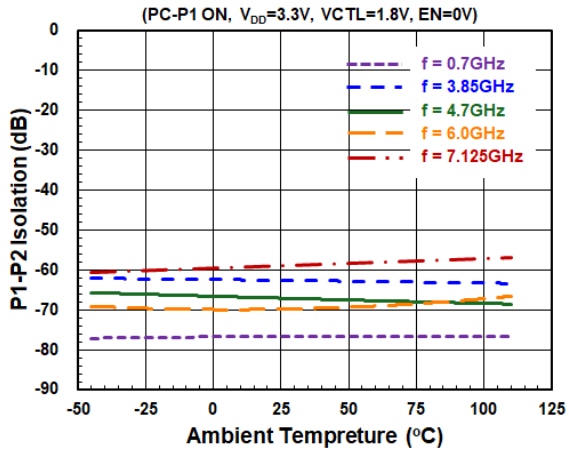
PC-P2 Isolaton vs Ambient Temperature



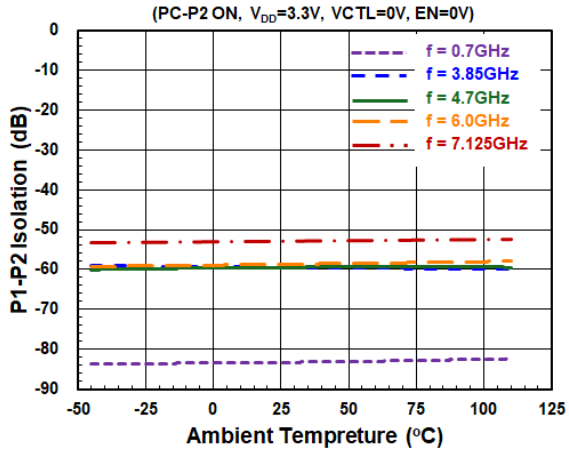
PC-P1 Isolation vs Ambient Temperature



P1-P2 Isolaton vs Ambient Temperature



P1-P2 Isolation vs Ambient Temperature



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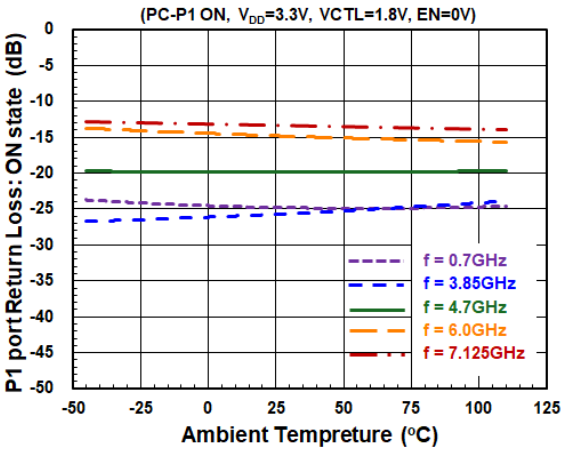
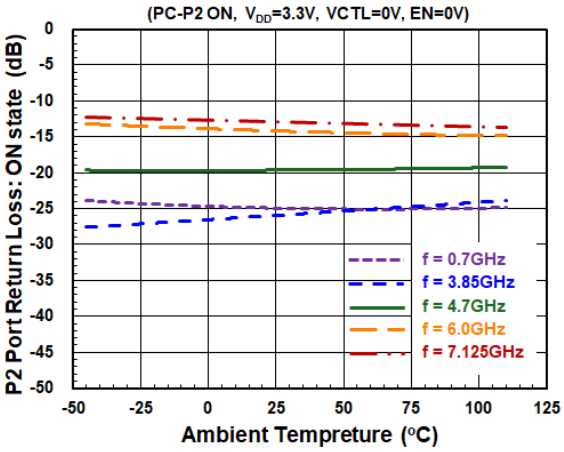
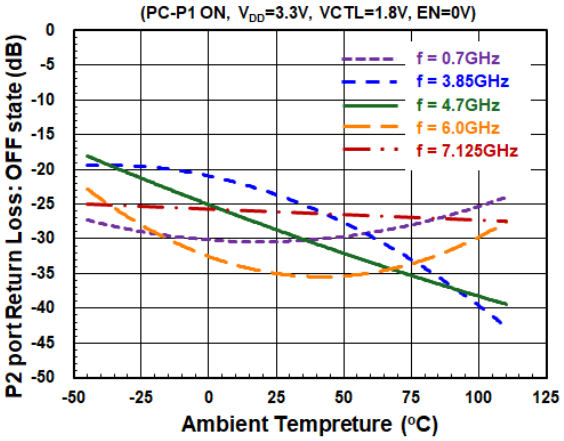
Retun Loss 1 vs Ambient Temperature



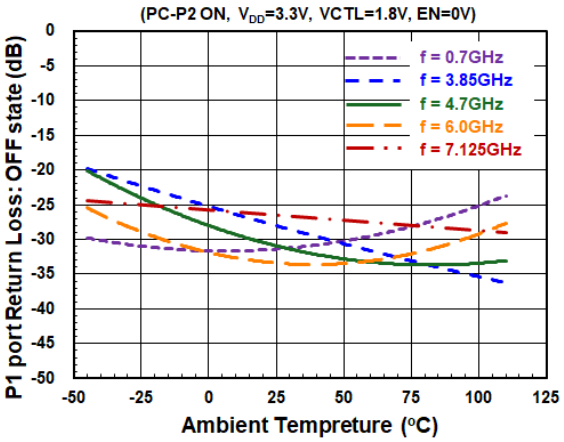
Return Loss 1 vs Ambient Temperature



Return Loss 2 vs Ambient Temperature



Return Loss 2 vs Ambient Temperature



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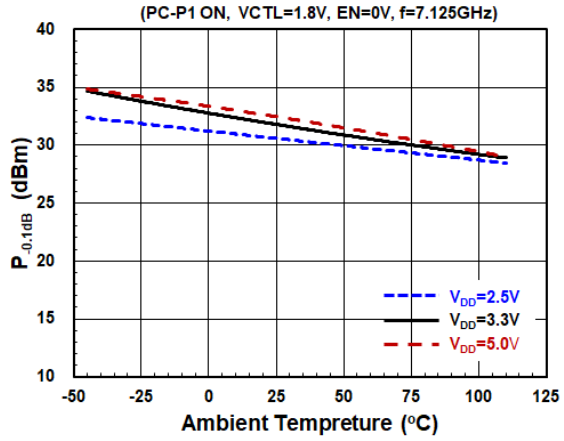
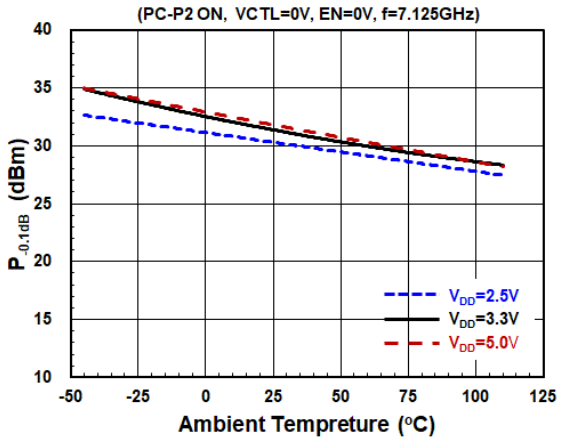
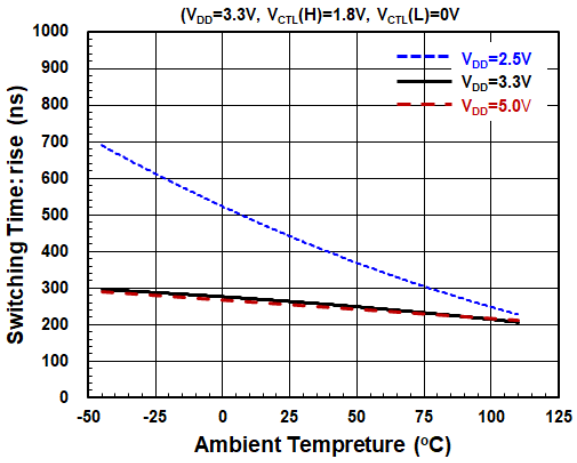
$P_{-0.1dB}$ vs Ambient Temperature



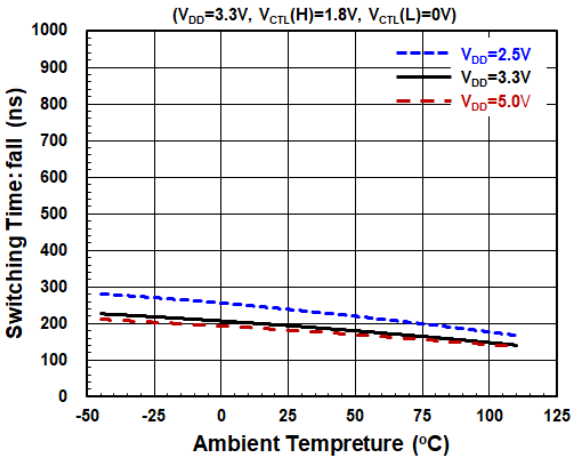
$P_{-0.1dB}$ vs Ambient Temperature



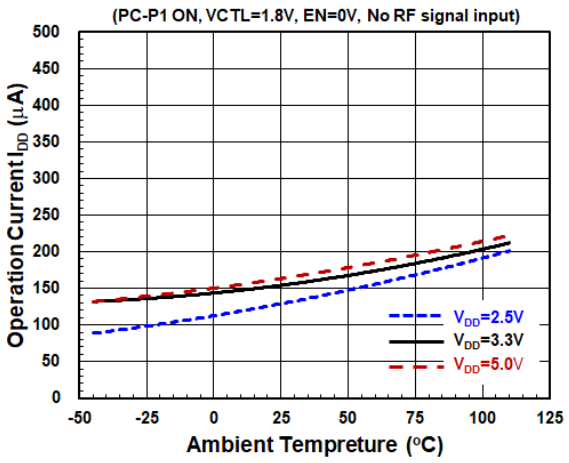
T_{SW}(rise) vs Ambient Temperature



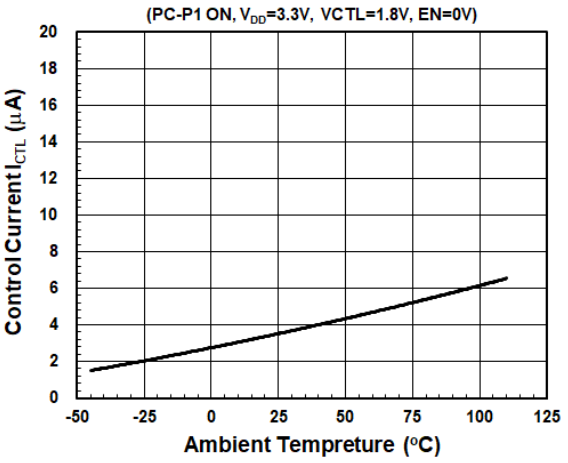
T_{SW}(fall) vs Ambient Temperature



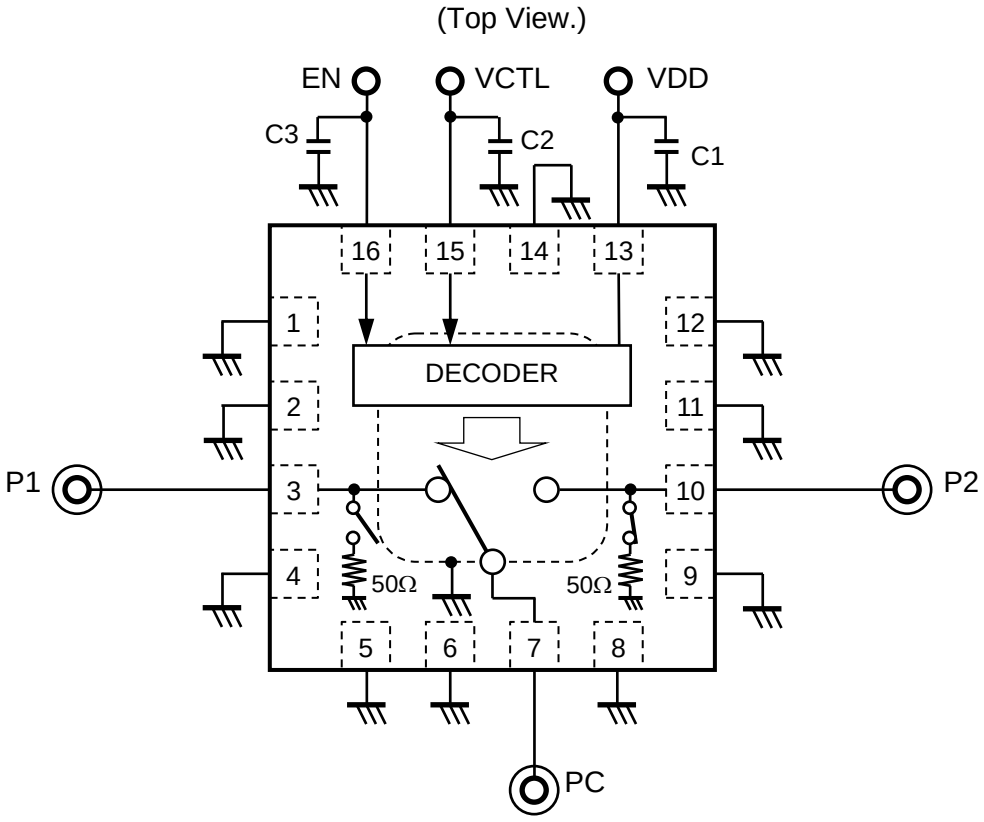
Operation Current vs Ambient Temperature



Control Current vs Ambient Temperature



■ APPLICATION CIRCUIT



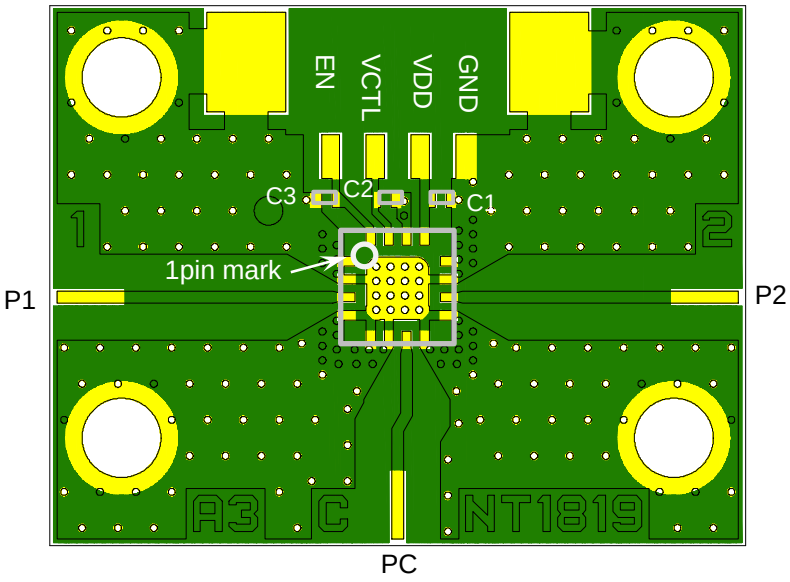
NT1819NAAE2S Typical Application Circuit

<Parts list>

Part ID	Value	Notes
C1	1000 pF	GRM03 series (muRata MFG)
C2, C3	10 pF	GRM03 series (muRata MFG)

● **Evaluation / PCB layout**

(TOP VIEW)



PC

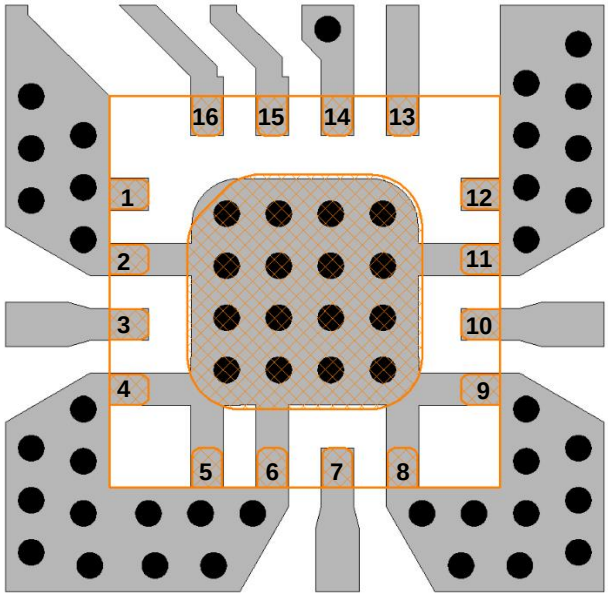
PCB: FR-4, t = 0.2 mm
Capacitor size: 0603 (0.6 x 0.3 mm)
Strip line width: 0.34 mm
PCB size: 19.4 x 14.0 mm
Through hole diameter: 0.2 mm

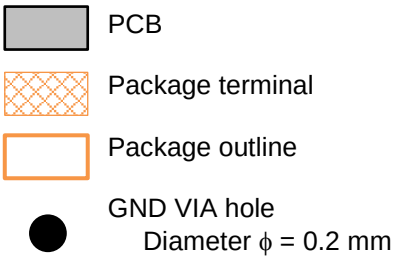
■ Loss of PCB and Connectors

Frequency (GHz)	Loss (dB)
0.7	0.16
1.9	0.25
2.7	0.32
3.85	0.42
4.7	0.49
6.0	0.61
7.125	0.70

● **PCB layout guideline**

(TOP VIEW)

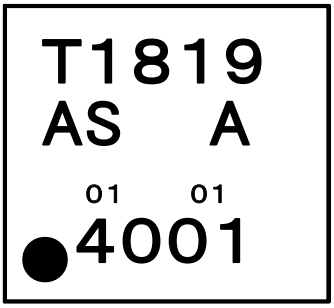




● **Precautions**

- No DC blocking capacitor is required for RF terminals. However, since each RF terminals are ground level, DC blocking capacitors are needed when another device biased DC connect to this IC.
- For avoiding the degradation of RF performance, the bypass capacitors (C1, C2, C3) should be placed as close as possible to VDD, VCTL, EN terminals.
- For good RF performance, all GND terminals and Exposed PAD should be connected to PCB ground plane, and through hole for ground should also be placed near GND terminals and Exposed PAD.

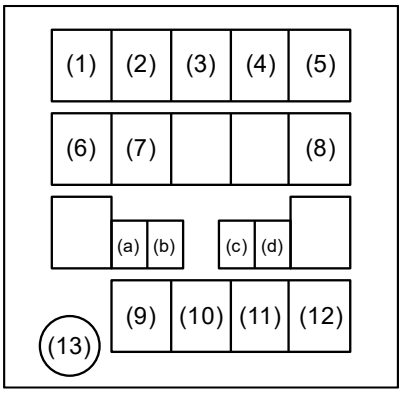
● MARKING SPECIFICATION



QFN3030-16-NA Marking Specification

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

Mark Index



Mark Explanation

Product name	Product category code	(1)
	Product code	(2)～(5)
	Product version	(6)
	Quality grade	(7)
Lot	Year code	(9)
	Serial number	(10)～(12)
	—	-
	—	-
Production code		(8)
Index mark		(13)
Mold address		(a)～(d)

REVISION HISTORY

Date	Revision	Contents of Changes
September 4, 2024	Ver. 1.0	Initial release

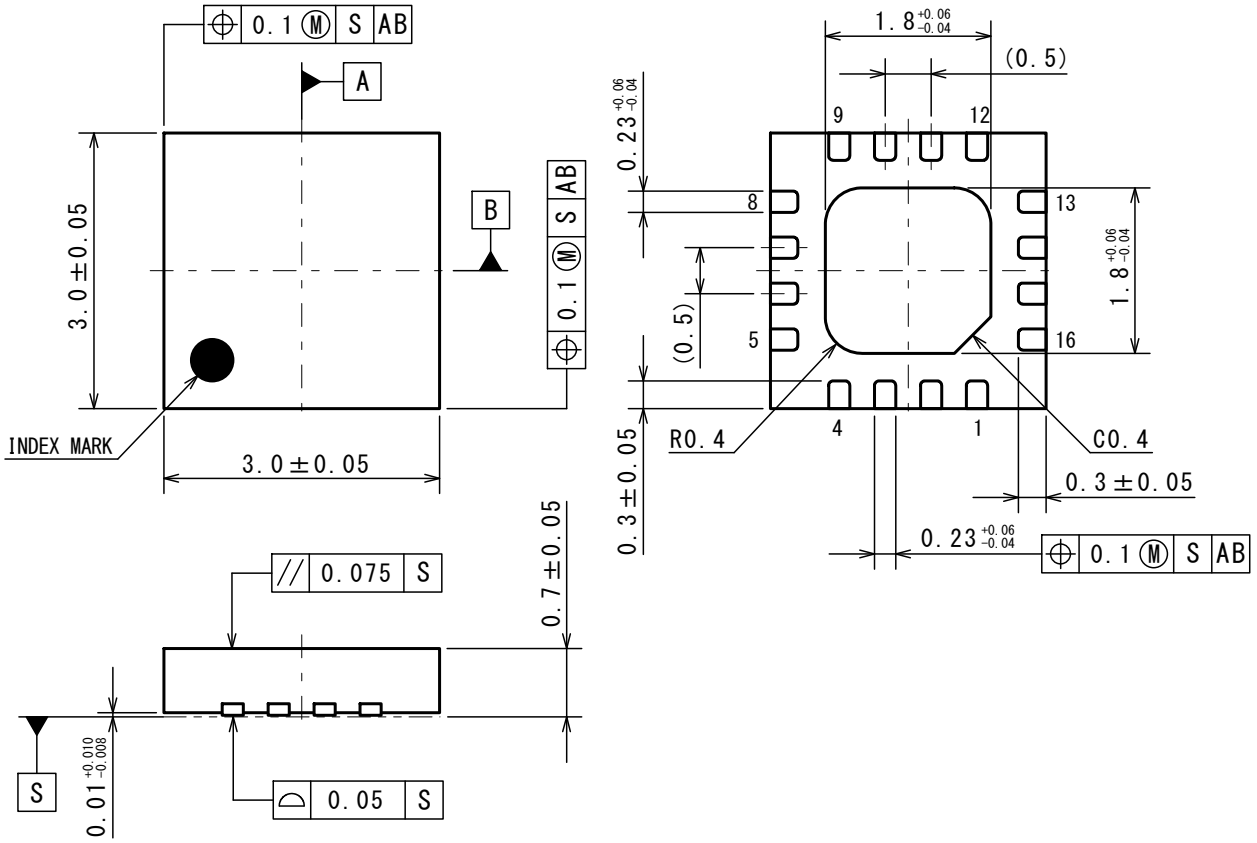
Nisshinbo Micro Devices Inc.

QFN3030-16-NA

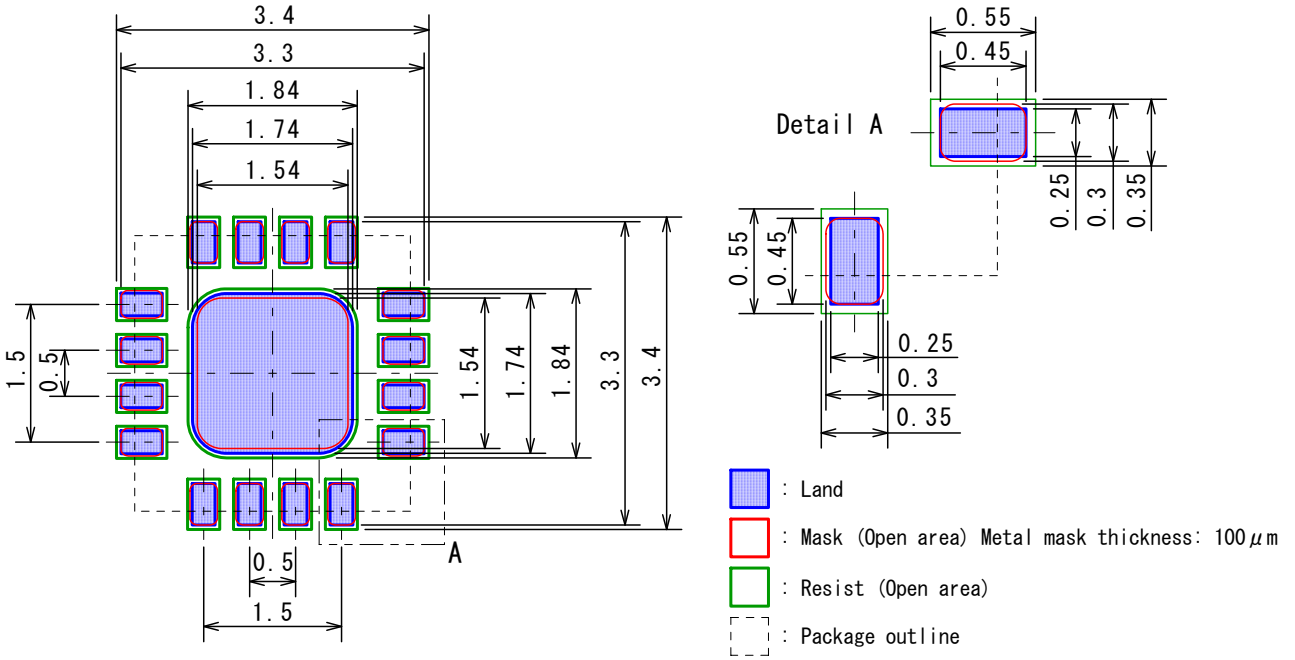
PI-QFN3030-16-NA-E-A

■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS



Nisshinbo Micro Devices Inc.

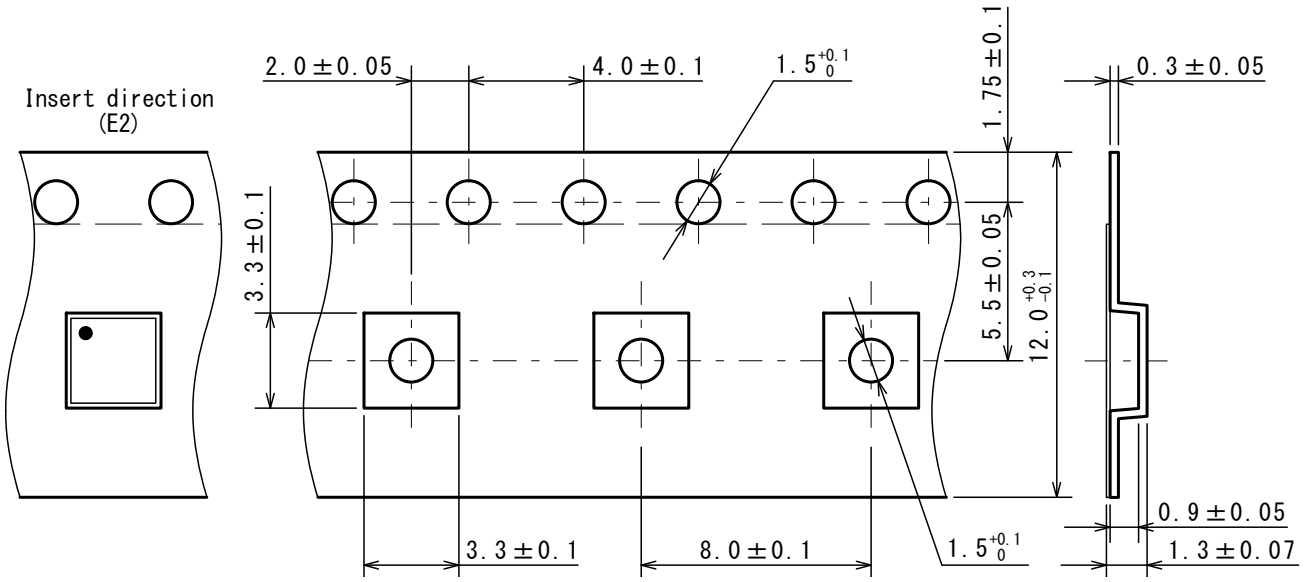
QFN3030-16-NA

PI-QFN3030-16-NA-E-A

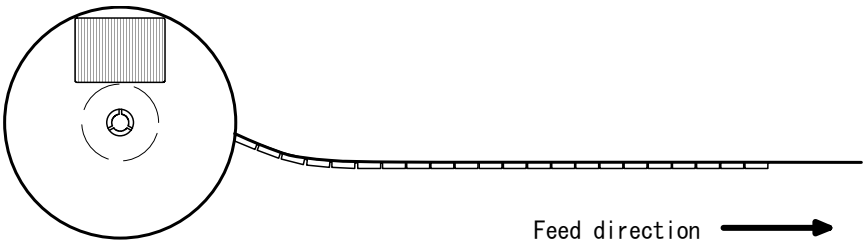
■ PACKING SPEC

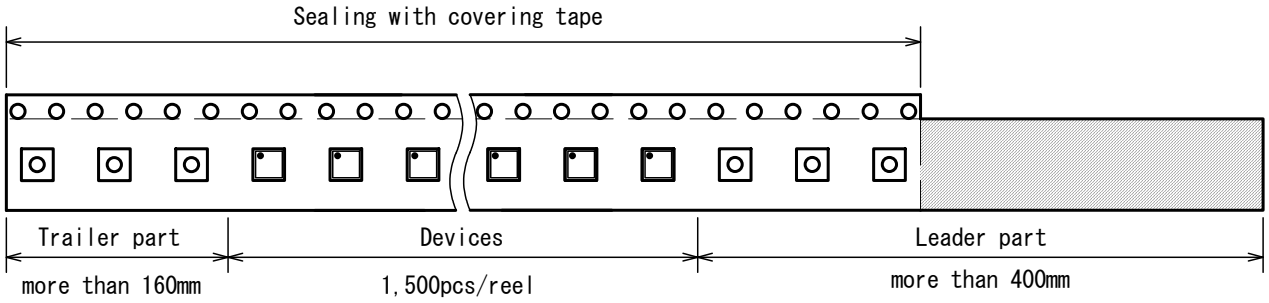
UNIT: mm

(1) Taping dimensions / Insert direction

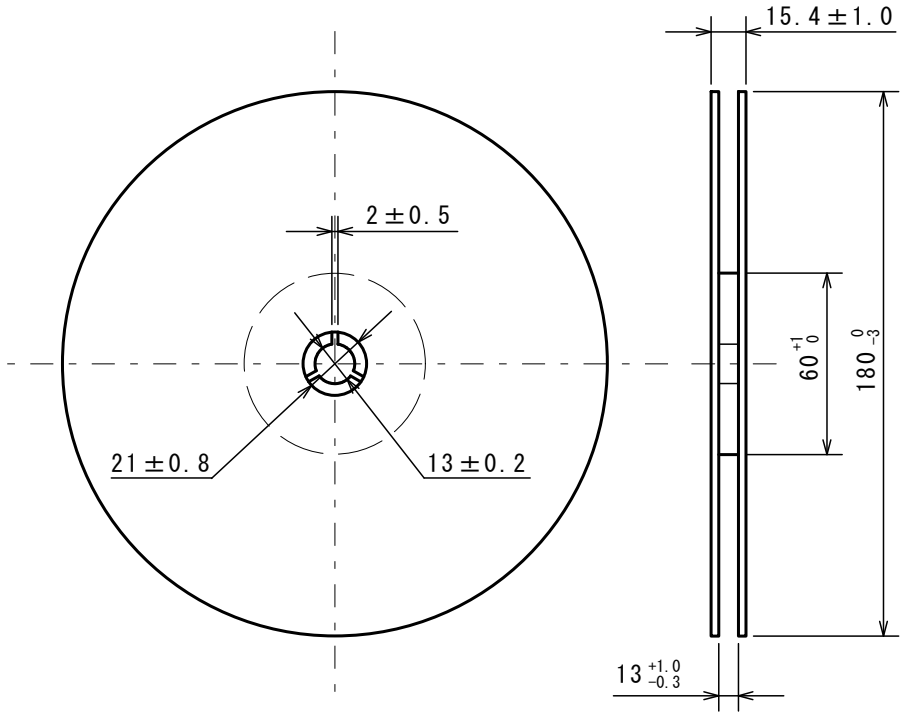


(2) Taping state





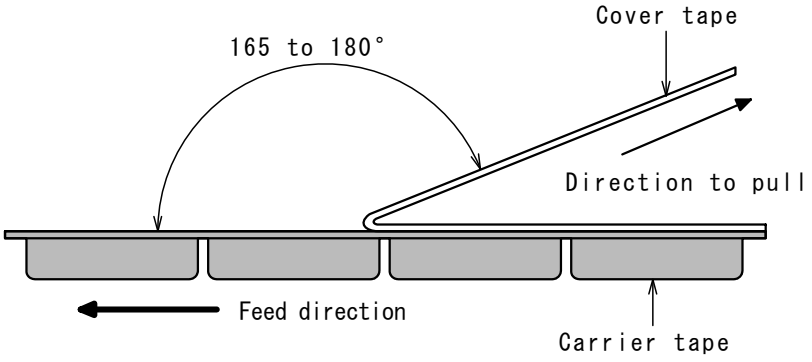
(3) Reel dimensions



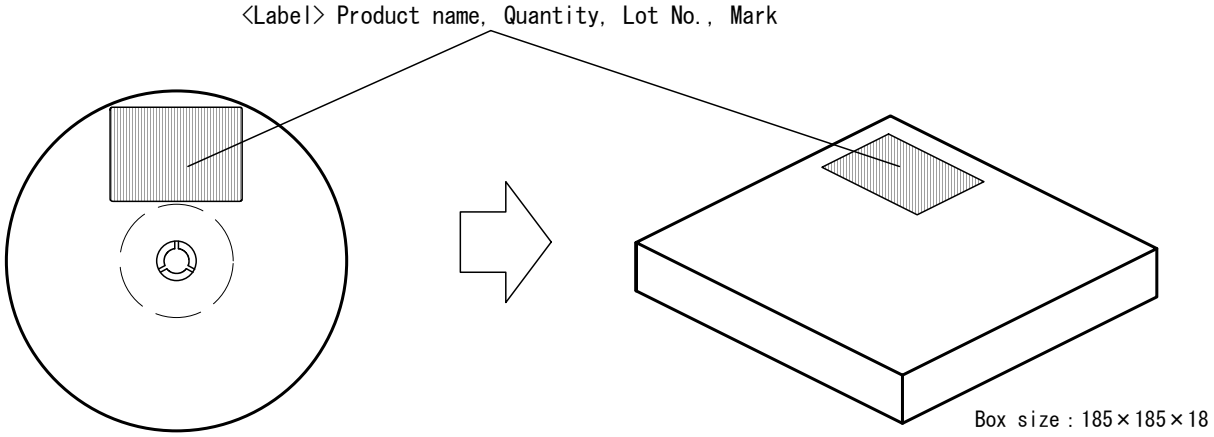
(4) Peeling strength

Peeling strength of cover tape

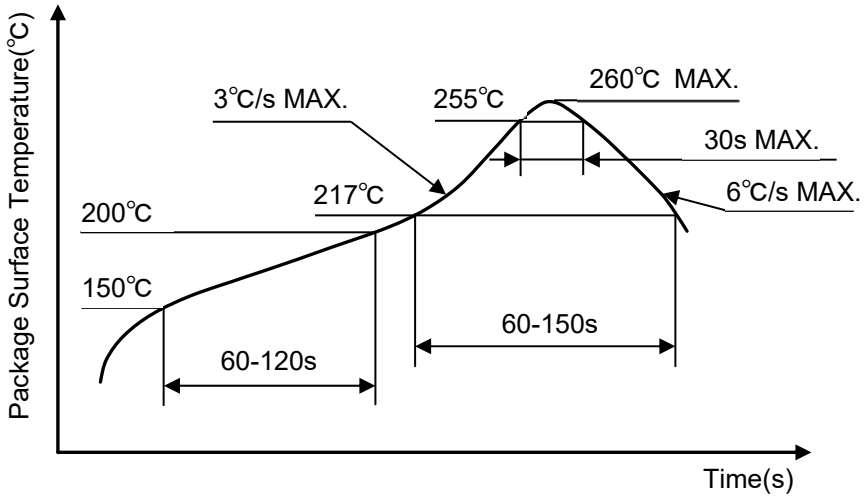
- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.3N



(5) Packing state



■ HEAT-RESISTANCE PROFILES



Reflow profile

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    - Traffic control system
    - Combustion equipment

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    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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