



Data Sheet

NT39024

Single Chip 720x544 Driver with Timing Controller

For 1440x272 TFT LCD

Version 0.7

Preliminary Spec

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Revision History

NT39024 Specification Revision History			
Version	Content	PAGE	Date
0.7	Modified serial 8-bit RGB output timing table	35	2008/05/21
	Modified HSD minimum setting from 01H to 02H	18	2008/05/21
	Modified DC electrical characteristics	32,33	2008/05/06
	Add conditions for VCOM AC Voltage	32	2008/05/06
	Added note for SHLR control register	16	2008/05/06
	Modified Serial 8-bit RGB input timing table	30	2008/05/06
	Modified DR0~DR7 pin descriptions	9	2008/05/06
0.6	Modified data input format	30,31	2008/04/14
	Modified output timing table	35	2008/03/18
0.5	Modified DC electrical characteristics	32,33	2008/03/04
	Modified 3-wire timing diagram	37	2008/03/04
	Modified Gamma Tables	26,27	2008/02/20
0.4	Modified PVDD operating range	3	2008/02/04
	Updated the procedure of OTP function	22	2008/02/04
	Added note for VCOMH adjustment	18	2008/02/04
0.3	Modified VDDIO minimum value	32	2008/01/30
0.2	Updated DC and AC electrical characteristics	32-34	2008/01/23
	Revised 3-wire command format	12	2008/01/17
0.1	New spec.	-	2007/12/12

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Features

- **Generate 720x544 TFT control signals with timing controller**
- **Panel resolution(HxV): 1440x272**
- **8-bit resolution 256 gray scale with Dithering(7bits DAC + 1 bit FRC)**
- **Display control and function select by 3-wire serial communication control.**
- **Build-in DC-DC control circuit, charge pump, VCOM with programmable adjustment**
- **Power for digital circuit(VDD): 2.7V~ 3.6V**
- **Power for analog circuit(PVDD): 2.6V ~ 3.6V**
- **Source output deviation: $\pm 20\text{mV}$**
- **Built-in R-DAC gamma correction**
- **Line inversion or half line inversion selectable**
- **Right/Left shift, Up and Down scan function selectable**
- **Build-In PWM circuit for LED Back-light**
- **COG package**

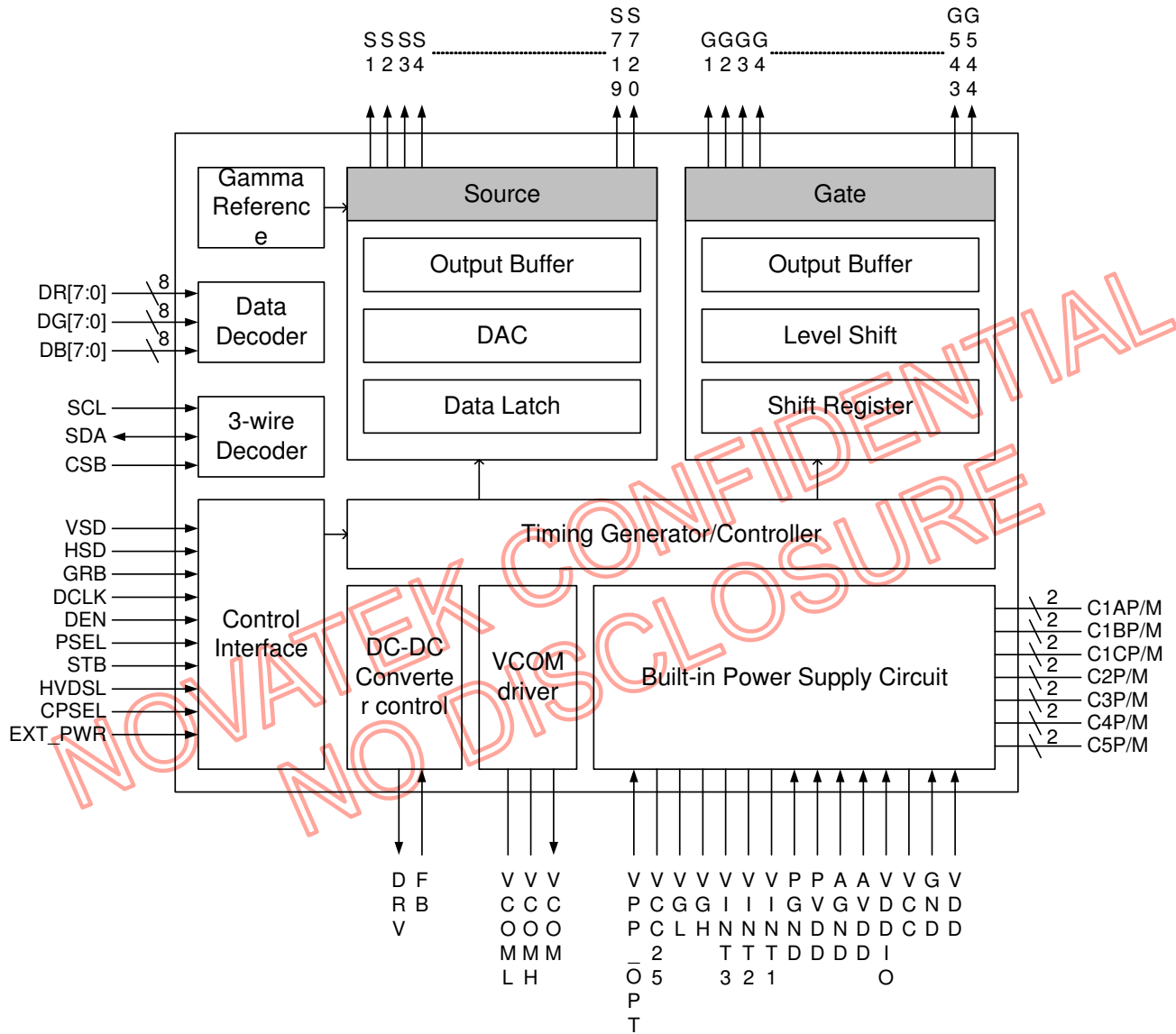
General Description

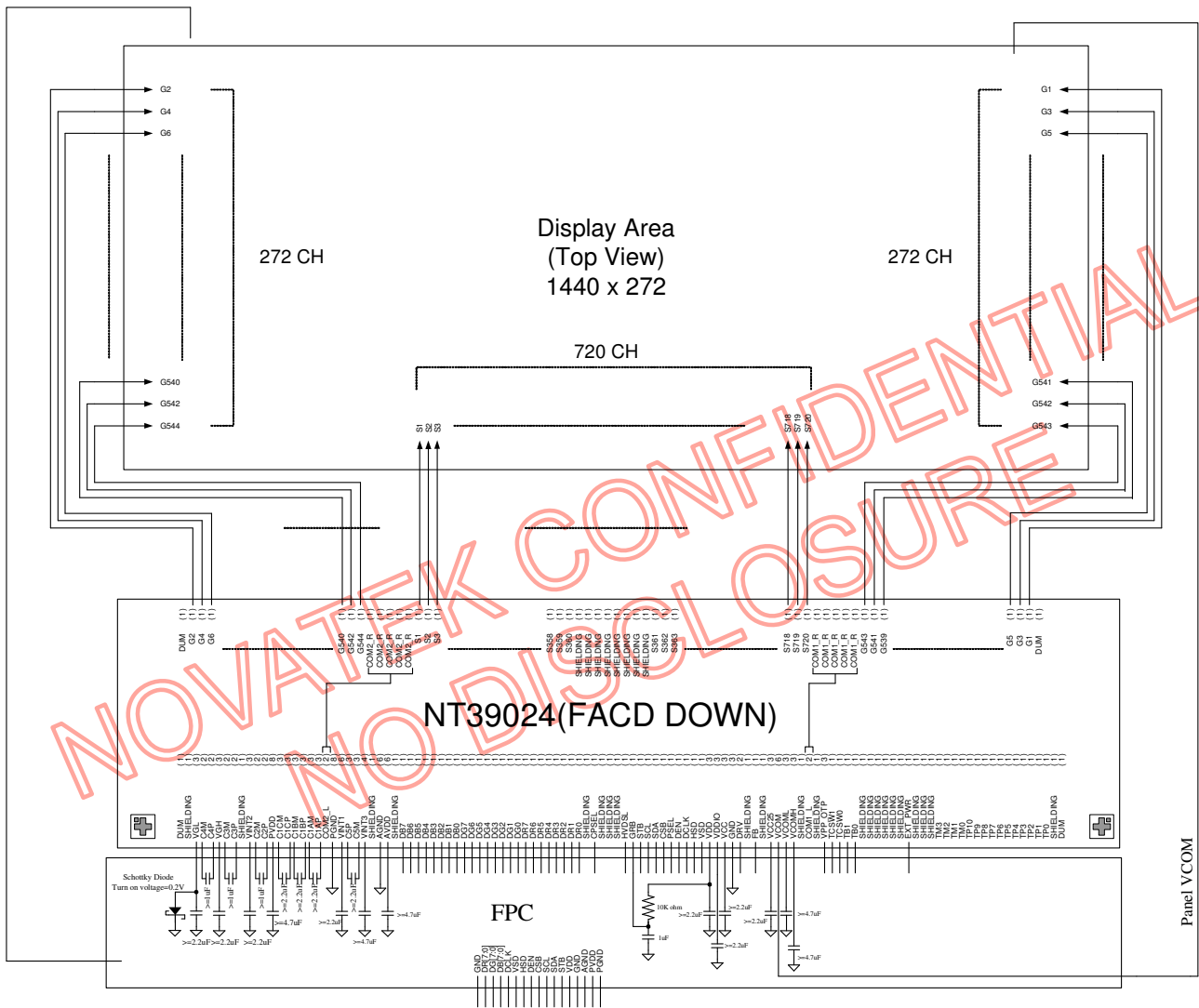
NT39024 is one-chip solution for TFT-LCD small panel. This chip integrated source driver, gate driver, built-in power generator and timing controller for the small panel application focused on the resolution of 1440x272. The serial communication interface is also embedded for function setting.

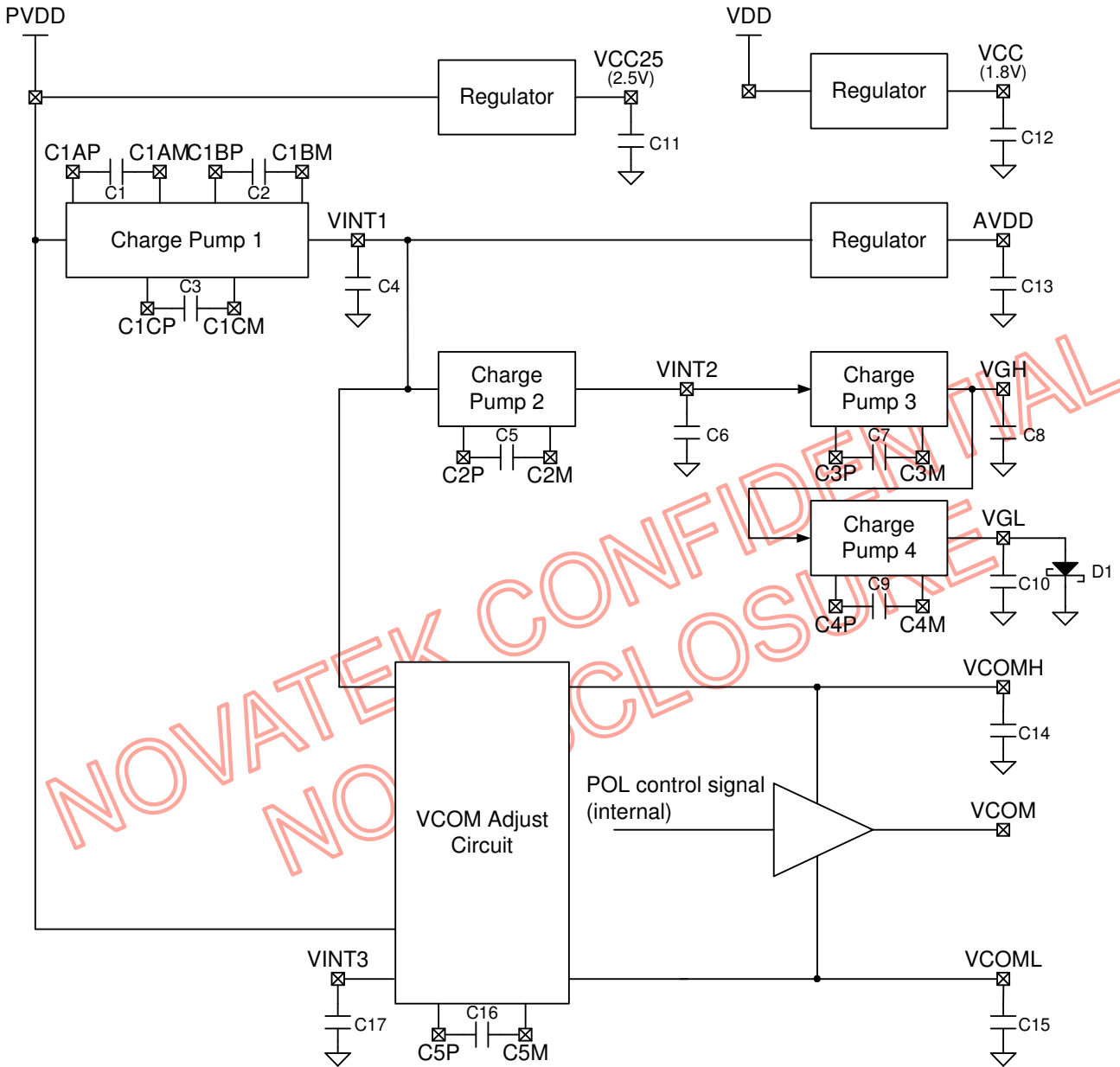
This chip can be operated under a wide range of supply voltage. By applying "Double Gate Driver" panel architecture, the number of source output channel is reduced to 720 and the number of gate output channels is increased to 544. For the concern of lower power dissipation, line inversion driving technique is adopted. With dithering technique was applied, source output support 8-bit resolution 256-gray scale for small output deviation are designed to support higher color resolution.

Function Block Diagram

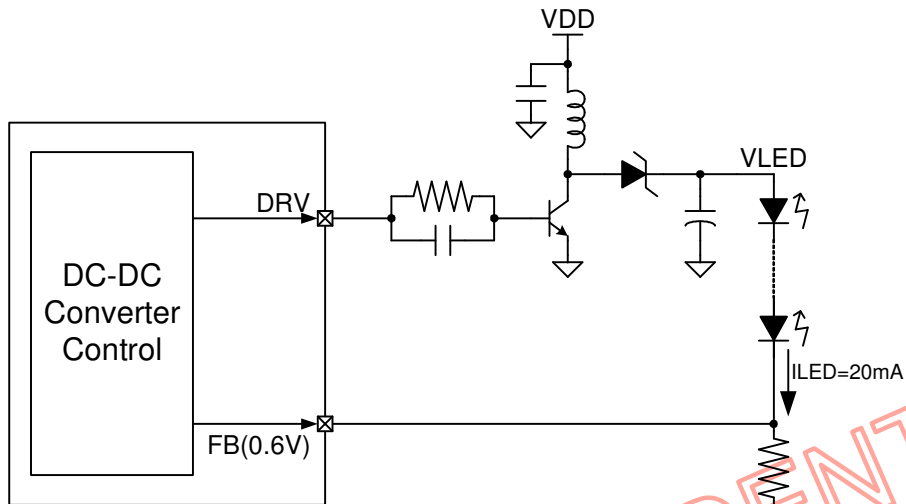
System block diagram



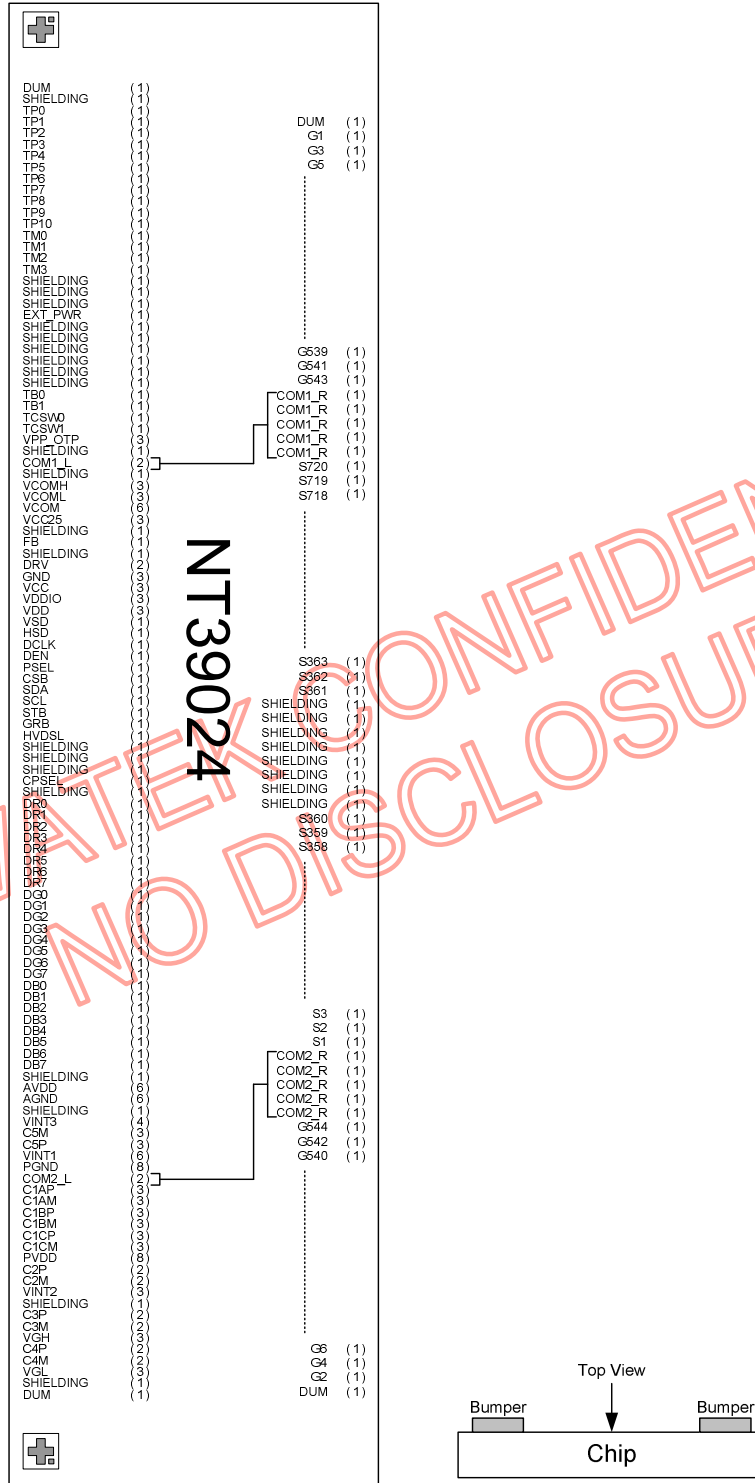
Application Block Diagram


Charge Pump Circuit Block


DC-DC Control Circuit



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Pad Sequence (bump side)


Pin Descriptions

Designation	I/O	Description
HSD	I (VDDIO)	Horizontal Sync input. Negative polarity. *Remark: Internal pulled weak high
VSD	I (VDDIO)	Vertical Sync input. Negative polarity. *Remark: Internal pulled weak high
DCLK	I (VDDIO)	Clock signal. Latching data at the rising edge.
DEN	I (VDDIO)	Data input Enable. Active High to enable the data input Bus under "DE Mode". *Remark: Internal pulled weak low
PSEL	I (VDDIO)	Parallel 24-bit and Serial 8-bit data input selection. PSEL="H", Parallel 24-bit RGB input through DR0~DR7, DB0~DB7, DG0~DG7 PSEL="L", Serial 8-bit data input through DR0~DR7 *Remark: Internal pulled high
DR0~DR7	I (VDDIO)	When PSEL="H", these will be treated as 8-bit Red data input. When PSEL="L", these will be treated as serial 8-bit digital data input.
DG0~DG7	I (VDDIO)	8-bit digital Green data input, only valid when PSEL="H" (Parallel mode). *Remark: Internal pulled weak low
DB0~DB7	I (VDDIO)	8-bit digital Blue data input, only valid when PSEL="H" (Parallel mode). *Remark: Internal pulled weak low
CSB	I (VDDIO)	Serial communication chip select. *Remark: Internal pulled weak high
SDA	I/O (VDDIO)	Serial communication data input. *Remark: Internal pulled low
SCL	I (VDDIO)	Serial communication clock input. *Remark: Internal pulled weak low
STB	I (VDDIO)	Standby setting for testing, it should be connected to VDDIO in normal operation mode. If connected to GND, the IC is in standby mode. *Remark: Internal pulled high
GRB	I (VDDIO)	Global reset pin, it should be connected to VDDIO in normal operating mode. If connected to GND, the timing controller is in reset state, suggest to be connected with a RC reset circuit for stability.
HVDSL	I (VDDIO)	HV mode or DE mode control signal. HVDSL="H": Set under HV mode, VSD and HSD signal have to provide by system. HVDSL="L": Set under DE mode, DE signal have to provide by system. *Remark: Internal pulled low
CPSEL	I (VDDIO)	Charge pump structure select pin. CPSEL="H", C1CP/M are connected to capacitor. CPSEL="L", C1CP/M are floating. *Remark: Internal pulled low
EXT_PWR	I (VDDIO)	External power control pin. EXT_PWR="H": VINT1 could be input externally. EXT_PWR="L": VINT1 is generated by charge pump circuit. *Remark: Internal pulled low
DC-DC Converter		
FB	I	Main boost regulator feedback input. Connect feedback resistive divider to GND. FB threshold is 0.6V nominal.
DRV	O	Power transistor gate signal for the boost converter.
Power		

VDD	PI	Power supply for digital circuits
GND	PI	Ground for digital circuits.
PVDD	PI	Power supply for analog circuits.
PGND	PI	Ground pin for power circuits.
AGND	PI	Ground pin for analog circuits.
VDDIO	PI	Power supply for logic I/O.
VPP_OTP	PI	Customer OTP power input pin.
VCC25	C	Power setting capacitor connect pin.
VCC	C	Capacitor connect pin for internal regulator.
AVDD	C	Power setting capacitor connect pin.
VINT1	C	Power setting capacitor connect pin.
VINT2	C	Power setting capacitor connect pin.
VINT3	C	Power setting capacitor connect pin.
VGH	C	Power setting capacitor connect pin.
VGL	C	Power setting capacitor connect pin.
C1AP/M C1BP/M C1CP/M C2P/M C3P/M C4P/M C5P/M	C	Capacitor connect pin for internal charge pump. Refer to the section of "Power Circuit" for the application.
VCOM Generator		
VCOM	O	Panel COMMON plate output.
VCOMH	C	Power supply for panel COMMON plate high level output.
VCOML	C	Power supply for panel COMMON plate low level output.
Source Driver		
S1~S720	O	Source driver output signals.
Gate Driver		
G1~G544	O	Gate driver output signals.
Other		
ALIGN_R ALIGN_L	M	For assembly alignment.
COM1_L COM1_R	S	The internal link together between input side and output side.
COM2_L COM2_R	S	The internal link together between input side and output side.
TM0~TM3 TP0~TP10	T	Test pins for NOVATEK internal testing only. *Remark: Not connected.
TB0 TB1 TB2 TB3	T	Test pins for testing. *Remark: Not connected.
TCSW0 TCSW1	T	Test pins for testing. *Remark: Not connected.
SHIELDING	S	This pin is connected to VGL internally. *Remark: Not connected.
DUM	D	Dummy pads. This pin is floating.

Note:

I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, T: Testing
I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

NT39024 Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_L	COM1_R
2	COM2_L	COM2_R

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3-Wire Serial Port Interface

3-Wire Command Format

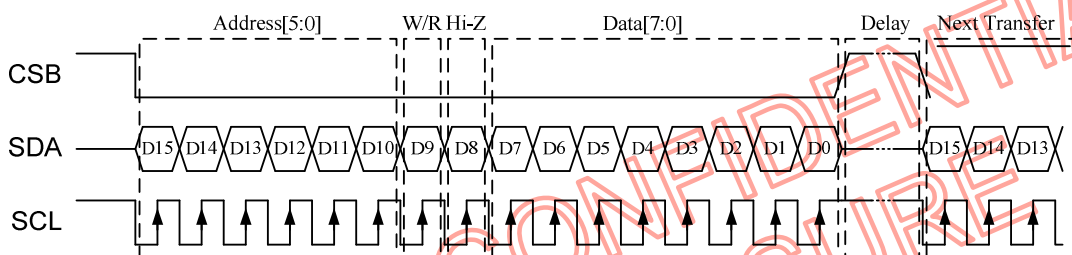
NT39024 use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. NT39024 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of "3-Wire Timing Diagram" for the detail timing.



3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. "0" for Write; "1" for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	X	DATA (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	Hi-Z	DATA (Issue by 3-Wire engine)							

3-Wire Control Registers

Following table list all the 3-Wire control registers and bit name definition for NT39024. Refer to the next section for detail register function description, please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

NT39024 3-Wire Control Register List

NO.	Address						R/W	D8	MSB	Initial value						LSB
	D15	D14	D13	D12	D11	D10				D9	D7	D6	D5	D4	D3	
R0	0	0	0	0	0	0	R/W(0)	X	HSDPOL	VSDPOL	CLKPOL	FPOL	NFSEL	FRAD		DITHB
									0	0	0	0	0	0	0	0
R1	0	0	0	0	0	1	R/W(0)	X	X	X	X	LHL	STB	GRB	SHLR	UPDN
												1	1	1	1	1
R2	0	0	0	0	1	0	R/W(0)	X	X	VFBSEL[1:0]		DRV_FREQ	PWM_DUTY[2:0]		SHDB	
										0	1	0	0	1	1	0
R3	0	0	0	0	1	1	R/W(0)	X	LED_ON_CYCLE[3:0]			LED_ON_RATIO[3:0]				
									0	1	1	1	1	1	1	1
R4	0	0	0	1	0	0	R/W(0)	X	DDL[7:0]							
									0	0	1	0	1	0	0	0
R5	0	0	0	1	0	1	R/W(0)	X	X	X	X	HDL[4:0]				
												0	1	0	0	0
R6	0	0	0	1	1	0	R/W(0)	X	OTP_VCOMH	VCOMH[6:0]						
									0	1	0	0	1	1	0	1
R7	0	0	0	1	1	1	R/W(0)	X	OTP_VCOML	VCOML[6:0]						
									0	0	0	1	1	0	1	1
R8	0	0	1	0	0	0	R/W(0)	X	BRI[7:0]							
									0	1	0	0	0	0	0	0
R9	0	0	1	0	0	1	R/W(0)	X	CON_B[7:0]							
									0	1	0	0	0	0	0	0
R10	0	0	1	0	1	0	R/W(0)	X	X	SUB_BRI_R[6:0]						
										1	0	0	0	0	0	0
R11	0	0	1	0	1	1	R/W(0)	X	X	SUB_CON_R[6:0]						
										1	0	0	0	0	0	0
R12	0	0	1	1	0	0	R/W(0)	X	X	SUB_BRI_B[6:0]						
										1	0	0	0	0	0	0
R13	0	0	1	1	0	1	R/W(0)	X	X	SUB_CON_B[6:0]						
										1	0	0	0	0	0	0
R14	0	0	1	1	1	0	R/W(0)	X	X	X	V2GAM[3:0]			GAMEN	X	
											1	0	0	0	0	
R15	0	0	1	1	1	1	R/W(0)	X	V4GAM[3:0]			V3GAM[3:0]				
									1	0	0	0	1	0	0	0
R16	0	1	0	0	0	0	R/W(0)	X	V6GAM[3:0]			V5GAM[3:0]				
									1	0	0	0	1	0	0	0
R17	0	1	0	0	0	1	R/W(0)	X	V8GAM[3:0]			V7GAM[3:0]				
									1	0	0	0	1	0	0	0
R18	0	1	0	0	1	0	R/W(0)	X	X	X	X	V9GAM[3:0]				
												1	0	0	0	
R19	0	1	0	0	1	1	R/W(0)	X	X	X	X	VGL_SEL[2:0]		VGH_SEL[2:0]		
												1	1	1	1	
R20	0	1	0	1	0	0	R/W(0)	X	TRMEN[7:0]							
									0	0	0	0	0	0	0	0

R21	0	1	0	1	0	1	R/W(0)	X	V13GAM[3:0]				V12GAM[3:0]			
									1	0	0	0	1	0	0	0
R22	0	1	0	1	1	0	R/W(0)	X	V15GAM[3:0]				V14GAM[3:0]			
									1	0	0	0	1	0	0	0
R23	0	1	0	1	1	1	R/W(0)	X	V17GAM[3:0]				V16GAM[3:0]			
									1	0	0	0	1	0	0	0
R24	0	1	1	0	0	0	R/W(0)	X	V19GAM[3:0]				V18GAM[3:0]			
									1	0	0	0	1	0	0	0

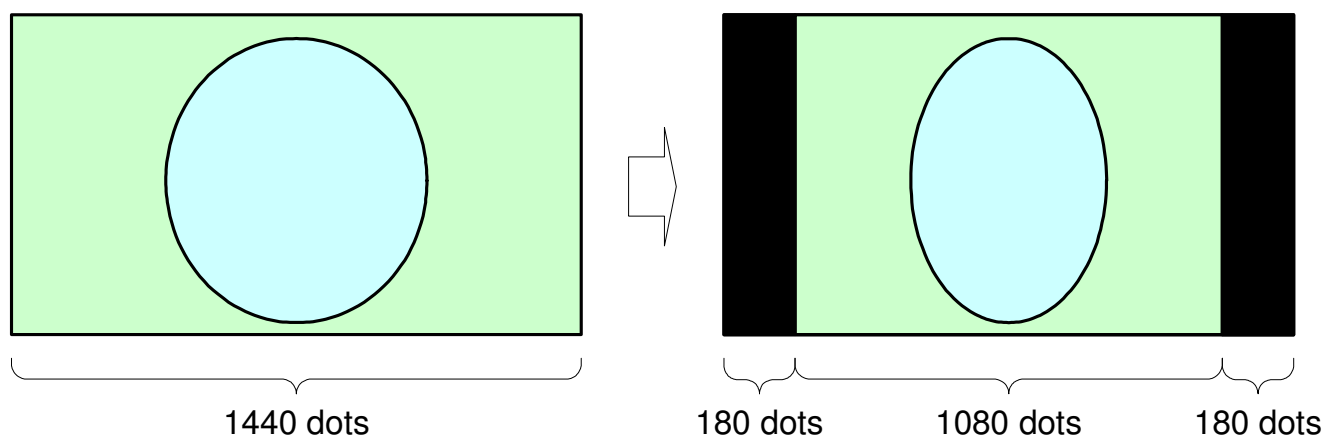
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3-wire Registers Function Description

R0: Timing Controller Function Register

Designation	Address	Description																					
DITHB	R0[0]	Dithering control bit. DITHB="1": Dithering off, (7-bits resolution, truncation last 1-bits of the input data) DITHB="0": Dithering on, (Pseudo 8-bits resolution). (Default)																					
FRAD[1:0]	R0[2:1]	Odd frame or Even frame advance control																					
		<table border="1"> <thead> <tr> <th>FRAD1</th> <th>FRAD0</th> <th>Advance Frame</th> <th>Notes</th> <th rowspan="5">Unit: H</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Default</td> <td>Odd/Even frame Tstv are the same</td> </tr> <tr> <td>0</td> <td>1</td> <td>Odd frame</td> <td>Even frame Tstv=HDL setting+1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Even frame</td> <td>Odd frame Tstv=HDL +1</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserve</td> <td>Reserve</td> </tr> </tbody> </table>	FRAD1	FRAD0	Advance Frame	Notes	Unit: H	0	0	Default	Odd/Even frame Tstv are the same	0	1	Odd frame	Even frame Tstv=HDL setting+1	1	0	Even frame	Odd frame Tstv=HDL +1	1	1	Reserve	Reserve
		FRAD1	FRAD0	Advance Frame	Notes	Unit: H																	
		0	0	Default	Odd/Even frame Tstv are the same																		
		0	1	Odd frame	Even frame Tstv=HDL setting+1																		
1	0	Even frame	Odd frame Tstv=HDL +1																				
1	1	Reserve	Reserve																				
NFSEL	R0[3]	Narrow display mode selection bit. NFSEL="1": Narrow display format is enable. NFSEL="0": Normally display. (Default)																					
FPOL	R0[4]	VCOM polarity inverse control bit. When FPOL="1", VCOM inverse polarity. When FPOL="0", VCOM normal polarity. (Default)																					
CLKPOL	R0[5]	DCLK polarity control bit. CLKPOL="1": Data sampling at DCLK falling edge. CLKPOL="0": Data sampling at DCLK rising edge. (Default)																					
VSDPOL	R0[6]	VSD polarity control bit. VSDPOL="1": VSD positive polarity. VSDPOL="0": VSD negative polarity. (Default)																					
HSDPOL	R0[7]	HSD polarity control bit. HSDPOL="1": HSD positive polarity. HSDPOL="0": HSD negative polarity. (Default)																					

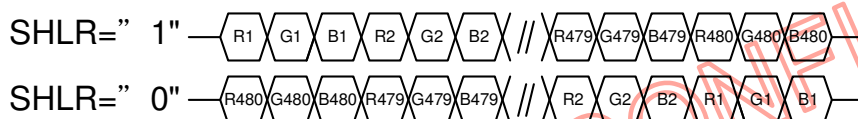
Narrow display mode



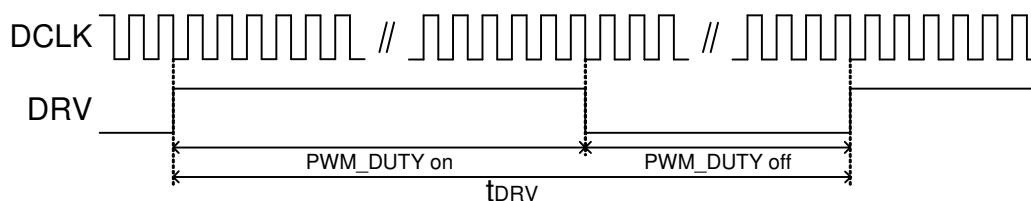
R1: Timing Controller Function Register

Designation	Address	Description
UPDN	R1[0]	Gate driver Up/Down scan control of gate driver. UPDN="1", Shift from up to down, First line=L1->L2-> ... ->L543->L544=Last line (Default) UPDN="0", Shift from down to up, First line=L544->L543-> ... ->L2->L1=Last line
SHLR	R1[1]	Right/Left sequence control of source driver. SHLR="1", Shift right: First data=S1->S2->S3 ... ->S720=Last data (Default) SHLR="0", Shift left: Last data=S1<-S2<-S3 ... <-S720=First data
GRB	R1[2]	Global reset bit. GRB="1", Normal operation. (Default) GRB="0", The controller is in reset state.
STB	R1[3]	Standby mode selection bit. STB="1", Normal operation. (Default) STB="0", Timing control, driver and DC-DC converter, are off, and all outputs are High-Z.
LHL	R1[4]	Line/Half-Line inversion selection bit. LHL="1", Line inversion. (Default) LHL="0", Half line inversion.

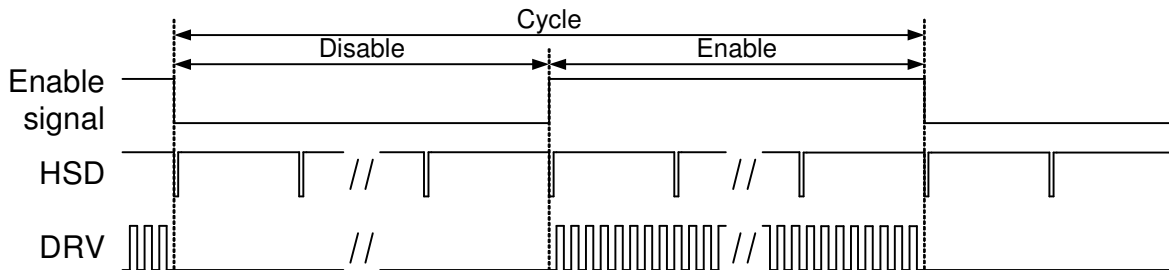
NOTE: When SHLR="0", input RGB sequence have no need to sweep in serial mode.


R2: Black light Controller Function Register

Designation	Address	Description																																				
SHDB	R2[0]	Shut down for back light power converter. STDB="1", The back light power converter is controlled by STB's power on/off sequence STDB="0", The back light power converter is off. (Default)																																				
PWM_DUTY [2:0]	R2[3:1]	PWM duty cycle selection for back light power convert																																				
		<table border="1"> <thead> <tr> <th>PWM_DUTY2</th> <th>PWM_DUTY1</th> <th>PWM_DUTY0</th> <th>PWM duty cycle</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>50%</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>60%</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>65%</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>70%(Default)</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>75%</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>80%</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>85%</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>90%</td> </tr> </tbody> </table>	PWM_DUTY2	PWM_DUTY1	PWM_DUTY0	PWM duty cycle	0	0	0	50%	0	0	1	60%	0	1	0	65%	0	1	1	70%(Default)	1	0	0	75%	1	0	1	80%	1	1	0	85%	1	1	1	90%
		PWM_DUTY2	PWM_DUTY1	PWM_DUTY0	PWM duty cycle																																	
		0	0	0	50%																																	
		0	0	1	60%																																	
		0	1	0	65%																																	
		0	1	1	70%(Default)																																	
		1	0	0	75%																																	
1	0	1	80%																																			
1	1	0	85%																																			
1	1	1	90%																																			
DRV_FREQ	R2[4]	DRV signal frequency setting DRV_FREQ="1", DRV frequency is DCLK/64. DRV_FREQ="0", DRV frequency is DCLK/32. (Default)																																				
VFBSEL[1:0]	R2[6:5]	FB voltage adjustable for DC-DC feedback threshold																																				
		<table border="1"> <thead> <tr> <th>VFBSEL1</th> <th>VFBSEL0</th> <th>Feedback threshold Voltage</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0.75</td> <td rowspan="5">V</td> </tr> <tr> <td>0</td> <td>1</td> <td>0.6(Default)</td> </tr> <tr> <td>1</td> <td>0</td> <td>0.45</td> </tr> <tr> <td>1</td> <td>1</td> <td>0.3</td> </tr> </tbody> </table>	VFBSEL1	VFBSEL0	Feedback threshold Voltage	Unit	0	0	0.75	V	0	1	0.6(Default)	1	0	0.45	1	1	0.3																			
		VFBSEL1	VFBSEL0	Feedback threshold Voltage	Unit																																	
		0	0	0.75	V																																	
		0	1	0.6(Default)																																		
1	0	0.45																																				
1	1	0.3																																				


R3: LED_ON setting Register

Designation	Address	Description				
LED_ON_RATIO[3:0]	R3[3:0]	Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.				
		LED_ON_RATIO3	LED_ON_RATIO2	LED_ON_RATIO1	LED_ON_RATIO0	Value
		0	0	0	0	1/16
		0	0	0	1	2/16
		0	0	1	0	3/16
		0	0	1	1	4/16
		0	1	0	0	5/16
		0	1	0	1	6/16
		0	1	1	0	7/16
		0	1	1	1	8/16
		1	0	0	0	9/16
		1	0	0	1	10/16
		1	0	1	0	11/16
		1	0	1	1	12/16
		1	1	0	0	13/16
		1	1	0	1	14/16
1	1	1	0	15/16		
1	1	1	1	16/16(Default)		
LED_ON_CYCLE[3:0]	R3[7:4]	Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.				
		LED_ON_CYCLE3	LED_ON_CYCLE2	LED_ON_CYCLE1	LED_ON_CYCLE0	Value
		0	0	0	0	1
		0	0	0	1	2
		0	0	1	0	3
		0	0	1	1	4
		0	1	0	0	5
		0	1	0	1	6
		0	1	1	0	7
		0	1	1	1	8(Default)
		1	0	0	0	9
		1	0	0	1	10
		1	0	1	0	11
		1	0	1	1	12
		1	1	0	0	13
		1	1	0	1	14
1	1	1	0	15		
1	1	1	1	16		



$$16 * \text{LED_ON_CYCLE} = \text{LED_ON_CYCLE} * (\text{LED_ON_RATIO} * 16) + \text{LED_ON_CYCLE} * (16 - \text{LED_ON_RATIO} * 16)$$

(Cycle)
(Enable)
(Disable)
Unit:HSD

R4: Data delay setting

Designation	Address	Description		
DDL[7:0]	R4[7:0]	Select the HSD signal to 1'st input data delay timing.		
		DDL[7:0]	DDL function	Unit
		24H	36(Minimum setting for Parallel mode)	DCLK
		:	:	
		28H	40(Default setting for Parallel mode)	
		:	:	
		6CH	108(Minimum setting for Serial mode)	
		:	:	
		78H	120(Default setting for Serial mode)	
:	:			
FFH	255			

Note: DDL function will be disabled under 8/24 bit DE mode.

R5: HSD delay setting

Designation	Address	Description		
HDL[4:0]	R5[4:0]	Select the Gate start pulse output delay timing.		
		HDL[4:0]	HDL function	Unit
		02H	2(minimum setting)	HSD
		:	:	
		08H	8(Default)	
		:	:	
1FH	31			

Note: HDL function will be disabled under 8/24 bit DE mode.

R6: VCOMH level control Register

Designation	Address	Description		
VCOMH[6:0]	R6[6:0]	VCOMH level adjustment. (20mV/LSB)		
		VCOMH[6:0]	VCOMH level	Unit
		00H	2.46	V
		:	:	
		1BH	3	
		:	:	
		4DH	4	
:	:			

			7FH	5	
OTP_VCOMH	R6[7]	VCOMH data source selection register OTP_VCOMH="1", VCOMH is switch to the 3-wire register memory when user want to adjust the VCOMH level. OTP_VCOMH="0", VCOMH is read from OTP memory. (Default)			

Note: VCOMH setting have to greater then PVDD.

R7: VCOML control Register

Designation	Address	Description			
VCOML[6:0]	R7[6:0]	VCOML level adjustment. (20mV/LSB)			
		VCOML[6:0]	VCOML level	Unit	V
		00H	-0.46	:	
		:	:	:	
		1BH	-1(Default)	:	
		:	:	:	
		4DH	-2	:	
:	:	:			
		7FH	-3		
OTP_VCOML	R7[7]	VCOML data source selection register OTP_VCOML="1", VCOML is switch to the 3-wire register memory when user want to adjust the VCOML level. OTP_VCOML="0", VCOML is read from OTP memory. (Default)			

R8: Brightness Control Register

Designation	Address	Description		
BRI[7:0]	R8[7:0]	Brightness level setting, the gain changes 1 step/bit		
		BRI[7:0]	Brightness gain	
		00H	Dark (-64)	:
		:	:	:
		40H	Center (0) (Default)	:
		:	:	:
		FFH	Bright (+191)	

R9: Contrast Control Register

Designation	Address	Description		
CON[7:0]	R9[7:0]	Contrast level setting, the gain changes (1/64)/bit		
		CON[7:0]	Contrast gain	
		00H	0	:
		:	:	:
		40H	1(Default)	:
		:	:	:
		FFH	3.984	

R10: SUB Brightness R Control Register

Designation	Address	Description		
SUB_BRI_R [6:0]	R10[6:0]	Red sub-pixel brightness level setting, setting accuracy: 1 step/bit		
		SUB_BRI_R[7:0]	R Brightness gain	
		00H	Dark (-64)	

			:	:
			40H	Center (0) (Default)
			:	:
			7FH	Bright (+63)

R11: SUB_Contrast_R Control Register

Designation	Address	Description		
SUB_CON_R[6:0]	R11[6:0]	Red sub-pixel contrast level setting, the gain changes (1/256)/bit		
			SUB_CON_R[7:0]	R Contrast gain
			00H	0.75
			:	:
			40H	1(Default)
			7FH	1.246

R12: SUB_Brightness_B Control Register

Designation	Address	Description		
SUB_BRI_B [6:0]	R12[6:0]	Blue sub-pixel brightness level setting, setting accuracy: 1 step/bit		
			SUB_BRI_B[7:0]	B Brightness gain
			00H	Dark (-64)
			:	:
			40H	Center (0) (Default)
			7FH	Bright (+63)

R13: SUB_Contrast_B Control Register

Designation	Address	Description		
SUB_CON_B[6:0]	R13[6:0]	Blue sub-pixel contrast level setting, the gain changes (1/256)/bit		
			SUB_CON_B[7:0]	B Contrast gain
			00H	0.75
			:	:
			40H	1(Default)
			7FH	1.246

R14: VGAM2 Level Control Register

Designation	Address	Description
-	R14[0]	Reserve
GAMEN	R14[1]	GAMMA adjustment enable control bit.(adjustable voltage for V2-V9 and V12-V19) GAMEN="1", Gamma correction enabled GAMEN="0", Gamma correction disabled.
V2GAM[3:0]	R14[5:2]	V2 GAMMA voltage level setting. Adjust level = 20mV / Step

R15: VGAM3/4 Level Control Register

Designation	Address	Description
V3GAM[3:0]	R15[3:0]	V3 GAMMA voltage level setting. Adjust level = 20mV / Step

V4GAM[3:0]	R15[7:4]	V4 GAMMA voltage level setting. Adjust level = 20mV / Step
------------	----------	---

R16: VGAM5/6 Level Control Register

Designation	Address	Description
V5GAM[3:0]	R16[3:0]	V5 GAMMA voltage level setting. Adjust level = 20mV / Step
V6GAM[3:0]	R16[7:4]	V6 GAMMA voltage level setting. Adjust level = 20mV / Step

R17: VGAM7/8 Level Control Register

Designation	Address	Description
V7GAM[3:0]	R17[3:0]	V7 GAMMA voltage level setting. Adjust level = 20mV / Step
V8GAM[3:0]	R17[7:4]	V8 GAMMA voltage level setting. Adjust level = 20mV / Step

R18: VGAM9 Level Control Register

Designation	Address	Description
V9GAM[3:0]	R18[3:0]	V9 GAMMA voltage level setting. Adjust level = 20mV / Step

VxGAM Level Control Register Setting Table

VxGMA[3:0]	VCOM=H	Unit	Note
00H	+160	mV	Refer to the Gamma Table for the default voltage level of V2~V9 x = 2, 3, 4, 5, 6, 7, 8, 9
:	:		
08H	VXGAM(Default)		
:	:		
0FH	-140		

R19: VGH/VGL output voltage selection

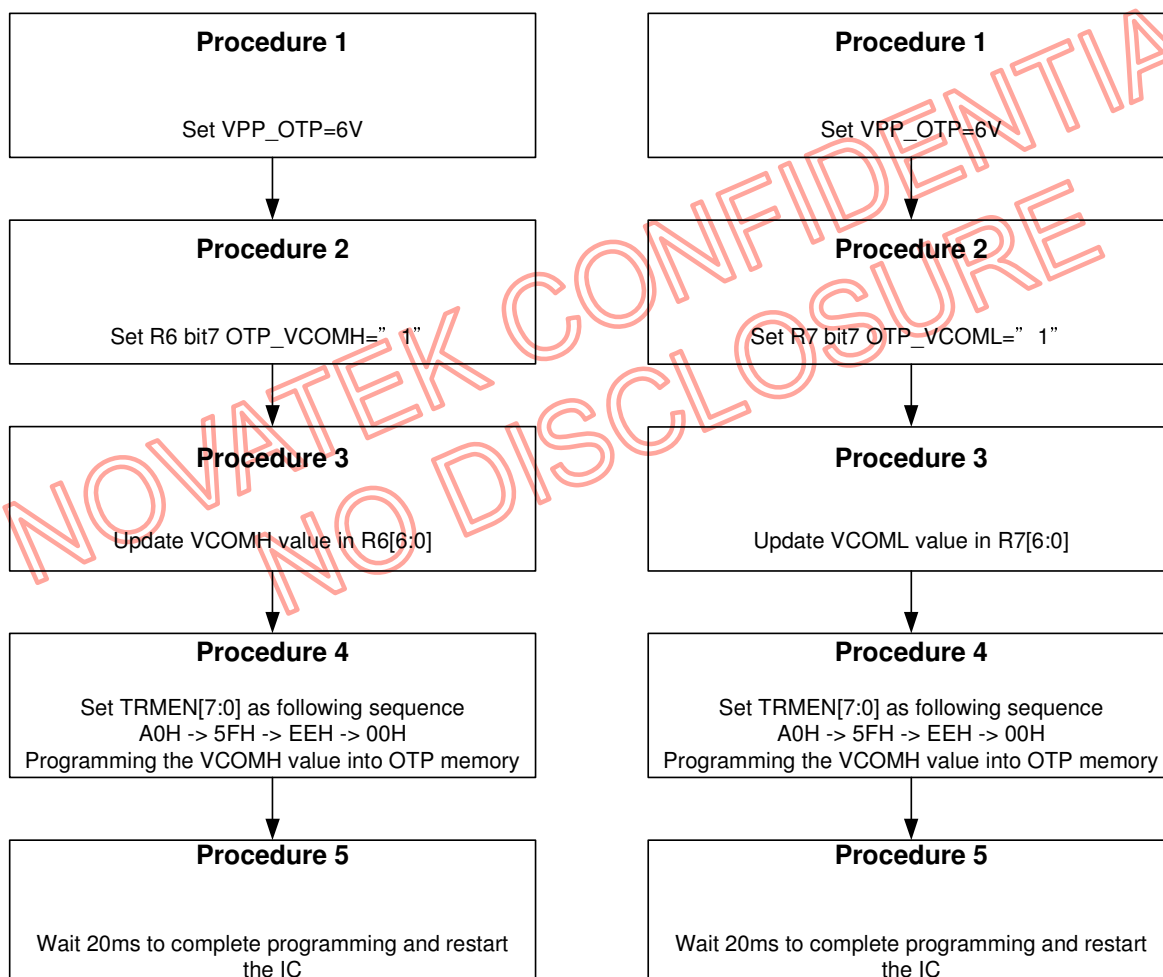
Designation	Address	Description			
VGH_SEL[1:0]	R19[1:0]	VGH output voltage selection			
		VGH_SEL1	VGH_SEL0	VGH voltage	Unit
		0	0	12	V
		0	1	13	
		1	0	14	
1	1	15(Default)			
VGL_SEL[1:0]	R19[3:2]	VGL output voltage selection			
		VGL_SEL1	VGL_SEL0	VGL voltage	Unit
		0	0	-7	V
		0	1	-8	
		1	0	-9	
1	1	-10(Default)			

Note: tolerance= $\pm 0.5V$

R20: TRMEN Register

Designation	Address	Description
TRMEN[7:0]	R20[7:0]	VCOMH and VCOML trim function control register. Write the follow command sequentially to enable the VCOMH or VCOML trim function. Adjust VCOMH level: Set TRMEN[7:0]=00H and write proper VCOMH[7:0] or VCOML[7:0] value using 3-wire commend. Programming the VCOMH or VCOML value into OTP memory: Set TRMEN[7:0] as following sequence A0H->5FH->EEH->00H OTP_VCOMH or OTP_VCOML will be clear to 0b after the programming procedure.

Note: The trim block can be written for only 2 times. Trim command exceed the limit may cause the VCOMH/VCOML output unknown value.

The procedures of OTP function for VCOMH and VCOML.


Note: DCLK frequency of parallel mode and serial mode are 9MHz and 27MHz respectively.

R21: VGAM12/13 Level Control Register

Designation	Address	Description
V12GAM[3:0]	R21[3:0]	V12 GAMMA voltage level setting. Adjust level = 20mV / Step
V13GAM[3:0]	R21[7:4]	V13 GAMMA voltage level setting. Adjust level = 20mV / Step

R22: VGAM14/15 Level Control Register

Designation	Address	Description
V14GAM[3:0]	R22[3:0]	V14 GAMMA voltage level setting. Adjust level = 20mV / Step
V15GAM[3:0]	R22[7:4]	V15 GAMMA voltage level setting. Adjust level = 20mV / Step

R23: VGAM16/17 Level Control Register

Designation	Address	Description
V16GAM[3:0]	R23[3:0]	V16 GAMMA voltage level setting. Adjust level = 20mV / Step
V17GAM[3:0]	R23[7:4]	V17 GAMMA voltage level setting. Adjust level = 20mV / Step

R24: VGAM18/19 Level Control Register

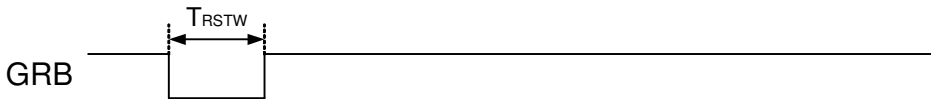
Designation	Address	Description
V18GAM[3:0]	R24[3:0]	V18 GAMMA voltage level setting. Adjust level = 20mV / Step
V19GAM[3:0]	R24[7:4]	V19 GAMMA voltage level setting. Adjust level = 20mV / Step

VxGAM Level Control Register Setting Table

VxGMA[3:0]	VCOM=L	Unit	Note
00H	+160	mV	Refer to the Gamma Table for the default voltage level of V12~ V19 x = 12, 13, 14, 15, 16, 17, 18, 19
:	:		
08H	VXGAM(Default)		
:	:		
0FH	-140		

Functional Descriptions

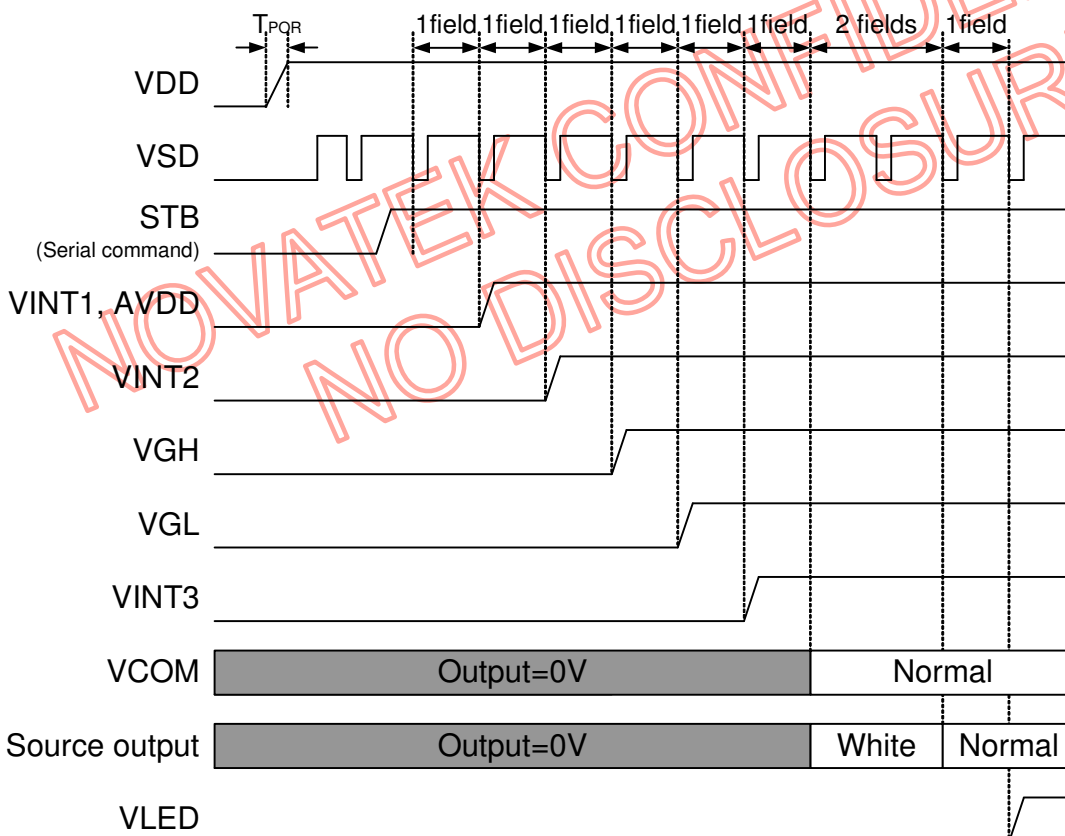
Global Reset Time (GRB ...pin control)

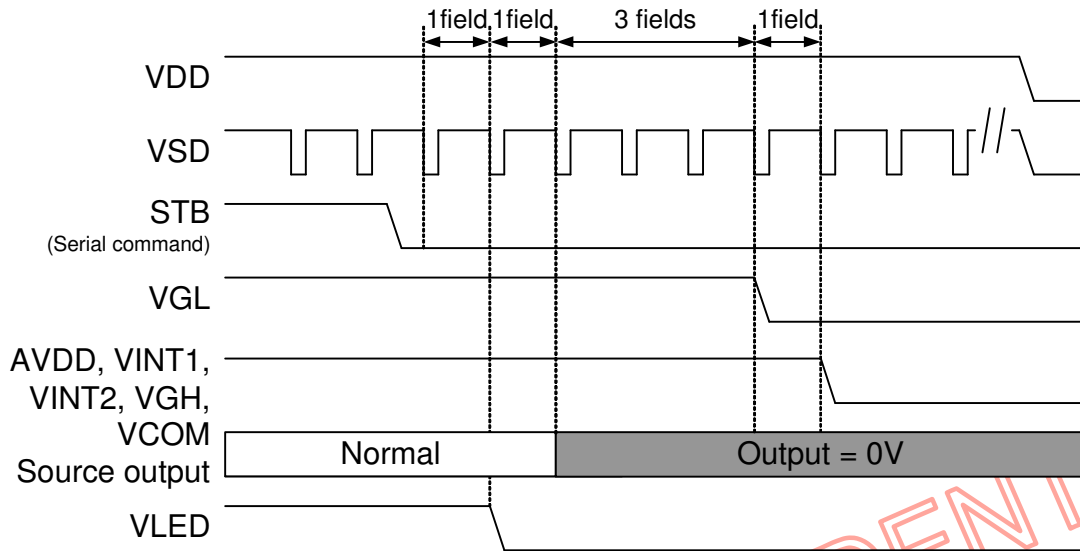


Power on/off sequence:

This IC is a high-voltage LCD driver, so it may be damaged by a large current flow if an incorrect power sequence is used. Connecting the drive powers, VEE & VGG, after the logical power, VCC, is the recommended sequence. When shutting off the power, shut off the drive power and then the logic system or turn off all power simultaneously.

■ Power on sequence



■ Power off sequence


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Input Data and Output Voltage

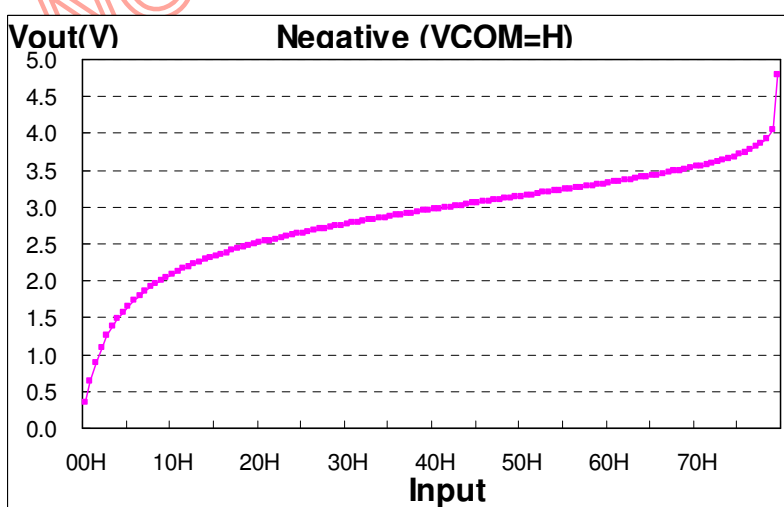
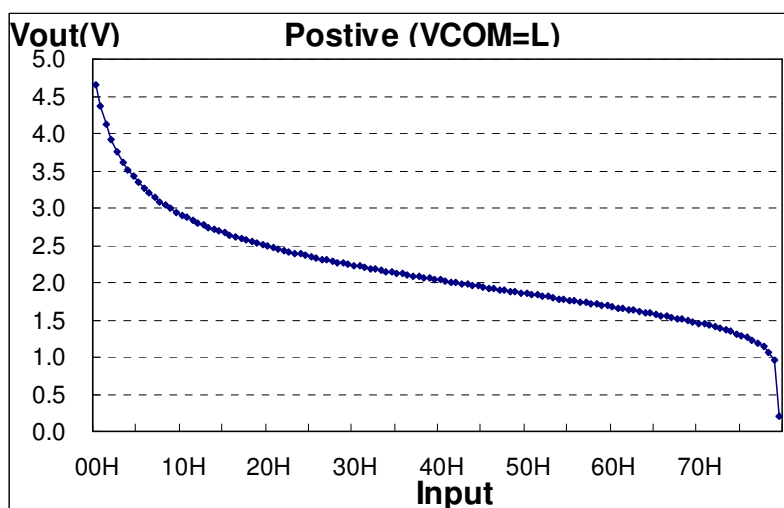
Source driver data output sequence can be control by "SHLR".

Output	S1	S2	S3	---	S718	S719	S720
SHLR="1"	First data						Last data
SHLR="0"	Last data						First data

Gate driver scan output sequence can be control by "UPDN".

Output	G1	G2	G3	---	G542	G543	G544
UPDN="1"	First data						Last data
UPDN="0"	Last data						First data

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.



Input Data and Output Voltage Reference Table

Note: Gamma Tables vary for each customer. Contact Novatek for more detailed information.

Vno.	Data	VCOMOUT=H	Vno.	Data	VCOMOUT=H
V1	00H	VDDA X 0.070		40H	VDDA X 0.594
	01H	VDDA X 0.128		41H	VDDA X 0.596
	02H	VDDA X 0.177		42H	VDDA X 0.598
	03H	VDDA X 0.218		43H	VDDA X 0.601
	04H	VDDA X 0.251		44H	VDDA X 0.603
	05H	VDDA X 0.277		45H	VDDA X 0.605
	06H	VDDA X 0.297		46H	VDDA X 0.608
	07H	VDDA X 0.315		47H	VDDA X 0.610
	08H	VDDA X 0.331	V5	48H	VDDA X 0.612
	09H	VDDA X 0.346		49H	VDDA X 0.614
	0AH	VDDA X 0.359		4AH	VDDA X 0.617
	0BH	VDDA X 0.371		4BH	VDDA X 0.619
	0CH	VDDA X 0.382		4CH	VDDA X 0.621
	0DH	VDDA X 0.393		4DH	VDDA X 0.623
	0EH	VDDA X 0.402		4EH	VDDA X 0.626
	0FH	VDDA X 0.411		4FH	VDDA X 0.628
	10H	VDDA X 0.419		50H	VDDA X 0.630
	11H	VDDA X 0.426		51H	VDDA X 0.632
V2	12H	VDDA X 0.433		52H	VDDA X 0.634
	13H	VDDA X 0.439		53H	VDDA X 0.636
	14H	VDDA X 0.445		54H	VDDA X 0.638
	15H	VDDA X 0.451		55H	VDDA X 0.641
	16H	VDDA X 0.457		56H	VDDA X 0.643
	17H	VDDA X 0.462		57H	VDDA X 0.645
	18H	VDDA X 0.467		58H	VDDA X 0.647
	19H	VDDA X 0.472		59H	VDDA X 0.649
	1AH	VDDA X 0.477	V6	5AH	VDDA X 0.652
	1BH	VDDA X 0.481		5BH	VDDA X 0.654
	1CH	VDDA X 0.486		5CH	VDDA X 0.656
	1DH	VDDA X 0.490		5DH	VDDA X 0.658
	1EH	VDDA X 0.495		5EH	VDDA X 0.661
	1FH	VDDA X 0.499		5FH	VDDA X 0.663
	20H	VDDA X 0.503		60H	VDDA X 0.665
	21H	VDDA X 0.506		61H	VDDA X 0.668
	22H	VDDA X 0.510		62H	VDDA X 0.670
	23H	VDDA X 0.514		63H	VDDA X 0.672
V3	24H	VDDA X 0.517		64H	VDDA X 0.675
	25H	VDDA X 0.521		65H	VDDA X 0.677
	26H	VDDA X 0.524		66H	VDDA X 0.680
	27H	VDDA X 0.527		67H	VDDA X 0.683
	28H	VDDA X 0.531		68H	VDDA X 0.685
	29H	VDDA X 0.534		69H	VDDA X 0.688
	2AH	VDDA X 0.537		6AH	VDDA X 0.691
	2BH	VDDA X 0.540	V7	6BH	VDDA X 0.693
	2CH	VDDA X 0.543		6CH	VDDA X 0.697
	2DH	VDDA X 0.546		6DH	VDDA X 0.700
	2EH	VDDA X 0.548		6EH	VDDA X 0.703
	2FH	VDDA X 0.551		6FH	VDDA X 0.706
	30H	VDDA X 0.554		70H	VDDA X 0.709
	31H	VDDA X 0.557		71H	VDDA X 0.712
	32H	VDDA X 0.560		72H	VDDA X 0.716
	33H	VDDA X 0.562		73H	VDDA X 0.719
	34H	VDDA X 0.565		74H	VDDA X 0.723
	35H	VDDA X 0.567		75H	VDDA X 0.728
V4	36H	VDDA X 0.570		76H	VDDA X 0.732
	37H	VDDA X 0.572	V8	77H	VDDA X 0.737
	38H	VDDA X 0.575		78H	VDDA X 0.742
	39H	VDDA X 0.577		79H	VDDA X 0.748
	3AH	VDDA X 0.580		7AH	VDDA X 0.755
	3BH	VDDA X 0.582		7BH	VDDA X 0.763
	3CH	VDDA X 0.584		7CH	VDDA X 0.772
	3DH	VDDA X 0.587	V9	7DH	VDDA X 0.786
	3EH	VDDA X 0.589		7EH	VDDA X 0.810
	3FH	VDDA X 0.592	V10	7FH	VDDA X 0.960

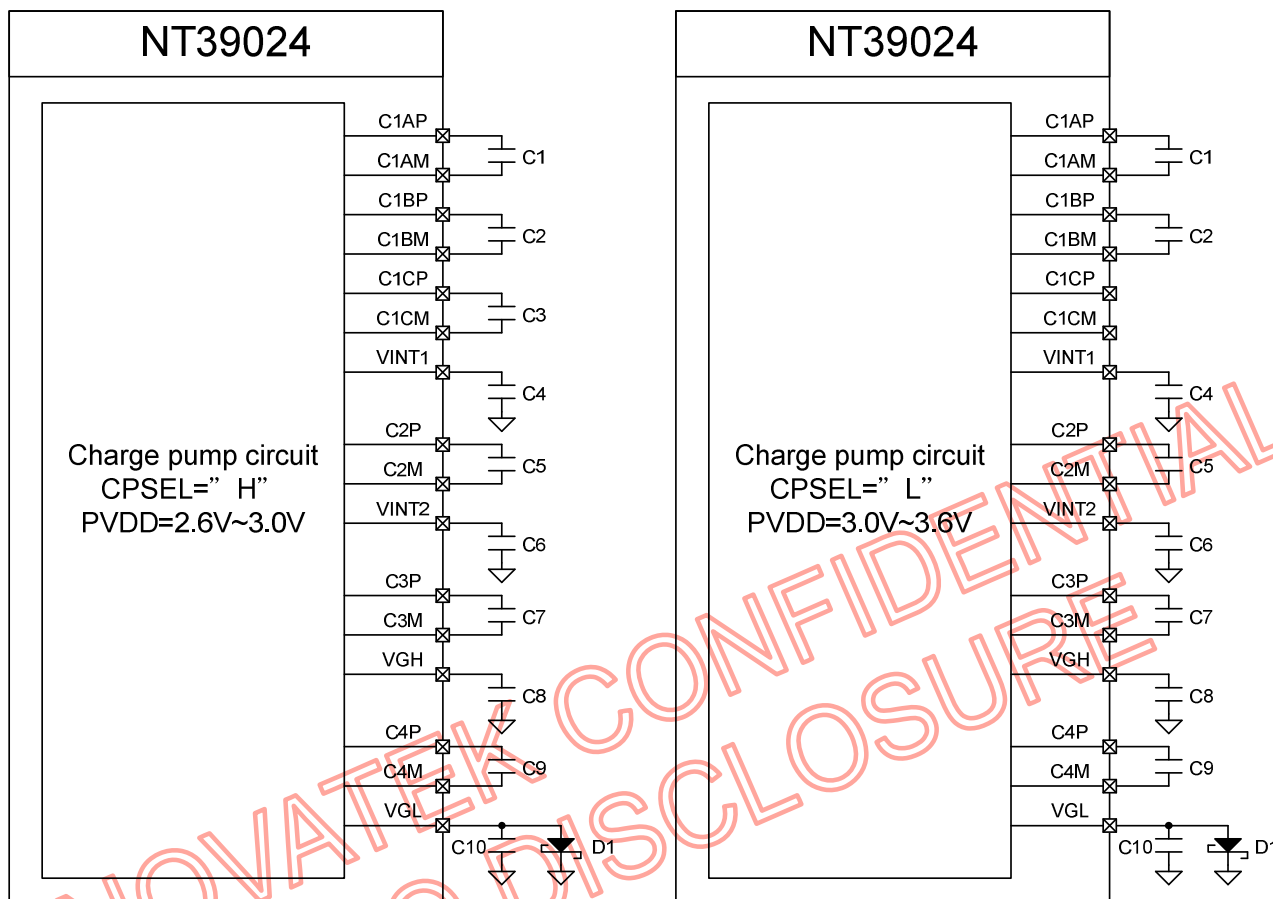
Vno.	Data	VCOMOUT=L	Vno.	Data	VCOMOUT=L
V20	00H	VDDA X 0.930		40H	VDDA X 0.406
	01H	VDDA X 0.872		41H	VDDA X 0.404
	02H	VDDA X 0.823		42H	VDDA X 0.402
	03H	VDDA X 0.782		43H	VDDA X 0.399
	04H	VDDA X 0.749		44H	VDDA X 0.397
	05H	VDDA X 0.723		45H	VDDA X 0.395
	06H	VDDA X 0.703		46H	VDDA X 0.392
	07H	VDDA X 0.685		47H	VDDA X 0.390
	08H	VDDA X 0.669	V16	48H	VDDA X 0.388
	09H	VDDA X 0.654		49H	VDDA X 0.386
	0AH	VDDA X 0.641		4AH	VDDA X 0.383
	0BH	VDDA X 0.629		4BH	VDDA X 0.381
	0CH	VDDA X 0.618		4CH	VDDA X 0.379
	0DH	VDDA X 0.607		4DH	VDDA X 0.377
	0EH	VDDA X 0.598		4EH	VDDA X 0.374
	0FH	VDDA X 0.589		4FH	VDDA X 0.372
	10H	VDDA X 0.581		50H	VDDA X 0.370
	11H	VDDA X 0.574		51H	VDDA X 0.368
V19	12H	VDDA X 0.567		52H	VDDA X 0.366
	13H	VDDA X 0.561		53H	VDDA X 0.364
	14H	VDDA X 0.555		54H	VDDA X 0.362
	15H	VDDA X 0.549		55H	VDDA X 0.359
	16H	VDDA X 0.543		56H	VDDA X 0.357
	17H	VDDA X 0.538		57H	VDDA X 0.355
	18H	VDDA X 0.533		58H	VDDA X 0.353
	19H	VDDA X 0.528		59H	VDDA X 0.351
	1AH	VDDA X 0.523	V15	5AH	VDDA X 0.348
	1BH	VDDA X 0.519		5BH	VDDA X 0.346
	1CH	VDDA X 0.514		5CH	VDDA X 0.344
	1DH	VDDA X 0.510		5DH	VDDA X 0.342
	1EH	VDDA X 0.505		5EH	VDDA X 0.339
	1FH	VDDA X 0.501		5FH	VDDA X 0.337
	20H	VDDA X 0.497		60H	VDDA X 0.335
	21H	VDDA X 0.494		61H	VDDA X 0.332
	22H	VDDA X 0.490		62H	VDDA X 0.330
	23H	VDDA X 0.486		63H	VDDA X 0.328
V18	24H	VDDA X 0.483		64H	VDDA X 0.325
	25H	VDDA X 0.479		65H	VDDA X 0.323
	26H	VDDA X 0.476		66H	VDDA X 0.320
	27H	VDDA X 0.473		67H	VDDA X 0.317
	28H	VDDA X 0.469		68H	VDDA X 0.315
	29H	VDDA X 0.466		69H	VDDA X 0.312
	2AH	VDDA X 0.463		6AH	VDDA X 0.309
	2BH	VDDA X 0.460	V14	6BH	VDDA X 0.307
	2CH	VDDA X 0.457		6CH	VDDA X 0.303
	2DH	VDDA X 0.454		6DH	VDDA X 0.300
	2EH	VDDA X 0.452		6EH	VDDA X 0.297
	2FH	VDDA X 0.449		6FH	VDDA X 0.294
	30H	VDDA X 0.446		70H	VDDA X 0.291
	31H	VDDA X 0.443		71H	VDDA X 0.288
	32H	VDDA X 0.440		72H	VDDA X 0.284
	33H	VDDA X 0.438		73H	VDDA X 0.281
	34H	VDDA X 0.435		74H	VDDA X 0.277
	35H	VDDA X 0.433		75H	VDDA X 0.272
V17	36H	VDDA X 0.430		76H	VDDA X 0.268
	37H	VDDA X 0.428	V13	77H	VDDA X 0.263
	38H	VDDA X 0.425		78H	VDDA X 0.258
	39H	VDDA X 0.423		79H	VDDA X 0.252
	3AH	VDDA X 0.420		7AH	VDDA X 0.245
	3BH	VDDA X 0.418		7BH	VDDA X 0.237
	3CH	VDDA X 0.416		7CH	VDDA X 0.228
	3DH	VDDA X 0.413	V12	7DH	VDDA X 0.214
	3EH	VDDA X 0.411		7EH	VDDA X 0.190
	3FH	VDDA X 0.408	V11	7FH	VDDA X 0.040

Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Pin Name	Wiring resistance value(Ω)	Pin Name	Wiring resistance value(Ω)
VDD	<10	VCOML	<10
PVDD	<3	VGH	<10
GND	<10	VGL	<10
AGND	<10	DRV	<20
PGND	<3	FB	<50
VDDIO	<10	HSD	<50
VPP_OTP	<10	VSD	<50
VCC25	<10	DCLK	<50
VCC	<10	DEN	<50
AVDD	<10	DR0~DR7	<50
VINT1	<5	DG0~DG7	<50
VINT2,3	<10	DB0~DB7	<50
C1AP/M	<5	CSB	<50
C1BP/M	<5	SDA	<50
C1CP/M	<5	SCL	<50
C2P/M	<10	STB	<1000
C3P/M	<10	GRB	<1000
C4P/M	<10	HVDSL	<1000
C5P/M	<10	PSEL	<1000
VCOM	<5	CPSEL	<1000
VCOMH	<10	EXT_PWR	<1000

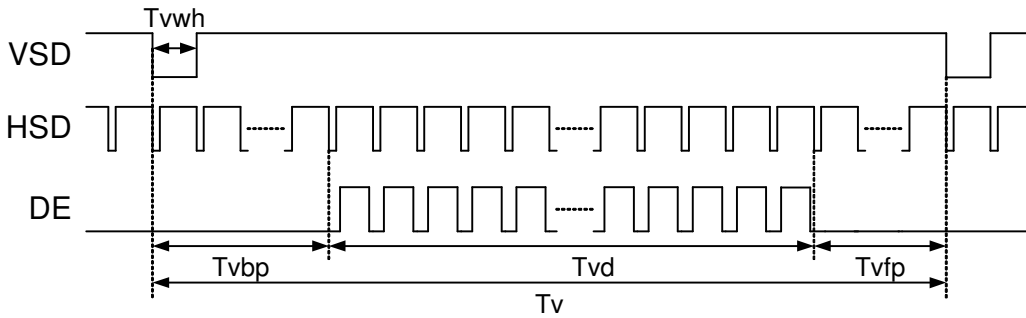
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The connection of charge pump circuit

Suggestion of external component

Component	Value	Voltage proof		
C5	1uF	>10V		
C7, C9	1uF	>16V		
C1, C2, C3, C11, C12, C16	2.2uF	>6V		
C6, C8, C10	2.2uF	>16V		
C4, C13, C14, C15, C17	4.7uF	>10V		
Component	Type	Forward voltage	Voltage proof	Characteristics
D1	Schottky Barrier Diode	<0.3V	>25V	IF > 200mA

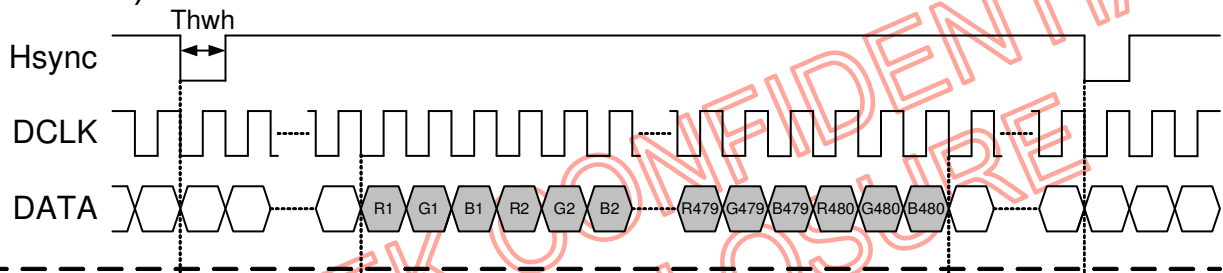
Data Input Format

Vertical input timing

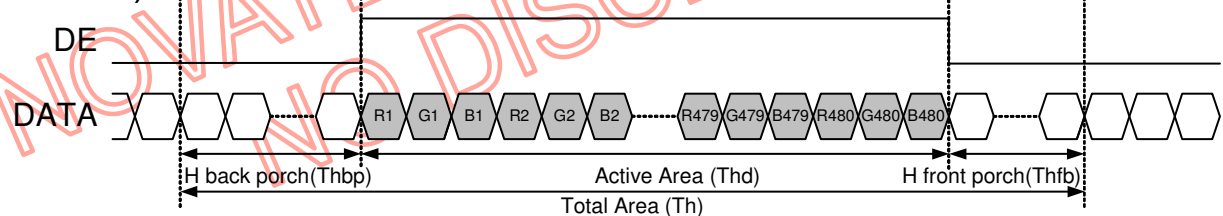


Serial 8-bit RGB Mode Data format

(HV Mode)

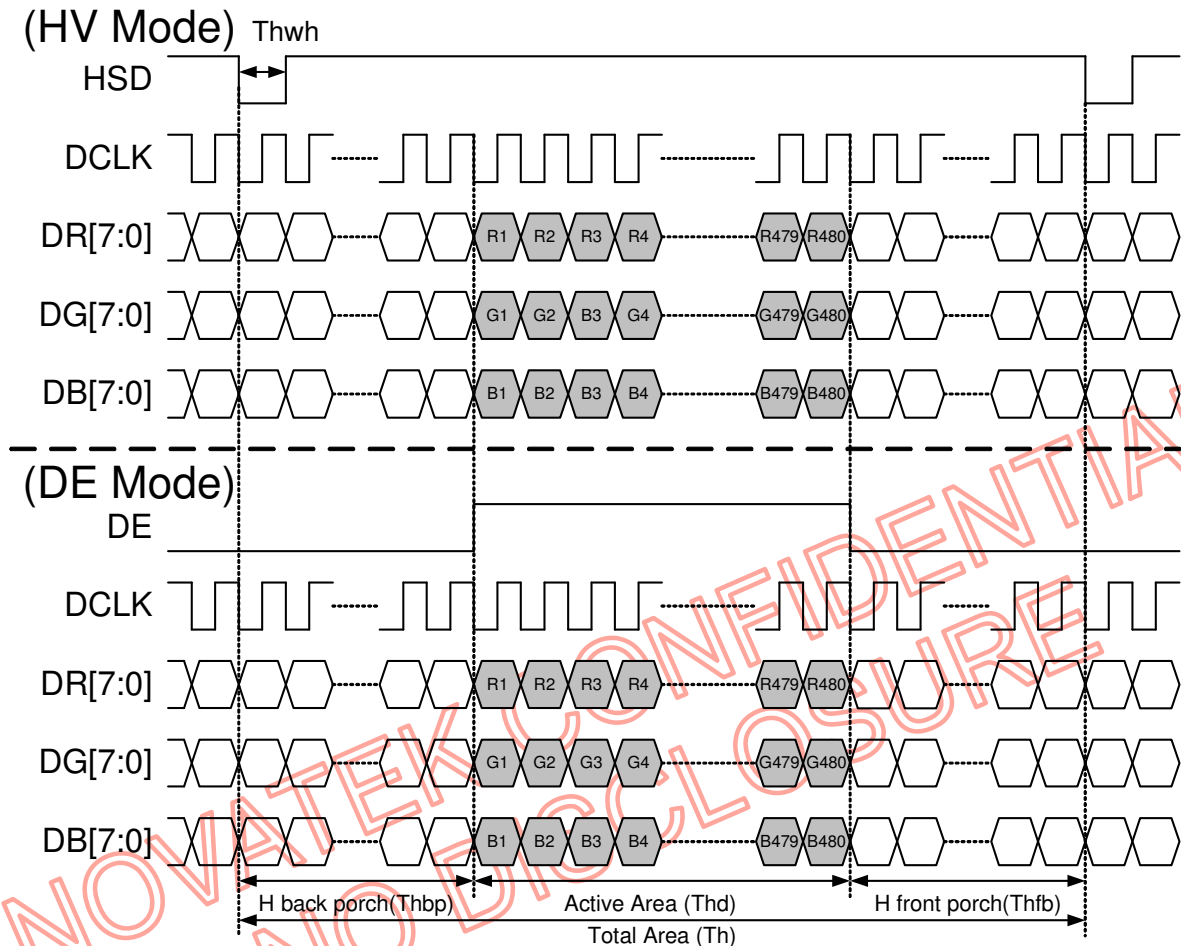


(DE Mode)



Serial 8-bit RGB input timing table

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	24	27	30	MHz
VSD period time	T _v	277	288	400	H
VSD display area	T _{vd}	272			H
VSD back porch	T _{vb}	3	8	31	H
VSD front porch	T _{vfp}	2	8	93	H
HSD period time	T _h	1560	1716	1900	DCLK
HSD display area	T _{hd}	1440			DCLK
HSD back porch	T _{hbp}	108	120	255	DCLK
HSD front porch	T _{hfp}	12	168	205	DCLK

Parallel RGB Mode Data format

Parallel RGB input timing table

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	5	9	12	MHz
VSD period time	Tv	277	288	400	H
VSD display area	Tvd	272			H
VSD back porch	Tvb	3	8	31	H
VSD front porch	Tvfp	2	8	93	H
HSD period time	Th	520	525	800	DCLK
HSD display area	Thd	480			DCLK
HSD back porch	Thbp	36	40	255	DCLK
HSD front porch	Thfp	4	5	65	DCLK

Absolute Maximum Ratings

Logic supply voltage, VDDIO	-0.5 to +5V
Analog supply voltage, AVDD, VGL	-0.3 to +7.0V
VGH~VGL	-16 to 0.3V
Operating Ambient Temperature, TA	-0.3 to 35V
Storage Temperature, TSTR	-20°C to 85°C
	-55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Range (GND=AGND=PGND=0V, TA= -20 to +85 °C)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Supply Voltage	VDD	2.7	3.3	3.6	V	
Charge Pump Supply Voltage	PVDD	3.0	3.3	3.6	V	CPSEL="L"
		2.6	2.7	3.0	V	CPSEL="H"
Digital interface supply Voltage	VDDIO	1.7	-	VDD	V	
Digital Input Voltage	Din	0	-	VDDIO	V	
OTP Supply Voltage	VPP_OTP	5.9	6	6.1	V	
VCOM AC Voltage	VCOMH- VCOML	2.96	-	6.2	V	VCOMAC=VCOMH-VCOML, VCOMH have to greater then PVDD

DC Electrical Characteristics (VDDIO=VDD=3.0 to 3.6V, GND=AGND=PGND=0V, TA= -20 to +85 °C)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Block Circuit						
Low Level Input Voltage	Vil	GND	-	0.3xVDDIO	V	Digital input pins
High Level Input Voltage	Vih	0.7xVDDIO	-	VDDIO	V	Digital input pins
Input Leakage Current	Ii	-	-	±1	uA	Digital input pins
Pull-high/low Impedance	Rin	-	200K	-	ohm	Digital control input pins VDDIO=3.3V, TA=25 °C
High Level Output Voltage	Voh	VDDIO-0.4	-	-	V	Digital output pins; Ioh=400uA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; Iol=-400uA
Digital Stand-by Current	I _{dst}	-	50	100	uA	Output are High-Z, all pins are default.
Digital Operating Current	I _{cc}	-	4	-	mA	DCLK=9MHz, F _{ld} =17.28KHz (@ 24bit RGB mode), no load TA=25 °C
Analog Block Circuit						
Analog Supply Voltage	AVDD	-	5.2	-	V	

Positive power Supply	VGH	11.5	15	15.5	V	By VGH_SEL[2:0] setting
Negative power Supply	VGL	-10.5	-10	-6.5	V	By VGL_SEL[2:0] setting
VCOMH Output Level	VCOMH	2.5	-	5	V	By VCOM_H[7:0] setting
VCOML Output Level	VCOML	-3	-	-0.46	V	By VCOM_L[6:0] setting
Feed back voltage for PWM	VFB	0.25	0.6	0.8	V	DC-DC operating. BY VFBSEL setting
Base drive current for PWM	IDRV	-	20	-	mA	VDD=3.3V
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V ~ 0.5V & AVDD-0.5 ~ AVDD-0.1
		-	±15	±20	mV	Vo=0.5V ~ AVDD-0.5V
Dynamic Range of Ouput	Vdr	0.1	-	AVDD-0.1	V	S1 to S720
Low-level Output Current of VCOM	IOLC	-	-18	-	mA	VCOMH=4V, VCOML=-1V VCOM output=-1V V.S. -0.1V
High-level Output Current of VCOM	IOHC	-	18	-	mA	VCOMH=4V, VCOML=-1V VCOM output=4V V.S. 3.1V
Source Low-level Output Current	IOLS	-	-100	-	uA	S1 to S720; VO=0.1 V.S. 1V
Source High-level Output Current	IOHS	-	100	-	uA	S1 to S720; VO=4.9 V.S. 4.0
Gate Low-level Output Current	IOLG	-	-250	-	uA	G1 to G544; VO=VGL V.S. VGL+0.5
Gate High-level Output Current	IOHG	-	250	-	uA	G1 to G544; VO=VGH V.S. VGH-0.5
Analog Stand-by Current	I _{stb}	-	-	100	uA	STB="L", all function are shutdown
Analog Operating Current	IDD	-	10	-	mA	DCLK=9MHz, F _{id} =17.28KHz (@ 24bit RGB mode), No load CPSEL="L", TA=25 °C
		-	15	-	mA	DCLK=9MHz, F _{id} =17.28KHz (@ 24bit RGB mode), No load CPSEL="H", TA=25 °C

AC Electrical Characteristics
 (VDDIO=VDD=3.0 to 3.6V, GND=0V, TA=-20 to +85 °C)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
system operation timing						
VCC power source slew time	TPOR	-	-	20	ms	From 0V to 99% VCC
GRB pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input Output timing						
DCLK clock time	Tclk	33.3	-	-	ns	DCLK=30MHz
Clock rising time	Trck	9	-	-	ns	
Clock falling time	Tfck	9	-	-	ns	
HSD width	Thwh	1	-	-	DCLK	
HSD period time	Th	55	60	65	us	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
VSD width	Tvwh	1	-	-	Th	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
DE setup time	Tdesu	12	-	-	ns	
DE hold time	Tdehd	12	-	-	ns	
Source output setting time	Tst	-	10	12	us	10% to 90% CL=60pF, RL=2Kohm
Gate output setting time	Tgst	-	500	1000	ns	10% to 90%, CL=60pF
VCOM output setting time	Tcst	-	-	12	us	10% to 90%, CL=40nF, RL=50ohm
Time from VSD to 1 st line data input	Tvs	3	8	31	Th	HV mode By HDL[4:0] setting
3-wire serial communication AC timing						
Serial clock	Tsck	200	-	-	ns	
SCL pulse duty	Tscdut	40	50	60	%	
Serial data setup time	Tisu	50	-	-	ns	
Serial data hold time	Tihd	50	-	-	ns	
Serial clock high/low	Tssw	50	-	-	ns	
CSB distinguish time	Tcd	400	-	-	ns	
CSB to VSD	Tcv	1	-	-	us	
CSB input setup time	Tcsu	50	-	-	ns	
CSB input hold time	Tchd	50	-	-	ns	

Output timing Table

Serial 8-bit RGB Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK frequency	Fclk	24	27	30	MHz	
DCLK cycle time	Tclk	33	37	42	ns	
DCLK pulse duty	Tcwh	40	50	60	%	
Time from HSD to source output	Thso	-	33	-	DCLK	
Time from HSD to gate output	Thgo	-	93	-	DCLK	
Time from HSD to gate output off	Thgz	-	3	-	DCLK	
Time from HSD to VCOM	Thvc	-	33	-	DCLK	

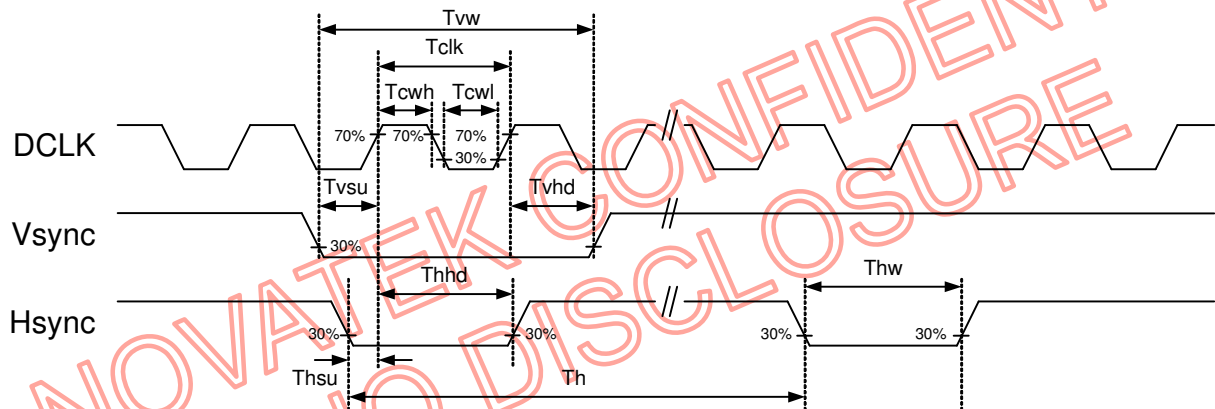
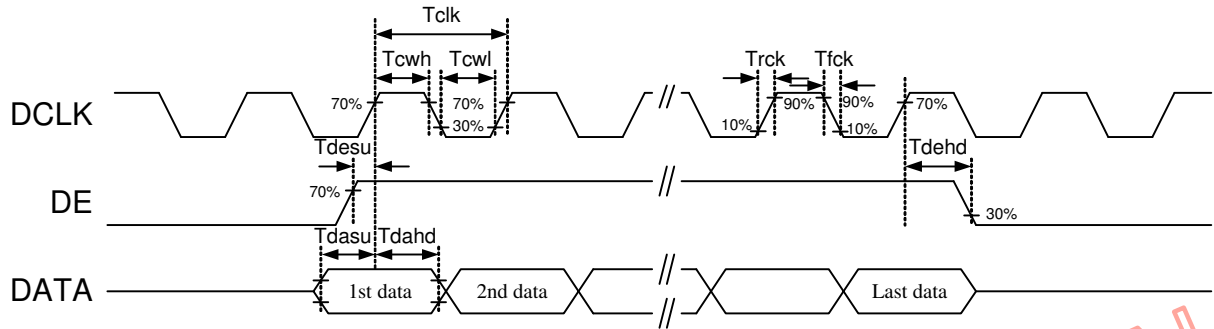
Parallel RGB Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK frequency	Fclk	5	9	12	MHz	
DCLK cycle time	Tclk	83	110	200	ns	
DCLK pulse duty	Tcwh	40	50	60	%	
Time from HSD to source output	Thso	-	13	-	DCLK	
Time from HSD to gate output	Thgo	-	33	-	DCLK	
Time from HSD to gate output off	Thgz	-	3	-	DCLK	
Time from HSD to VCOM	Thvc	-	13	-	DCLK	

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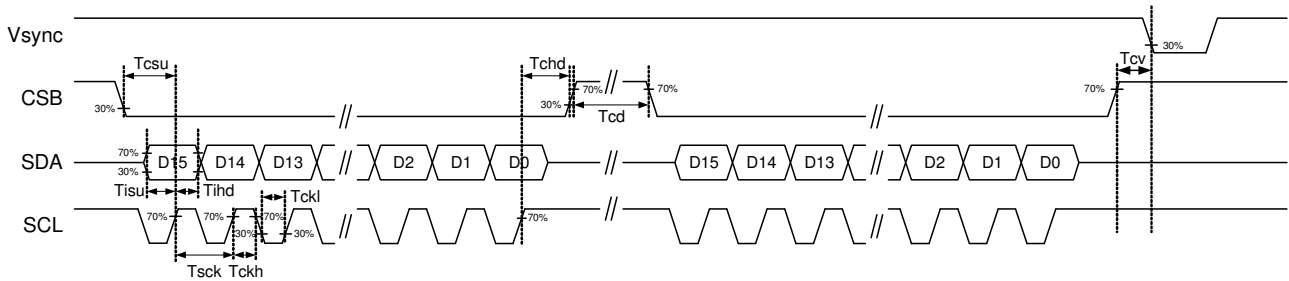
Timing Diagram

Clock and Data Input Timing Diagram

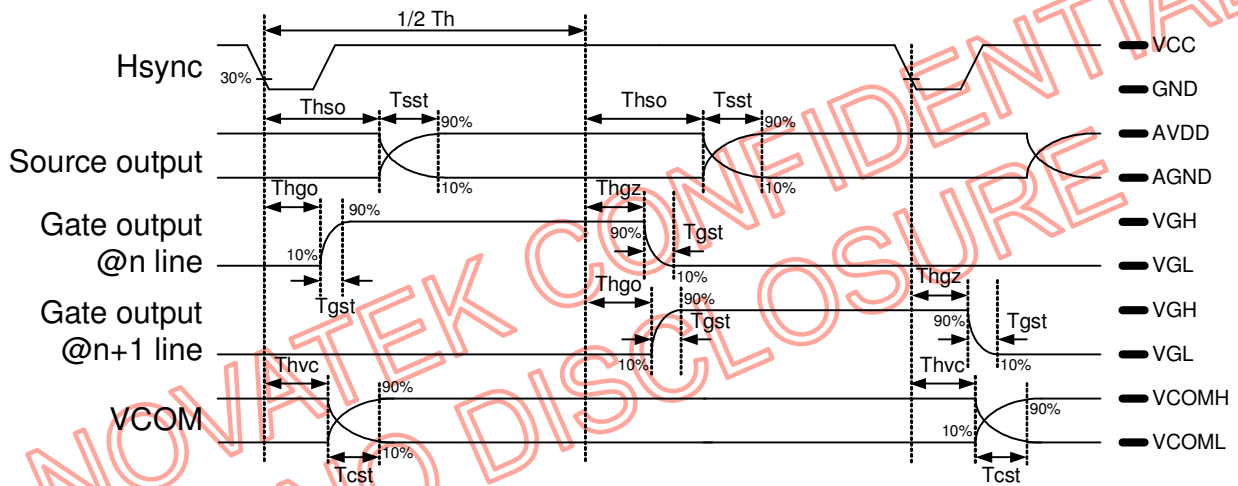


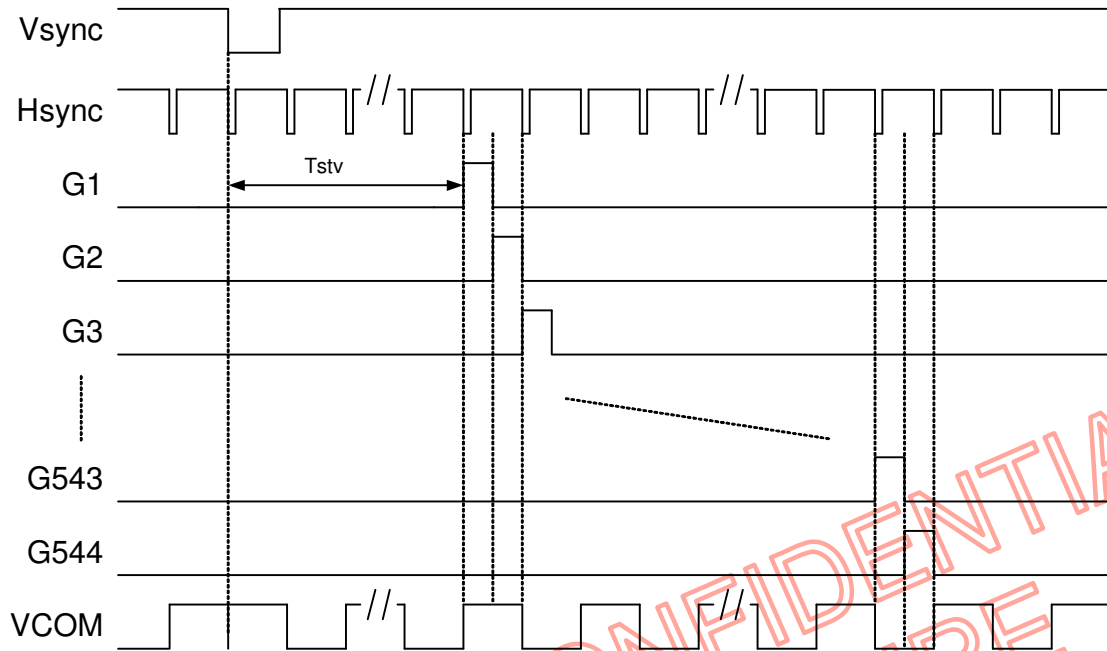
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3-Wire Timing Diagram



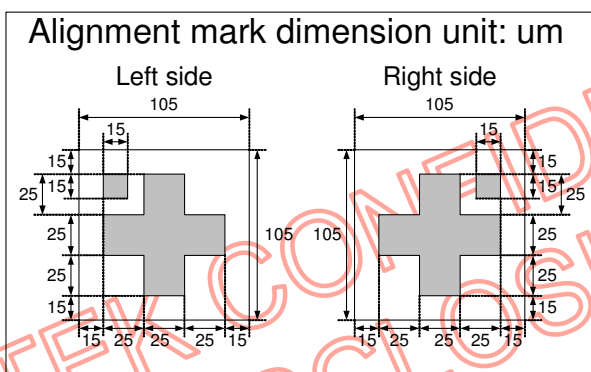
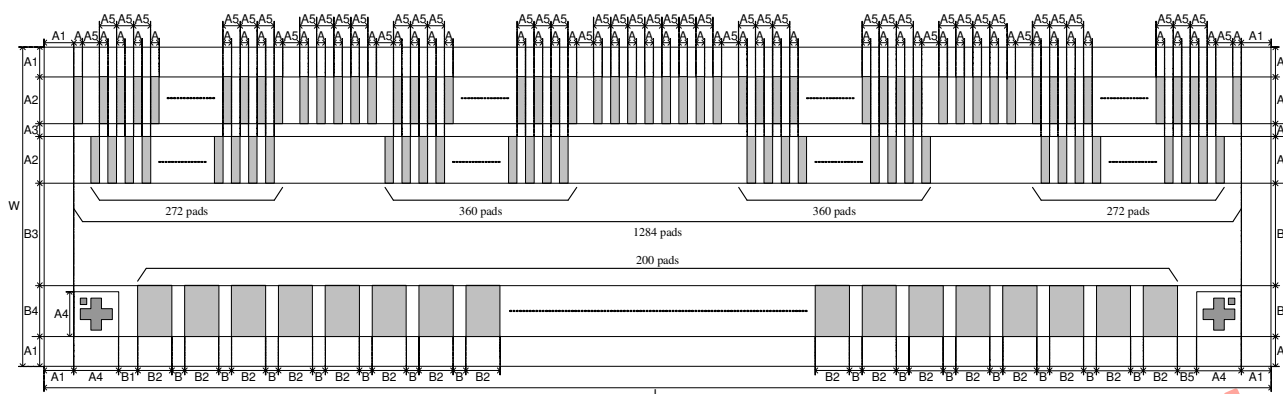
Output timing Diagram



Vertical Timing Diagram


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Chip Outline Dimensions



Symbol	Dimensions (μm)	Symbol	Dimensions (μm)	Symbol	Dimensions (μm)
A	17	B	30	W	750(Max)
A1	59	B1	57	L	22405(Max)
A2	110	B2	80		
A3	30	B3	262		
A4	105	B4	120		
A5	34	B5	50		

*Remark: Chip dimension include scribe line

Pad Coordinate

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
1	DUM1	-10941.5	-256	51	VCC25	-5441.5	-256	101	DG6	58.5	-256
2	SHIELDING1	-10831.5	-256	52	VCC25	-5331.5	-256	102	DG7	168.5	-256
3	TP0	-10721.5	-256	53	VCC25	-5221.5	-256	103	DB0	278.5	-256
4	TP1	-10611.5	-256	54	SHIELDING13	-5111.5	-256	104	DB1	388.5	-256
5	TP2	-10501.5	-256	55	FB	-5001.5	-256	105	DB2	498.5	-256
6	TP3	-10391.5	-256	56	SHIELDING14	-4891.5	-256	106	DB3	608.5	-256
7	TP4	-10281.5	-256	57	DRV	-4781.5	-256	107	DB4	718.5	-256
8	TP5	-10171.5	-256	58	DRV	-4671.5	-256	108	DB5	828.5	-256
9	TP6	-10061.5	-256	59	GND	-4561.5	-256	109	DB6	938.5	-256
10	TP7	-9951.5	-256	60	GND	-4451.5	-256	110	DB7	1048.5	-256
11	TP8	-9841.5	-256	61	GND	-4341.5	-256	111	SHIELDING19	1158.5	-256
12	TP9	-9731.5	-256	62	VCC	-4231.5	-256	112	AVDD	1268.5	-256
13	TP10	-9621.5	-256	63	VCC	-4121.5	-256	113	AVDD	1378.5	-256
14	TM0	-9511.5	-256	64	VCC	-4011.5	-256	114	AVDD	1488.5	-256
15	TM1	-9401.5	-256	65	VDDIO	-3901.5	-256	115	AVDD	1598.5	-256
16	TM2	-9291.5	-256	66	VDDIO	-3791.5	-256	116	AVDD	1708.5	-256
17	TM3	-9181.5	-256	67	VDDIO	-3681.5	-256	117	AVDD	1818.5	-256
18	SHIELDING2	-9071.5	-256	68	VDD	-3571.5	-256	118	AGND	1928.5	-256
19	SHIELDING3	-8961.5	-256	69	VDD	-3461.5	-256	119	AGND	2038.5	-256
20	SHIELDING4	-8851.5	-256	70	VDD	-3351.5	-256	120	AGND	2148.5	-256
21	EXT_PWR	-8741.5	-256	71	VSD	-3241.5	-256	121	AGND	2258.5	-256
22	SHIELDING5	-8631.5	-256	72	HSD	-3131.5	-256	122	AGND	2368.5	-256
23	SHIELDING6	-8521.5	-256	73	DCLK	-3021.5	-256	123	AGND	2478.5	-256
24	SHIELDING7	-8411.5	-256	74	DEN	-2911.5	-256	124	SHIELDING20	2588.5	-256
25	SHIELDING8	-8301.5	-256	75	PSEL	-2801.5	-256	125	VINT3	2698.5	-256
26	SHIELDING9	-8191.5	-256	76	CSB	-2691.5	-256	126	VINT3	2808.5	-256
27	SHIELDING10	-8081.5	-256	77	SDA	-2581.5	-256	127	VINT3	2918.5	-256
28	TB0	-7971.5	-256	78	SCL	-2471.5	-256	128	VINT3	3028.5	-256
29	TB1	-7861.5	-256	79	STB	-2361.5	-256	129	C5M	3138.5	-256
30	TCSW0	-7751.5	-256	80	GRB	-2251.5	-256	130	C5M	3248.5	-256
31	TCSW1	-7641.5	-256	81	HVDSL	-2141.5	-256	131	C5M	3358.5	-256
32	VPP_OTP	-7531.5	-256	82	SHIELDING15	-2031.5	-256	132	C5P	3468.5	-256
33	VPP_OTP	-7421.5	-256	83	SHIELDING16	-1921.5	-256	133	C5P	3578.5	-256
34	VPP_OTP	-7311.5	-256	84	SHIELDING17	-1811.5	-256	134	C5P	3688.5	-256
35	SHIELDING11	-7201.5	-256	85	CPSEL	-1701.5	-256	135	VINT1	3798.5	-256
36	COM1_L	-7091.5	-256	86	SHIELDING18	-1591.5	-256	136	VINT1	3908.5	-256
37	COM1_L	-6981.5	-256	87	DR0	-1481.5	-256	137	VINT1	4018.5	-256
38	SHIELDING12	-6871.5	-256	88	DR1	-1371.5	-256	138	VINT1	4128.5	-256
39	VCOMH	-6761.5	-256	89	DR2	-1261.5	-256	139	VINT1	4238.5	-256
40	VCOMH	-6651.5	-256	90	DR3	-1151.5	-256	140	VINT1	4348.5	-256
41	VCOMH	-6541.5	-256	91	DR4	-1041.5	-256	141	PGND	4458.5	-256
42	VCOML	-6431.5	-256	92	DR5	-931.5	-256	142	PGND	4568.5	-256
43	VCOML	-6321.5	-256	93	DR6	-821.5	-256	143	PGND	4678.5	-256
44	VCOML	-6211.5	-256	94	DR7	-711.5	-256	144	PGND	4788.5	-256
45	VCOM	-6101.5	-256	95	DG0	-601.5	-256	145	PGND	4898.5	-256
46	VCOM	-5991.5	-256	96	DG1	-491.5	-256	146	PGND	5008.5	-256
47	VCOM	-5881.5	-256	97	DG2	-381.5	-256	147	PGND	5118.5	-256
48	VCOM	-5771.5	-256	98	DG3	-271.5	-256	148	PGND	5228.5	-256
49	VCOM	-5661.5	-256	99	DG4	-161.5	-256	149	COM2_L	5338.5	-256
50	VCOM	-5551.5	-256	100	DG5	-51.5	-256	150	COM2_L	5448.5	-256

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
151	C1AP	5558.5	-256	201	DUM3	11135	261	251	G100	10268	261
152	C1AP	5668.5	-256	202	G2	11101	121	252	G102	10251	121
153	C1AP	5778.5	-256	203	G4	11084	261	253	G104	10234	261
154	C1AM	5888.5	-256	204	G6	11067	121	254	G106	10217	121
155	C1AM	5998.5	-256	205	G8	11050	261	255	G108	10200	261
156	C1AM	6108.5	-256	206	G10	11033	121	256	G110	10183	121
157	C1BP	6218.5	-256	207	G12	11016	261	257	G112	10166	261
158	C1BP	6328.5	-256	208	G14	10999	121	258	G114	10149	121
159	C1BP	6438.5	-256	209	G16	10982	261	259	G116	10132	261
160	C1BM	6548.5	-256	210	G18	10965	121	260	G118	10115	121
161	C1BM	6658.5	-256	211	G20	10948	261	261	G120	10098	261
162	C1BM	6768.5	-256	212	G22	10931	121	262	G122	10081	121
163	C1CP	6878.5	-256	213	G24	10914	261	263	G124	10064	261
164	C1CP	6988.5	-256	214	G26	10897	121	264	G126	10047	121
165	C1CP	7098.5	-256	215	G28	10880	261	265	G128	10030	261
166	C1CM	7208.5	-256	216	G30	10863	121	266	G130	10013	121
167	C1CM	7318.5	-256	217	G32	10846	261	267	G132	9996	261
168	C1CM	7428.5	-256	218	G34	10829	121	268	G134	9979	121
169	PVDD	7538.5	-256	219	G36	10812	261	269	G136	9962	261
170	PVDD	7648.5	-256	220	G38	10795	121	270	G138	9945	121
171	PVDD	7758.5	-256	221	G40	10778	261	271	G140	9928	261
172	PVDD	7868.5	-256	222	G42	10761	121	272	G142	9911	121
173	PVDD	7978.5	-256	223	G44	10744	261	273	G144	9894	261
174	PVDD	8088.5	-256	224	G46	10727	121	274	G146	9877	121
175	PVDD	8198.5	-256	225	G48	10710	261	275	G148	9860	261
176	PVDD	8308.5	-256	226	G50	10693	121	276	G150	9843	121
177	C2P	8418.5	-256	227	G52	10676	261	277	G152	9826	261
178	C2P	8528.5	-256	228	G54	10659	121	278	G154	9809	121
179	C2M	8638.5	-256	229	G56	10642	261	279	G156	9792	261
180	C2M	8748.5	-256	230	G58	10625	121	280	G158	9775	121
181	VINT2	8858.5	-256	231	G60	10608	261	281	G160	9758	261
182	VINT2	8968.5	-256	232	G62	10591	121	282	G162	9741	121
183	VINT2	9078.5	-256	233	G64	10574	261	283	G164	9724	261
184	SHIELDING21	9188.5	-256	234	G66	10557	121	284	G166	9707	121
185	C3P	9298.5	-256	235	G68	10540	261	285	G168	9690	261
186	C3P	9408.5	-256	236	G70	10523	121	286	G170	9673	121
187	C3M	9518.5	-256	237	G72	10506	261	287	G172	9656	261
188	C3M	9628.5	-256	238	G74	10489	121	288	G174	9639	121
189	VGH	9738.5	-256	239	G76	10472	261	289	G176	9622	261
190	VGH	9848.5	-256	240	G78	10455	121	290	G178	9605	121
191	VGH	9958.5	-256	241	G80	10438	261	291	G180	9588	261
192	C4P	10068.5	-256	242	G82	10421	121	292	G182	9571	121
193	C4P	10178.5	-256	243	G84	10404	261	293	G184	9554	261
194	C4M	10288.5	-256	244	G86	10387	121	294	G186	9537	121
195	C4M	10398.5	-256	245	G88	10370	261	295	G188	9520	261
196	VGL	10508.5	-256	246	G90	10353	121	296	G190	9503	121
197	VGL	10618.5	-256	247	G92	10336	261	297	G192	9486	261
198	VGL	10728.5	-256	248	G94	10319	121	298	G194	9469	121
199	SHIELDING22	10838.5	-256	249	G96	10302	261	299	G196	9452	261
200	DUM2	10948.5	-256	250	G98	10285	121	300	G198	9435	121

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
301	G200	9418	261	351	G300	8568	261	401	G400	7718	261
302	G202	9401	121	352	G302	8551	121	402	G402	7701	121
303	G204	9384	261	353	G304	8534	261	403	G404	7684	261
304	G206	9367	121	354	G306	8517	121	404	G406	7667	121
305	G208	9350	261	355	G308	8500	261	405	G408	7650	261
306	G210	9333	121	356	G310	8483	121	406	G410	7633	121
307	G212	9316	261	357	G312	8466	261	407	G412	7616	261
308	G214	9299	121	358	G314	8449	121	408	G414	7599	121
309	G216	9282	261	359	G316	8432	261	409	G416	7582	261
310	G218	9265	121	360	G318	8415	121	410	G418	7565	121
311	G220	9248	261	361	G320	8398	261	411	G420	7548	261
312	G222	9231	121	362	G322	8381	121	412	G422	7531	121
313	G224	9214	261	363	G324	8364	261	413	G424	7514	261
314	G226	9197	121	364	G326	8347	121	414	G426	7497	121
315	G228	9180	261	365	G328	8330	261	415	G428	7480	261
316	G230	9163	121	366	G330	8313	121	416	G430	7463	121
317	G232	9146	261	367	G332	8296	261	417	G432	7446	261
318	G234	9129	121	368	G334	8279	121	418	G434	7429	121
319	G236	9112	261	369	G336	8262	261	419	G436	7412	261
320	G238	9095	121	370	G338	8245	121	420	G438	7395	121
321	G240	9078	261	371	G340	8228	261	421	G440	7378	261
322	G242	9061	121	372	G342	8211	121	422	G442	7361	121
323	G244	9044	261	373	G344	8194	261	423	G444	7344	261
324	G246	9027	121	374	G346	8177	121	424	G446	7327	121
325	G248	9010	261	375	G348	8160	261	425	G448	7310	261
326	G250	8993	121	376	G350	8143	121	426	G450	7293	121
327	G252	8976	261	377	G352	8126	261	427	G452	7276	261
328	G254	8959	121	378	G354	8109	121	428	G454	7259	121
329	G256	8942	261	379	G356	8092	261	429	G456	7242	261
330	G258	8925	121	380	G358	8075	121	430	G458	7225	121
331	G260	8908	261	381	G360	8058	261	431	G460	7208	261
332	G262	8891	121	382	G362	8041	121	432	G462	7191	121
333	G264	8874	261	383	G364	8024	261	433	G464	7174	261
334	G266	8857	121	384	G366	8007	121	434	G466	7157	121
335	G268	8840	261	385	G368	7990	261	435	G468	7140	261
336	G270	8823	121	386	G370	7973	121	436	G470	7123	121
337	G272	8806	261	387	G372	7956	261	437	G472	7106	261
338	G274	8789	121	388	G374	7939	121	438	G474	7089	121
339	G276	8772	261	389	G376	7922	261	439	G476	7072	261
340	G278	8755	121	390	G378	7905	121	440	G478	7055	121
341	G280	8738	261	391	G380	7888	261	441	G480	7038	261
342	G282	8721	121	392	G382	7871	121	442	G482	7021	121
343	G284	8704	261	393	G384	7854	261	443	G484	7004	261
344	G286	8687	121	394	G386	7837	121	444	G486	6987	121
345	G288	8670	261	395	G388	7820	261	445	G488	6970	261
346	G290	8653	121	396	G390	7803	121	446	G490	6953	121
347	G292	8636	261	397	G392	7786	261	447	G492	6936	261
348	G294	8619	121	398	G394	7769	121	448	G494	6919	121
349	G296	8602	261	399	G396	7752	261	449	G496	6902	261
350	G298	8585	121	400	G398	7735	121	450	G498	6885	121

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
451	G500	6868	261	501	S23	5899	121	551	S73	5049	121
452	G502	6851	121	502	S24	5882	261	552	S74	5032	261
453	G504	6834	261	503	S25	5865	121	553	S75	5015	121
454	G506	6817	121	504	S26	5848	261	554	S76	4998	261
455	G508	6800	261	505	S27	5831	121	555	S77	4981	121
456	G510	6783	121	506	S28	5814	261	556	S78	4964	261
457	G512	6766	261	507	S29	5797	121	557	S79	4947	121
458	G514	6749	121	508	S30	5780	261	558	S80	4930	261
459	G516	6732	261	509	S31	5763	121	559	S81	4913	121
460	G518	6715	121	510	S32	5746	261	560	S82	4896	261
461	G520	6698	261	511	S33	5729	121	561	S83	4879	121
462	G522	6681	121	512	S34	5712	261	562	S84	4862	261
463	G524	6664	261	513	S35	5695	121	563	S85	4845	121
464	G526	6647	121	514	S36	5678	261	564	S86	4828	261
465	G528	6630	261	515	S37	5661	121	565	S87	4811	121
466	G530	6613	121	516	S38	5644	261	566	S88	4794	261
467	G532	6596	261	517	S39	5627	121	567	S89	4777	121
468	G534	6579	121	518	S40	5610	261	568	S90	4760	261
469	G536	6562	261	519	S41	5593	121	569	S91	4743	121
470	G538	6545	121	520	S42	5576	261	570	S92	4726	261
471	G540	6528	261	521	S43	5559	121	571	S93	4709	121
472	G542	6511	121	522	S44	5542	261	572	S94	4692	261
473	G544	6494	261	523	S45	5525	121	573	S95	4675	121
474	COM2_R	6443	261	524	S46	5508	261	574	S96	4658	261
475	COM2_R	6409	261	525	S47	5491	121	575	S97	4641	121
476	COM2_R	6375	261	526	S48	5474	261	576	S98	4624	261
477	COM2_R	6341	261	527	S49	5457	121	577	S99	4607	121
478	COM2_R	6307	261	528	S50	5440	261	578	S100	4590	261
479	S1	6273	121	529	S51	5423	121	579	S101	4573	121
480	S2	6256	261	530	S52	5406	261	580	S102	4556	261
481	S3	6239	121	531	S53	5389	121	581	S103	4539	121
482	S4	6222	261	532	S54	5372	261	582	S104	4522	261
483	S5	6205	121	533	S55	5355	121	583	S105	4505	121
484	S6	6188	261	534	S56	5338	261	584	S106	4488	261
485	S7	6171	121	535	S57	5321	121	585	S107	4471	121
486	S8	6154	261	536	S58	5304	261	586	S108	4454	261
487	S9	6137	121	537	S59	5287	121	587	S109	4437	121
488	S10	6120	261	538	S60	5270	261	588	S110	4420	261
489	S11	6103	121	539	S61	5253	121	589	S111	4403	121
490	S12	6086	261	540	S62	5236	261	590	S112	4386	261
491	S13	6069	121	541	S63	5219	121	591	S113	4369	121
492	S14	6052	261	542	S64	5202	261	592	S114	4352	261
493	S15	6035	121	543	S65	5185	121	593	S115	4335	121
494	S16	6018	261	544	S66	5168	261	594	S116	4318	261
495	S17	6001	121	545	S67	5151	121	595	S117	4301	121
496	S18	5984	261	546	S68	5134	261	596	S118	4284	261
497	S19	5967	121	547	S69	5117	121	597	S119	4267	121
498	S20	5950	261	548	S70	5100	261	598	S120	4250	261
499	S21	5933	121	549	S71	5083	121	599	S121	4233	121
500	S22	5916	261	550	S72	5066	261	600	S122	4216	261

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
601	S123	4199	121	651	S173	3349	121	701	S223	2499	121
602	S124	4182	261	652	S174	3332	261	702	S224	2482	261
603	S125	4165	121	653	S175	3315	121	703	S225	2465	121
604	S126	4148	261	654	S176	3298	261	704	S226	2448	261
605	S127	4131	121	655	S177	3281	121	705	S227	2431	121
606	S128	4114	261	656	S178	3264	261	706	S228	2414	261
607	S129	4097	121	657	S179	3247	121	707	S229	2397	121
608	S130	4080	261	658	S180	3230	261	708	S230	2380	261
609	S131	4063	121	659	S181	3213	121	709	S231	2363	121
610	S132	4046	261	660	S182	3196	261	710	S232	2346	261
611	S133	4029	121	661	S183	3179	121	711	S233	2329	121
612	S134	4012	261	662	S184	3162	261	712	S234	2312	261
613	S135	3995	121	663	S185	3145	121	713	S235	2295	121
614	S136	3978	261	664	S186	3128	261	714	S236	2278	261
615	S137	3961	121	665	S187	3111	121	715	S237	2261	121
616	S138	3944	261	666	S188	3094	261	716	S238	2244	261
617	S139	3927	121	667	S189	3077	121	717	S239	2227	121
618	S140	3910	261	668	S190	3060	261	718	S240	2210	261
619	S141	3893	121	669	S191	3043	121	719	S241	2193	121
620	S142	3876	261	670	S192	3026	261	720	S242	2176	261
621	S143	3859	121	671	S193	3009	121	721	S243	2159	121
622	S144	3842	261	672	S194	2992	261	722	S244	2142	261
623	S145	3825	121	673	S195	2975	121	723	S245	2125	121
624	S146	3808	261	674	S196	2958	261	724	S246	2108	261
625	S147	3791	121	675	S197	2941	121	725	S247	2091	121
626	S148	3774	261	676	S198	2924	261	726	S248	2074	261
627	S149	3757	121	677	S199	2907	121	727	S249	2057	121
628	S150	3740	261	678	S200	2890	261	728	S250	2040	261
629	S151	3723	121	679	S201	2873	121	729	S251	2023	121
630	S152	3706	261	680	S202	2856	261	730	S252	2006	261
631	S153	3689	121	681	S203	2839	121	731	S253	1989	121
632	S154	3672	261	682	S204	2822	261	732	S254	1972	261
633	S155	3655	121	683	S205	2805	121	733	S255	1955	121
634	S156	3638	261	684	S206	2788	261	734	S256	1938	261
635	S157	3621	121	685	S207	2771	121	735	S257	1921	121
636	S158	3604	261	686	S208	2754	261	736	S258	1904	261
637	S159	3587	121	687	S209	2737	121	737	S259	1887	121
638	S160	3570	261	688	S210	2720	261	738	S260	1870	261
639	S161	3553	121	689	S211	2703	121	739	S261	1853	121
640	S162	3536	261	690	S212	2686	261	740	S262	1836	261
641	S163	3519	121	691	S213	2669	121	741	S263	1819	121
642	S164	3502	261	692	S214	2652	261	742	S264	1802	261
643	S165	3485	121	693	S215	2635	121	743	S265	1785	121
644	S166	3468	261	694	S216	2618	261	744	S266	1768	261
645	S167	3451	121	695	S217	2601	121	745	S267	1751	121
646	S168	3434	261	696	S218	2584	261	746	S268	1734	261
647	S169	3417	121	697	S219	2567	121	747	S269	1717	121
648	S170	3400	261	698	S220	2550	261	748	S270	1700	261
649	S171	3383	121	699	S221	2533	121	749	S271	1683	121
650	S172	3366	261	700	S222	2516	261	750	S272	1666	261

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
751	S273	1649	121	801	S323	799	121	851	S365	-238	261
752	S274	1632	261	802	S324	782	261	852	S366	-255	121
753	S275	1615	121	803	S325	765	121	853	S367	-272	261
754	S276	1598	261	804	S326	748	261	854	S368	-289	121
755	S277	1581	121	805	S327	731	121	855	S369	-306	261
756	S278	1564	261	806	S328	714	261	856	S370	-323	121
757	S279	1547	121	807	S329	697	121	857	S371	-340	261
758	S280	1530	261	808	S330	680	261	858	S372	-357	121
759	S281	1513	121	809	S331	663	121	859	S373	-374	261
760	S282	1496	261	810	S332	646	261	860	S374	-391	121
761	S283	1479	121	811	S333	629	121	861	S375	-408	261
762	S284	1462	261	812	S334	612	261	862	S376	-425	121
763	S285	1445	121	813	S335	595	121	863	S377	-442	261
764	S286	1428	261	814	S336	578	261	864	S378	-459	121
765	S287	1411	121	815	S337	561	121	865	S379	-476	261
766	S288	1394	261	816	S338	544	261	866	S380	-493	121
767	S289	1377	121	817	S339	527	121	867	S381	-510	261
768	S290	1360	261	818	S340	510	261	868	S382	-527	121
769	S291	1343	121	819	S341	493	121	869	S383	-544	261
770	S292	1326	261	820	S342	476	261	870	S384	-561	121
771	S293	1309	121	821	S343	459	121	871	S385	-578	261
772	S294	1292	261	822	S344	442	261	872	S386	-595	121
773	S295	1275	121	823	S345	425	121	873	S387	-612	261
774	S296	1258	261	824	S346	408	261	874	S388	-629	121
775	S297	1241	121	825	S347	391	121	875	S389	-646	261
776	S298	1224	261	826	S348	374	261	876	S390	-663	121
777	S299	1207	121	827	S349	357	121	877	S391	-680	261
778	S300	1190	261	828	S350	340	261	878	S392	-697	121
779	S301	1173	121	829	S351	323	121	879	S393	-714	261
780	S302	1156	261	830	S352	306	261	880	S394	-731	121
781	S303	1139	121	831	S353	289	121	881	S395	-748	261
782	S304	1122	261	832	S354	272	261	882	S396	-765	121
783	S305	1105	121	833	S355	255	121	883	S397	-782	261
784	S306	1088	261	834	S356	238	261	884	S398	-799	121
785	S307	1071	121	835	S357	221	121	885	S399	-816	261
786	S308	1054	261	836	S358	204	261	886	S400	-833	121
787	S309	1037	121	837	S359	187	121	887	S401	-850	261
788	S310	1020	261	838	S360	170	261	888	S402	-867	121
789	S311	1003	121	839	SHIELDING23	119	261	889	S403	-884	261
790	S312	986	261	840	SHIELDING24	85	261	890	S404	-901	121
791	S313	969	121	841	SHIELDING25	51	261	891	S405	-918	261
792	S314	952	261	842	SHIELDING26	17	261	892	S406	-935	121
793	S315	935	121	843	SHIELDING27	-17	261	893	S407	-952	261
794	S316	918	261	844	SHIELDING28	-51	261	894	S408	-969	121
795	S317	901	121	845	SHIELDING29	-85	261	895	S409	-986	261
796	S318	884	261	846	SHIELDING30	-119	261	896	S410	-1003	121
797	S319	867	121	847	S361	-170	261	897	S411	-1020	261
798	S320	850	261	848	S362	-187	121	898	S412	-1037	121
799	S321	833	121	849	S363	-204	261	899	S413	-1054	261
800	S322	816	261	850	S364	-221	121	900	S414	-1071	121

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
901	S415	-1088	261	951	S465	-1938	261	1001	S515	-2788	261
902	S416	-1105	121	952	S466	-1955	121	1002	S516	-2805	121
903	S417	-1122	261	953	S467	-1972	261	1003	S517	-2822	261
904	S418	-1139	121	954	S468	-1989	121	1004	S518	-2839	121
905	S419	-1156	261	955	S469	-2006	261	1005	S519	-2856	261
906	S420	-1173	121	956	S470	-2023	121	1006	S520	-2873	121
907	S421	-1190	261	957	S471	-2040	261	1007	S521	-2890	261
908	S422	-1207	121	958	S472	-2057	121	1008	S522	-2907	121
909	S423	-1224	261	959	S473	-2074	261	1009	S523	-2924	261
910	S424	-1241	121	960	S474	-2091	121	1010	S524	-2941	121
911	S425	-1258	261	961	S475	-2108	261	1011	S525	-2958	261
912	S426	-1275	121	962	S476	-2125	121	1012	S526	-2975	121
913	S427	-1292	261	963	S477	-2142	261	1013	S527	-2992	261
914	S428	-1309	121	964	S478	-2159	121	1014	S528	-3009	121
915	S429	-1326	261	965	S479	-2176	261	1015	S529	-3026	261
916	S430	-1343	121	966	S480	-2193	121	1016	S530	-3043	121
917	S431	-1360	261	967	S481	-2210	261	1017	S531	-3060	261
918	S432	-1377	121	968	S482	-2227	121	1018	S532	-3077	121
919	S433	-1394	261	969	S483	-2244	261	1019	S533	-3094	261
920	S434	-1411	121	970	S484	-2261	121	1020	S534	-3111	121
921	S435	-1428	261	971	S485	-2278	261	1021	S535	-3128	261
922	S436	-1445	121	972	S486	-2295	121	1022	S536	-3145	121
923	S437	-1462	261	973	S487	-2312	261	1023	S537	-3162	261
924	S438	-1479	121	974	S488	-2329	121	1024	S538	-3179	121
925	S439	-1496	261	975	S489	-2346	261	1025	S539	-3196	261
926	S440	-1513	121	976	S490	-2363	121	1026	S540	-3213	121
927	S441	-1530	261	977	S491	-2380	261	1027	S541	-3230	261
928	S442	-1547	121	978	S492	-2397	121	1028	S542	-3247	121
929	S443	-1564	261	979	S493	-2414	261	1029	S543	-3264	261
930	S444	-1581	121	980	S494	-2431	121	1030	S544	-3281	121
931	S445	-1598	261	981	S495	-2448	261	1031	S545	-3298	261
932	S446	-1615	121	982	S496	-2465	121	1032	S546	-3315	121
933	S447	-1632	261	983	S497	-2482	261	1033	S547	-3332	261
934	S448	-1649	121	984	S498	-2499	121	1034	S548	-3349	121
935	S449	-1666	261	985	S499	-2516	261	1035	S549	-3366	261
936	S450	-1683	121	986	S500	-2533	121	1036	S550	-3383	121
937	S451	-1700	261	987	S501	-2550	261	1037	S551	-3400	261
938	S452	-1717	121	988	S502	-2567	121	1038	S552	-3417	121
939	S453	-1734	261	989	S503	-2584	261	1039	S553	-3434	261
940	S454	-1751	121	990	S504	-2601	121	1040	S554	-3451	121
941	S455	-1768	261	991	S505	-2618	261	1041	S555	-3468	261
942	S456	-1785	121	992	S506	-2635	121	1042	S556	-3485	121
943	S457	-1802	261	993	S507	-2652	261	1043	S557	-3502	261
944	S458	-1819	121	994	S508	-2669	121	1044	S558	-3519	121
945	S459	-1836	261	995	S509	-2686	261	1045	S559	-3536	261
946	S460	-1853	121	996	S510	-2703	121	1046	S560	-3553	121
947	S461	-1870	261	997	S511	-2720	261	1047	S561	-3570	261
948	S462	-1887	121	998	S512	-2737	121	1048	S562	-3587	121
949	S463	-1904	261	999	S513	-2754	261	1049	S563	-3604	261
950	S464	-1921	121	1000	S514	-2771	121	1050	S564	-3621	121

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
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1052	S566	-3655	121	1102	S616	-4505	121	1152	S666	-5355	121
1053	S567	-3672	261	1103	S617	-4522	261	1153	S667	-5372	261
1054	S568	-3689	121	1104	S618	-4539	121	1154	S668	-5389	121
1055	S569	-3706	261	1105	S619	-4556	261	1155	S669	-5406	261
1056	S570	-3723	121	1106	S620	-4573	121	1156	S670	-5423	121
1057	S571	-3740	261	1107	S621	-4590	261	1157	S671	-5440	261
1058	S572	-3757	121	1108	S622	-4607	121	1158	S672	-5457	121
1059	S573	-3774	261	1109	S623	-4624	261	1159	S673	-5474	261
1060	S574	-3791	121	1110	S624	-4641	121	1160	S674	-5491	121
1061	S575	-3808	261	1111	S625	-4658	261	1161	S675	-5508	261
1062	S576	-3825	121	1112	S626	-4675	121	1162	S676	-5525	121
1063	S577	-3842	261	1113	S627	-4692	261	1163	S677	-5542	261
1064	S578	-3859	121	1114	S628	-4709	121	1164	S678	-5559	121
1065	S579	-3876	261	1115	S629	-4726	261	1165	S679	-5576	261
1066	S580	-3893	121	1116	S630	-4743	121	1166	S680	-5593	121
1067	S581	-3910	261	1117	S631	-4760	261	1167	S681	-5610	261
1068	S582	-3927	121	1118	S632	-4777	121	1168	S682	-5627	121
1069	S583	-3944	261	1119	S633	-4794	261	1169	S683	-5644	261
1070	S584	-3961	121	1120	S634	-4811	121	1170	S684	-5661	121
1071	S585	-3978	261	1121	S635	-4828	261	1171	S685	-5678	261
1072	S586	-3995	121	1122	S636	-4845	121	1172	S686	-5695	121
1073	S587	-4012	261	1123	S637	-4862	261	1173	S687	-5712	261
1074	S588	-4029	121	1124	S638	-4879	121	1174	S688	-5729	121
1075	S589	-4046	261	1125	S639	-4896	261	1175	S689	-5746	261
1076	S590	-4063	121	1126	S640	-4913	121	1176	S690	-5763	121
1077	S591	-4080	261	1127	S641	-4930	261	1177	S691	-5780	261
1078	S592	-4097	121	1128	S642	-4947	121	1178	S692	-5797	121
1079	S593	-4114	261	1129	S643	-4964	261	1179	S693	-5814	261
1080	S594	-4131	121	1130	S644	-4981	121	1180	S694	-5831	121
1081	S595	-4148	261	1131	S645	-4998	261	1181	S695	-5848	261
1082	S596	-4165	121	1132	S646	-5015	121	1182	S696	-5865	121
1083	S597	-4182	261	1133	S647	-5032	261	1183	S697	-5882	261
1084	S598	-4199	121	1134	S648	-5049	121	1184	S698	-5899	121
1085	S599	-4216	261	1135	S649	-5066	261	1185	S699	-5916	261
1086	S600	-4233	121	1136	S650	-5083	121	1186	S700	-5933	121
1087	S601	-4250	261	1137	S651	-5100	261	1187	S701	-5950	261
1088	S602	-4267	121	1138	S652	-5117	121	1188	S702	-5967	121
1089	S603	-4284	261	1139	S653	-5134	261	1189	S703	-5984	261
1090	S604	-4301	121	1140	S654	-5151	121	1190	S704	-6001	121
1091	S605	-4318	261	1141	S655	-5168	261	1191	S705	-6018	261
1092	S606	-4335	121	1142	S656	-5185	121	1192	S706	-6035	121
1093	S607	-4352	261	1143	S657	-5202	261	1193	S707	-6052	261
1094	S608	-4369	121	1144	S658	-5219	121	1194	S708	-6069	121
1095	S609	-4386	261	1145	S659	-5236	261	1195	S709	-6086	261
1096	S610	-4403	121	1146	S660	-5253	121	1196	S710	-6103	121
1097	S611	-4420	261	1147	S661	-5270	261	1197	S711	-6120	261
1098	S612	-4437	121	1148	S662	-5287	121	1198	S712	-6137	121
1099	S613	-4454	261	1149	S663	-5304	261	1199	S713	-6154	261
1100	S614	-4471	121	1150	S664	-5321	121	1200	S714	-6171	121

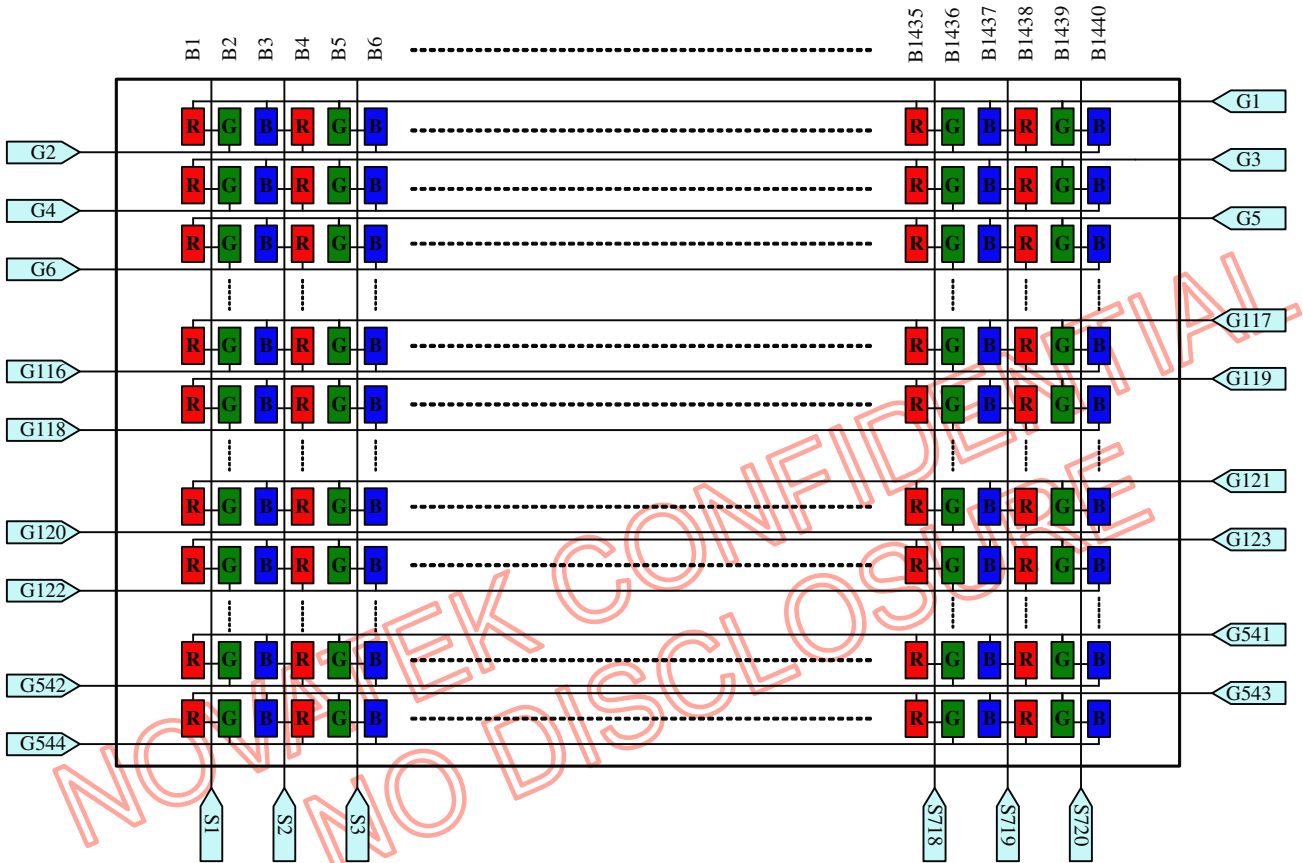
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1202	S716	-6205	121	1252	G463	-7174	261	1302	G363	-8024	261
1203	S717	-6222	261	1253	G461	-7191	121	1303	G361	-8041	121
1204	S718	-6239	121	1254	G459	-7208	261	1304	G359	-8058	261
1205	S719	-6256	261	1255	G457	-7225	121	1305	G357	-8075	121
1206	S720	-6273	121	1256	G455	-7242	261	1306	G355	-8092	261
1207	COM1_R	-6307	261	1257	G453	-7259	121	1307	G353	-8109	121
1208	COM1_R	-6341	261	1258	G451	-7276	261	1308	G351	-8126	261
1209	COM1_R	-6375	261	1259	G449	-7293	121	1309	G349	-8143	121
1210	COM1_R	-6409	261	1260	G447	-7310	261	1310	G347	-8160	261
1211	COM1_R	-6443	261	1261	G445	-7327	121	1311	G345	-8177	121
1212	G543	-6494	261	1262	G443	-7344	261	1312	G343	-8194	261
1213	G541	-6511	121	1263	G441	-7361	121	1313	G341	-8211	121
1214	G539	-6528	261	1264	G439	-7378	261	1314	G339	-8228	261
1215	G537	-6545	121	1265	G437	-7395	121	1315	G337	-8245	121
1216	G535	-6562	261	1266	G435	-7412	261	1316	G335	-8262	261
1217	G533	-6579	121	1267	G433	-7429	121	1317	G333	-8279	121
1218	G531	-6596	261	1268	G431	-7446	261	1318	G331	-8296	261
1219	G529	-6613	121	1269	G429	-7463	121	1319	G329	-8313	121
1220	G527	-6630	261	1270	G427	-7480	261	1320	G327	-8330	261
1221	G525	-6647	121	1271	G425	-7497	121	1321	G325	-8347	121
1222	G523	-6664	261	1272	G423	-7514	261	1322	G323	-8364	261
1223	G521	-6681	121	1273	G421	-7531	121	1323	G321	-8381	121
1224	G519	-6698	261	1274	G419	-7548	261	1324	G319	-8398	261
1225	G517	-6715	121	1275	G417	-7565	121	1325	G317	-8415	121
1226	G515	-6732	261	1276	G415	-7582	261	1326	G315	-8432	261
1227	G513	-6749	121	1277	G413	-7599	121	1327	G313	-8449	121
1228	G511	-6766	261	1278	G411	-7616	261	1328	G311	-8466	261
1229	G509	-6783	121	1279	G409	-7633	121	1329	G309	-8483	121
1230	G507	-6800	261	1280	G407	-7650	261	1330	G307	-8500	261
1231	G505	-6817	121	1281	G405	-7667	121	1331	G305	-8517	121
1232	G503	-6834	261	1282	G403	-7684	261	1332	G303	-8534	261
1233	G501	-6851	121	1283	G401	-7701	121	1333	G301	-8551	121
1234	G499	-6868	261	1284	G399	-7718	261	1334	G299	-8568	261
1235	G497	-6885	121	1285	G397	-7735	121	1335	G297	-8585	121
1236	G495	-6902	261	1286	G395	-7752	261	1336	G295	-8602	261
1237	G493	-6919	121	1287	G393	-7769	121	1337	G293	-8619	121
1238	G491	-6936	261	1288	G391	-7786	261	1338	G291	-8636	261
1239	G489	-6953	121	1289	G389	-7803	121	1339	G289	-8653	121
1240	G487	-6970	261	1290	G387	-7820	261	1340	G287	-8670	261
1241	G485	-6987	121	1291	G385	-7837	121	1341	G285	-8687	121
1242	G483	-7004	261	1292	G383	-7854	261	1342	G283	-8704	261
1243	G481	-7021	121	1293	G381	-7871	121	1343	G281	-8721	121
1244	G479	-7038	261	1294	G379	-7888	261	1344	G279	-8738	261
1245	G477	-7055	121	1295	G377	-7905	121	1345	G277	-8755	121
1246	G475	-7072	261	1296	G375	-7922	261	1346	G275	-8772	261
1247	G473	-7089	121	1297	G373	-7939	121	1347	G273	-8789	121
1248	G471	-7106	261	1298	G371	-7956	261	1348	G271	-8806	261
1249	G469	-7123	121	1299	G369	-7973	121	1349	G269	-8823	121
1250	G467	-7140	261	1300	G367	-7990	261	1350	G267	-8840	261

Pad No.	Designation	CX	CY	Pad No.	GND	-4341.5	-256	Pad No.	Designation	CX	CY
1351	G265	-8857	121	1401	G165	-9707	121	1451	G65	-10557	121
1352	G263	-8874	261	1402	G163	-9724	261	1452	G63	-10574	261
1353	G261	-8891	121	1403	G161	-9741	121	1453	G61	-10591	121
1354	G259	-8908	261	1404	G159	-9758	261	1454	G59	-10608	261
1355	G257	-8925	121	1405	G157	-9775	121	1455	G57	-10625	121
1356	G255	-8942	261	1406	G155	-9792	261	1456	G55	-10642	261
1357	G253	-8959	121	1407	G153	-9809	121	1457	G53	-10659	121
1358	G251	-8976	261	1408	G151	-9826	261	1458	G51	-10676	261
1359	G249	-8993	121	1409	G149	-9843	121	1459	G49	-10693	121
1360	G247	-9010	261	1410	G147	-9860	261	1460	G47	-10710	261
1361	G245	-9027	121	1411	G145	-9877	121	1461	G45	-10727	121
1362	G243	-9044	261	1412	G143	-9894	261	1462	G43	-10744	261
1363	G241	-9061	121	1413	G141	-9911	121	1463	G41	-10761	121
1364	G239	-9078	261	1414	G139	-9928	261	1464	G39	-10778	261
1365	G237	-9095	121	1415	G137	-9945	121	1465	G37	-10795	121
1366	G235	-9112	261	1416	G135	-9962	261	1466	G35	-10812	261
1367	G233	-9129	121	1417	G133	-9979	121	1467	G33	-10829	121
1368	G231	-9146	261	1418	G131	-9996	261	1468	G31	-10846	261
1369	G229	-9163	121	1419	G129	-10013	121	1469	G29	-10863	121
1370	G227	-9180	261	1420	G127	-10030	261	1470	G27	-10880	261
1371	G225	-9197	121	1421	G125	-10047	121	1471	G25	-10897	121
1372	G223	-9214	261	1422	G123	-10064	261	1472	G23	-10914	261
1373	G221	-9231	121	1423	G121	-10081	121	1473	G21	-10931	121
1374	G219	-9248	261	1424	G119	-10098	261	1474	G19	-10948	261
1375	G217	-9265	121	1425	G117	-10115	121	1475	G17	-10965	121
1376	G215	-9282	261	1426	G115	-10132	261	1476	G15	-10982	261
1377	G213	-9299	121	1427	G113	-10149	121	1477	G13	-10999	121
1378	G211	-9316	261	1428	G111	-10166	261	1478	G11	-11016	261
1379	G209	-9333	121	1429	G109	-10183	121	1479	G9	-11033	121
1380	G207	-9350	261	1430	G107	-10200	261	1480	G7	-11050	261
1381	G205	-9367	121	1431	G105	-10217	121	1481	G5	-11067	121
1382	G203	-9384	261	1432	G103	-10234	261	1482	G3	-11084	261
1383	G201	-9401	121	1433	G101	-10251	121	1483	G1	-11101	121
1384	G199	-9418	261	1434	G99	-10268	261	1484	DUM4	-11135	261
1385	G197	-9435	121	1435	G97	-10285	121				
1386	G195	-9452	261	1436	G95	-10302	261				
1387	G193	-9469	121	1437	G93	-10319	121				
1388	G191	-9486	261	1438	G91	-10336	261				
1389	G189	-9503	121	1439	G89	-10353	121				
1390	G187	-9520	261	1440	G87	-10370	261				
1391	G185	-9537	121	1441	G85	-10387	121				
1392	G183	-9554	261	1442	G83	-10404	261				
1393	G181	-9571	121	1443	G81	-10421	121				
1394	G179	-9588	261	1444	G79	-10438	261				
1395	G177	-9605	121	1445	G77	-10455	121				
1396	G175	-9622	261	1446	G75	-10472	261				
1397	G173	-9639	121	1447	G73	-10489	121				
1398	G171	-9656	261	1448	G71	-10506	261				
1399	G169	-9673	121	1449	G69	-10523	121				
1400	G167	-9690	261	1450	G67	-10540	261				

Appendix

Color Filter Arrangement

NT39024 supported the stripe color filter arrangement and the connection are shown as following.



With collaboration of <https://www.displayfuture.com>