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NT3967

TFT LCD Source Driver

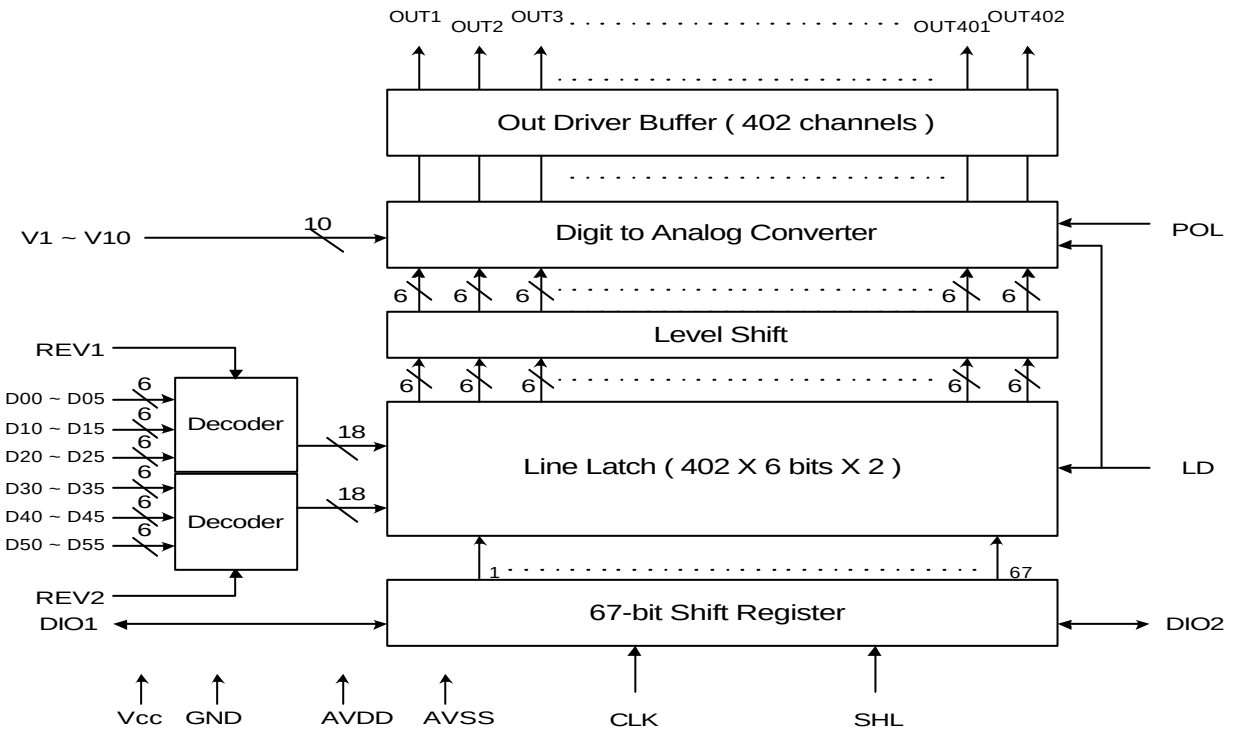
Features

- Output: 402 output channels
- 6-bit resolution /64 gray scales
- Dot inversion with polarity control
- V1 ~ V10 for adjusting Gamma correction
- Power for analog circuit: 6.5 ~ 10 V
- Output dynamic range: 0.1 ~ AVDD-0.1V
- Power consumption of analog circuit: 3 mA
- Power for interface circuit: 2.5~3.6V
- Operating frequency: 65MHz
- Output deviation: 10 ~ 20mV
- Data inversion for reducing EMI
- Cascade function with bi-direction shift control
- CMOS silicon gate (p-type substrate)
- TCP package

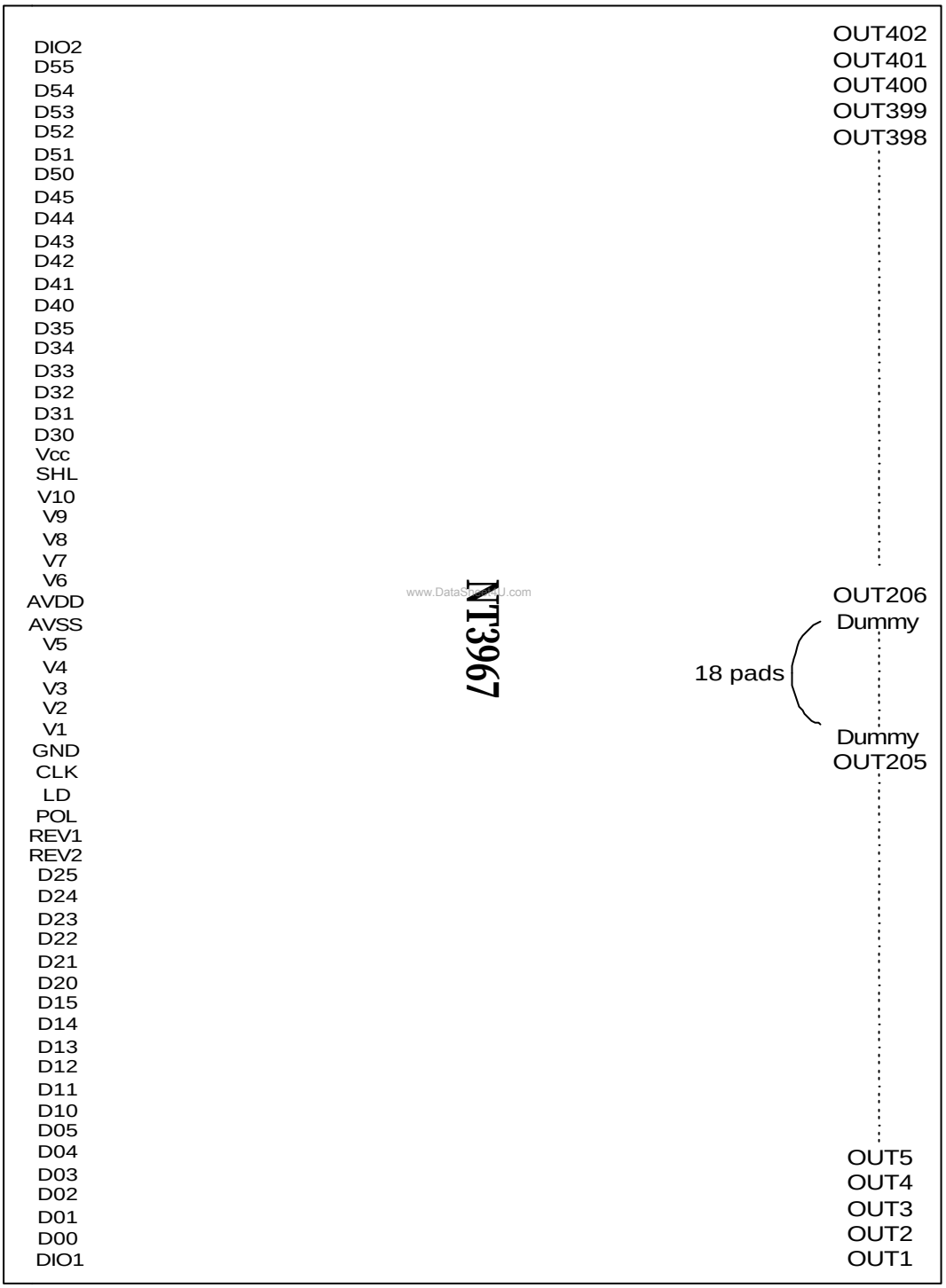
General Description

The NT3967 is a data driver IC for a color TFT LCD panel, SVGA(800*600) and UXGA(1600*1200) applications. For better performance, dot inversion and a wide range voltage output are designed in this chip and for reducing EMI, data inversion control is used. This chip supplies 10 sections of voltage-reference for Gamma correction.

Block diagram



NT3967 Pad configuration (Face up): This figure does not specify the TCP package.



Pin Description

Designation	I/O	Description
D05 ~ D00 D15 ~ D10 D25 ~ D20 D35 ~ D30 D45 ~ D40 D55 ~ D50	I	Data input. For six 6-bit data,2 pixels, of color data (R, G, B) DX5 : MSB; DX0 : LSB
REV1	I	Controls whether the data of D00~D25 are inverted or not. When "REV1"=1 these data will be inverted. EX. "00" → "3F", "07" → "38", "15" → "2A", and so on.
REV2	I	Controls whether the data of D30~D55 are inverted or not, same as REV1.
CLK	I	Clock input; latching data onto the line latches at the rising edge.
V1 ~ V10	I	Gamma correction reference voltage. The voltage of these pins must be AVSS< V10< V9< V8<V7<V6; V5<V4<V3<V2<V1< AVDD
OUT1 ~ OUT402	O	Output drive signals;
SHL	I	Selects left or right shift; SHL="1" : DIO1→OUT1,2,3,4,5,6→OUT7,8,9,10,11,12--→OUT397,398,399,400,401,402= DIO2 SHL="0" : DIO1=OUT1,2,3,4,5,6←OUT7,8,9,10,11,12←-- OUT397,398,399,400,401,402←DIO2
DIO1 DIO2	I/O	Start pulse signal input/output When SHL is applied high (SHL="1"), a start high-pulse on DIO1 is latched at the rising edge of the CLK. Then the data are latched serially onto internal latches at the rising edge of the CLK. After all line latches are filled with data, 67 clocks, a pulse is shifted out through the DIO2 pin at the rising edge of the CLK. This function can cascade two or more devices for dot-size expansion. In normal applications, the DIO2 signal of the first device is connected to the DIO1 of the second stage, the DIO2 of the second one is connected to the DIO1 of the third, and so on, like a daisy chain. In contrast, when SHL is applied low, a start pulse inputs on DIO2, and a pulse outputs through DIO1. *Remark: The input pulse-width of DIO1/2 may exceed 1 clock-cycle.
LD	I	Latches the polarity of outputs and switches the new data to outputs. 1. At the rising edge, latches the "POL" signal to control the polarity of the outputs. 2. The pin also controls the switch of the line registers that switches the new incoming data to outputs. *Remark: The LD may switch the new data to outputs at anytime even if the line data are not completely full.
POL	I	Polarity selector for the dot-inversion control. Available at the rising edge of LD "POL" value is latched at the rising edge of "LD" to control the polarity of the even or odd outputs. "POL=1" indicates that even outputs are of positive polarity with a voltage range from V1~V5, and odd outputs are of negative polarity with a voltage range from V6 to V10. On the other hand, if LD receives low level "POL", even outputs are of negative polarity and odd outputs are of positive polarity. POL=1: Even outputs range from V1 ~ V5 Odd outputs range from V6 ~ V10 POL=0: Even outputs range from V6 ~ V10 Odd outputs range from V1 ~ V5
AVDD	I	Power supply for analog circuit
AVSS	I	Ground pin for analog circuit
Vcc	I	Power supply for digital circuit
GND	I	Ground pin for digital circuit
Dummy	-	Dummy pads

SHL	DIO1	DIO2	SHIFT
1	Input	Output	Right
0	Output	Input	Left

Power on/off sequence:
This IC is a high-voltage LCD driver, so it may be damaged by a large current flow when an incorrect power sequence is used. The recommend ed power on/off sequence is to first connect the logical power, Vcc & GND and then the drive power, AVDD&AVSS with V1~V10 . When shutting off the power, first shut off the drive power and then the logic system, or turn off all power simultaneously.

Relationship between the order of input data and output channels

(1) SHL=" 1" , Start pulse from DIO1, shift right

Output	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	- - -	OUT402
Order	First data						--→	Last data
Data	D05~D00	D15~D10	D25~D20	D35~D30	D45~D40	D55~D50	- - -	D55~D50

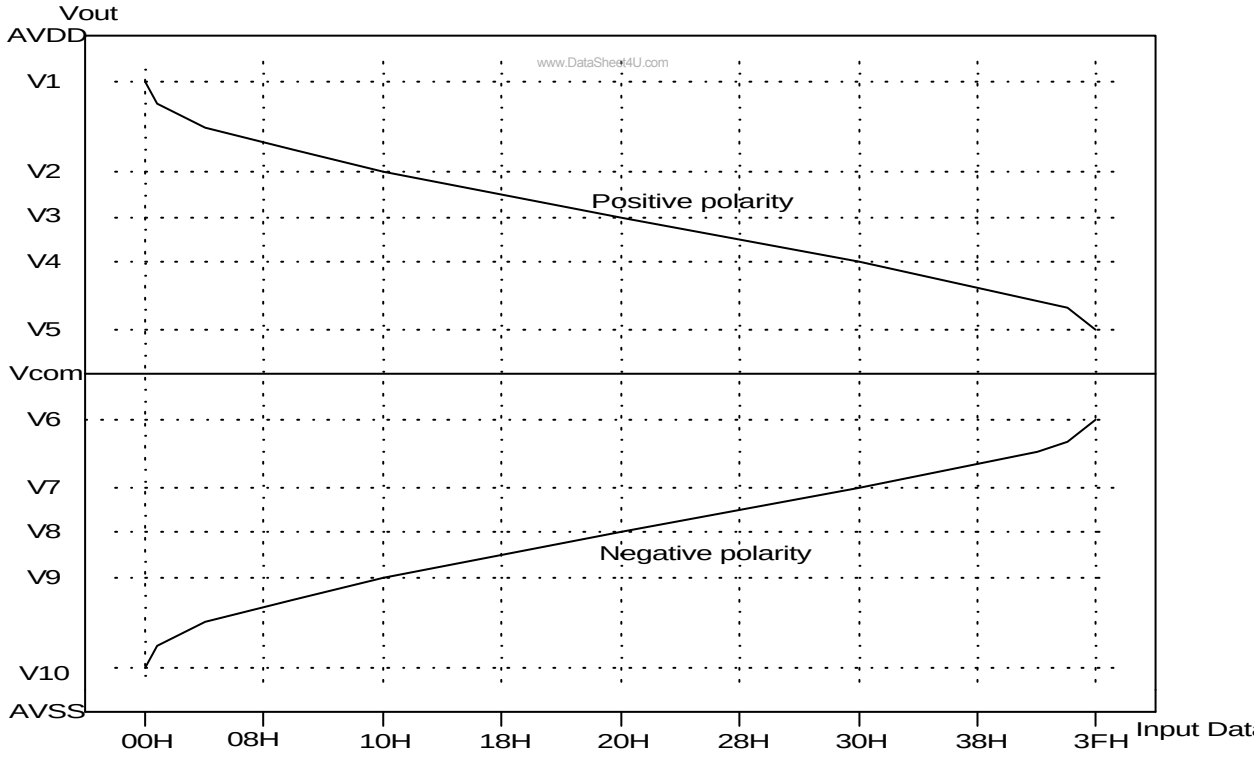
(2) SHL=" 0" , Start pulse from DIO2, shift left

Output	OUT397	OUT398	OUT399	OUT400	OUT401	OUT402	- - -	OUT6
Order	First data						--→	Last data
Data	D05~D00	D15~D10	D25~D20	D35~D30	D45~D40	D55~D50	- - -	D55~D50

Relationship between input data and output voltage

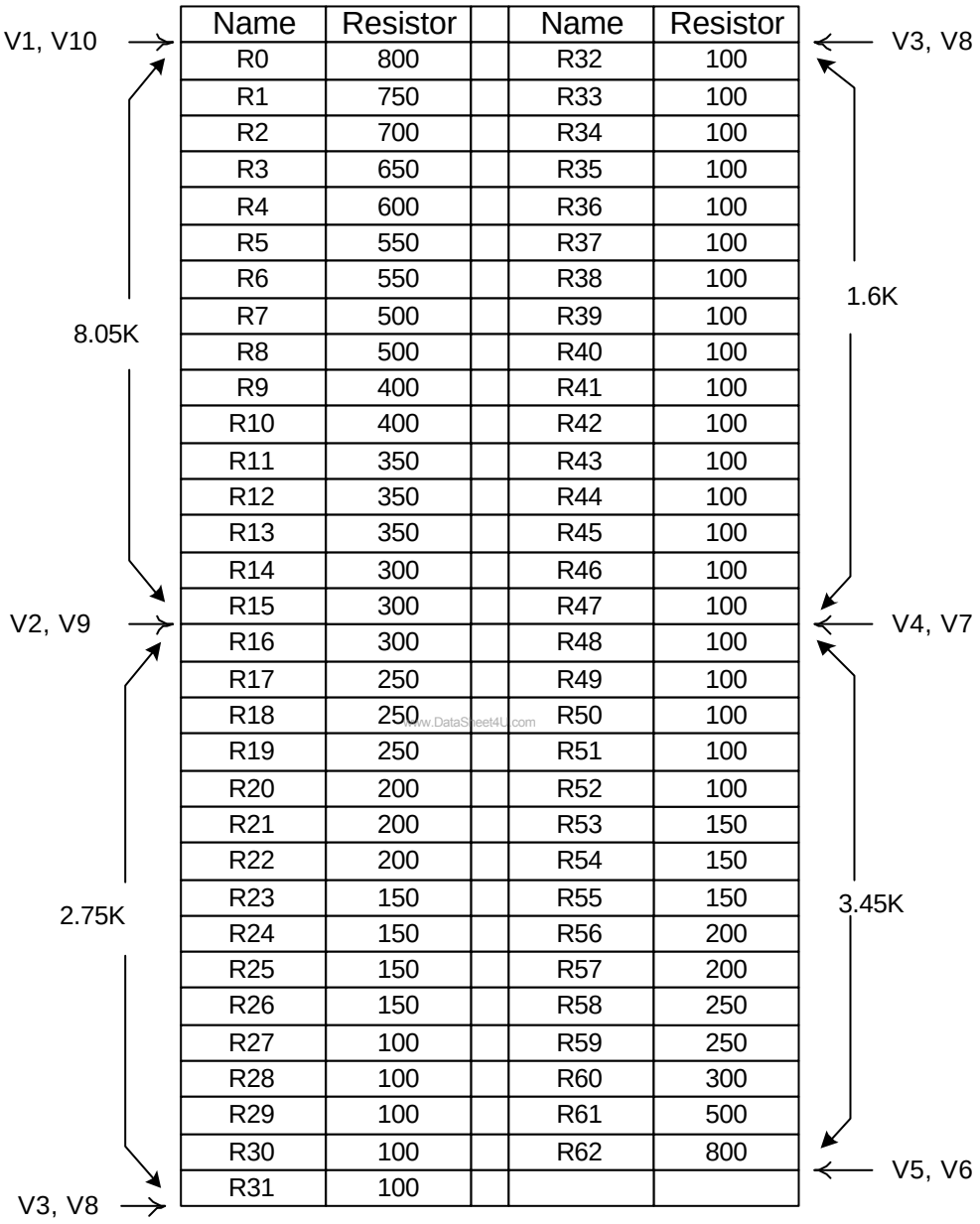
The figure below shows the relationship between the input data and the output voltage with the polarity. The range of V1~V5 is for positive polarity, and V6 ~ V10 for negative polarity. Please refer to the following page to get the relative re sistor value and voltage calculation method.

Gamma correction diagram



Remark: AVDD-0.1 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5; V6 ≥ V7 ≥ V8 ≥ V9 ≥ V10 ≥AVSS+0.1V

Gamma correction resistor



Name	Resistor		Name	Resistor
R0	800		R32	100
R1	750		R33	100
R2	700		R34	100
R3	650		R35	100
R4	600		R36	100
R5	550		R37	100
R6	550		R38	100
R7	500		R39	100
R8	500		R40	100
R9	400		R41	100
R10	400		R42	100
R11	350		R43	100
R12	350		R44	100
R13	350		R45	100
R14	300		R46	100
R15	300		R47	100
R16	300		R48	100
R17	250		R49	100
R18	250		R50	100
R19	250		R51	100
R20	200		R52	100
R21	200		R53	150
R22	200		R54	150
R23	150		R55	150
R24	150		R56	200
R25	150		R57	200
R26	150		R58	250
R27	100		R59	250
R28	100		R60	300
R29	100		R61	500
R30	100		R62	800
R31	100			

Total impedance, Rn=R0 ~ R62, equals 15.85K

Output Voltage VS Input Data

Data	Output Voltage (Positive polarity)	Output Voltage (Negative polarity)
00H	V1	V10
01H	V2 + (V1 – V2) X 7250/8050	V10 + (V9 – V10) X 800/8050
02H	V2 + (V1 – V2) X 6500/8050	V10 + (V9 – V10) X 1550/8050
03H	V2 + (V1 – V2) X 5800/8050	V10 + (V9 – V10) X 2250/8050
04H	V2 + (V1 – V2) X 5150/8050	V10 + (V9 – V10) X 2900/8050
05H	V2 + (V1 – V2) X 4550/8050	V10 + (V9 – V10) X 3500/8050
06H	V2 + (V1 – V2) X 4000/8050	V10 + (V9 – V10) X 4050/8050
07H	V2 + (V1 – V2) X 3450/8050	V10 + (V9 – V10) X 4600/8050
08H	V2 + (V1 – V2) X 2950/8050	V10 + (V9 – V10) X 5100/8050
09H	V2 + (V1 – V2) X 2450/8050	V10 + (V9 – V10) X 5600/8050
0AH	V2 + (V1 – V2) X 2050/8050	V10 + (V9 – V10) X 6000/8050
0BH	V2 + (V1 – V2) X 1650/8050	V10 + (V9 – V10) X 6400/8050
0CH	V2 + (V1 – V2) X 1300/8050	V10 + (V9 – V10) X 6750/8050
0DH	V2 + (V1 – V2) X 950/8050	V10 + (V9 – V10) X 7100/8050
0EH	V2 + (V1 – V2) X 600/8050	V10 + (V9 – V10) X 7450/8050
0FH	V2 + (V1 – V2) X 300/8050	V10 + (V9 – V10) X 7750/8050
10H	V2	V9
11H	V3 + (V2 – V3) X2450/2750	V9 + (V8 – V9) X 300/2750
12H	V3 + (V2 – V3) X 2200/2750	V9 + (V8 – V9) X 550/2750
13H	V3 + (V2 – V3) X 1950/2750	V9 + (V8 – V9) X 800/2750
14H	V3 + (V2 – V3) X 1700/2750	V9 + (V8 – V9) X 1050/2750
15H	V3 + (V2 – V3) X 1500/2750	V9 + (V8 – V9) X 1250/2750
16H	V3 + (V2 – V3) X 1300/2750	V9 + (V8 – V9) X 1450/2750
17H	V3 + (V2 – V3) X 1100/2750	V9 + (V8 – V9) X 1650/2750
18H	V3 + (V2 – V3) X 950/2750	V9 + (V8 – V9) X 1800/2750
19H	V3 + (V2 – V3) X 800/2750	V9 + (V8 – V9) X 1950/2750
1AH	V3 + (V2 – V3) X 650/2750	V9 + (V8 – V9) X 2100/2750
1BH	V3 + (V2 – V3) X 500/2750	V9 + (V8 – V9) X 2250/2750
1CH	V3 + (V2 – V3) X 400/2750	V9 + (V8 – V9) X 2350/2750
1DH	V3 + (V2 – V3) X 300/2750	V9 + (V8 – V9) X 2450/2750
1EH	V3 + (V2 – V3) X 200/2750	V9 + (V8 – V9) X 2550/2750
1FH	V3 + (V2 – V3) X 100/2750	V9 + (V8 – V9) X 2650/2750
20H	V3	V8
21H	V4 + (V3 – V4) X 1500/1600	V8 + (V7 – V8) X 100/1600
22H	V4 + (V3 – V4) X 1400/1600	V8 + (V7 – V8) X 200/1600
23H	V4 + (V3 – V4) X 1300/1600	V8 + (V7 – V8) X 300/1600
24H	V4 + (V3 – V4) X 1200/1600	V8 + (V7 – V8) X 400/1600
25H	V4 + (V3 – V4) X 1100/1600	V8 + (V7 – V8) X 500/1600
26H	V4 + (V3 – V4) X 1000/1600	V8 + (V7 – V8) X 600/1600
27H	V4 + (V3 – V4) X 900/1600	V8 + (V7 – V8) X 700/1600
28H	V4 + (V3 – V4) X 800/1600	V8 + (V7 – V8) X 800/1600
29H	V4 + (V3 – V4) X 700/1600	V8 + (V7 – V8) X 900/1600
2AH	V4 + (V3 – V4) X 600/1600	V8 + (V7 – V8) X 1000/1600
2BH	V4 + (V3 – V4) X 500/1600	V8 + (V7 – V8) X 1100/1600
2CH	V4 + (V3 – V4) X 400/1600	V8 + (V7 – V8) X 1200/1600
2DH	V4 + (V3 – V4) X 300/1600	V8 + (V7 – V8) X 1300/1600
2EH	V4 + (V3 – V4) X 200/1600	V8 + (V7 – V8) X 1400/1600
2FH	V4 + (V3 – V4) X 100/1600	V8 + (V7 – V8) X 1500/1600

Output Voltage VS Input Data (continued)

Data	Output Voltage (Positive polarity)	Output Voltage (Negative polarity)
30H	V4	V7
31H	V5 + (V4 – V5) X 3350/3450	V7 + (V6 – V7) X 100/3450
32H	V5 + (V4 – V5) X 3250/3450	V7 + (V6 – V7) X 200/3450
33H	V5 + (V4 – V5) X 3150/3450	V7 + (V6 – V7) X300/3450
34H	V5 + (V4 – V5) X 3050/3450	V7 + (V6 – V7) X 400/3450
35H	V5 + (V4 – V5) X 2950/3450	V7 + (V6 – V7) X 500/3450
36H	V5 + (V4 – V5) X 2800/3450	V7 + (V6 – V7) X 650/3450
37H	V5 + (V4 – V5) X 2650/3450	V7 + (V6 – V7) X 800/3450
38H	V5 + (V4 – V5) X 2500/3450	V7 + (V6 – V7) X 950/3450
39H	V5 + (V4 – V5) X 2300/3450	V7 + (V6 – V7) X 1150/3450
3AH	V5 + (V4 – V5) X 2100/3450	V7 + (V6 – V7) X 1350/3450
3BH	V5 + (V4 – V5) X 1850/3450	V7 + (V6 – V7) X 1600/3450
3CH	V5 + (V4 – V5) X 1600/3450	V7 + (V6 – V7) X 1850/3450
3DH	V5 + (V4 – V5) X 1300/3450	V7 + (V6 – V7) X 2150/3450
3EH	V5 + (V4 – V5) X 800/3450	V7 + (V6 – V7) X 2650/3450
3FH	V5	V6

Absolute Maximum Ratings*

Digital supply voltage, Vcc	-0.5V to 5V
Analog supply voltage, AVDD	-0.5V to +11V
Supply voltage, V1~ V10	-0.3 ~AVDD+0.3
Digital input voltage	-0.5V to Vcc+0.5V
Output voltage, DIO1 & DIO2	-0.5V to Vcc+0.5V
Output voltage,OUT1~OUT420	-0.5V to AVDD+0.5V
Storage temperature	-55°C to 100°C
Operating temperature	-10°C to 75°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Vcc=2.5~3.6V , AVDD=6.5~10V, AVSS=GND=0V, TA=-10°C~75°C)

(For the digital circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	Vcc	2.5	-	3.6	V	Digital power
Low Level Input Voltage	Vil	0	-	0.3xVcc	V	For the digital circuit
High Level Input Voltage	Vih	0.7xVcc	-	Vcc	V	For the digital circuit
High Level Output Voltage	Voh	Vcc-0.3V	-	-	V	DIO1/2, Ioh=500uA
Low Level Output Voltage	Vol	-	-	GND+0.3V	V	DIO1/2, Iol=-500uA
Input Leakage Current	Ii	-	-	±1	μA	For the digital circuit
Digital Stand-by current	Ist	-	-	50	μA	CLK is stopped, DIO1/2 No load
Digital Operating Current	Icc	-	3	5	mA	Fclk=40 MHz, FLD=50KHz

(For the analog circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	AVDD	6.5	8.4	10	V	For the analog circuit power
Input level of V1 ~ V5	Vref	0.4AVDD	-	AVDD-0.1	V	Gamma correction voltage
Input level of V6 ~ V10	Vref	0.1		0.6AVDD	V	Gamma correction voltage
Voltage Output Deviation	Vvd	-	±20	±25	mV	Vo=0.1V ~ 1.5V & AVDD-1.5 ~ AVDD-0.1V
			±10	±20	mV	Vo=1.5V ~ AVDD-1.5V
Voltage Output Offset	Voc		±10		mV	
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	OUT1 ~ OUT402
Sinking Current of outputs	IOL	-150	-180	-	μA	OUT1 ~ OUT402; Vo=0.1V V.S 1.1V
Driving Current of outputs	IOH	150	200	-	μA	OUT1 ~ OUT402; Vo=9.9V V.S 8.9V
Impedance of Gamma Correction	Ri	0.8*Rn	Rn	1.3*Rn	ohm	Rn=15850 ohm, from V1 ~ V5 & V6~V10
Analog Operating Current	IDD	-	3	6	mA	No load, Fclk=33MHz, FLD=50KHz

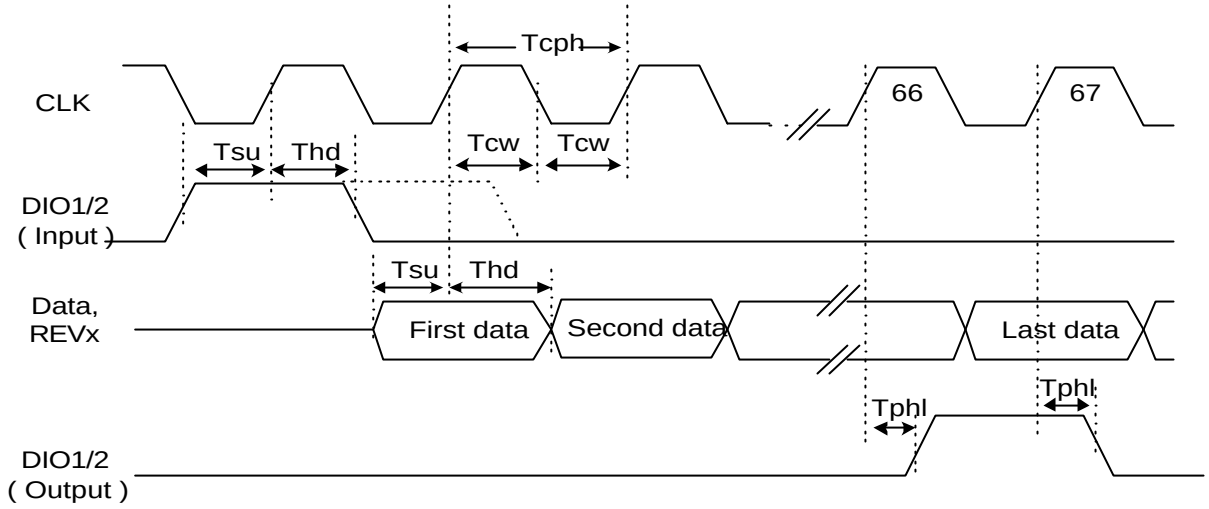
AC Electrical Characteristics 1 (V_{CC} =3.0~3.6V , AV_{DD}=6.5~10V, AVSS=GND=0V, T_A= -10~75°C)

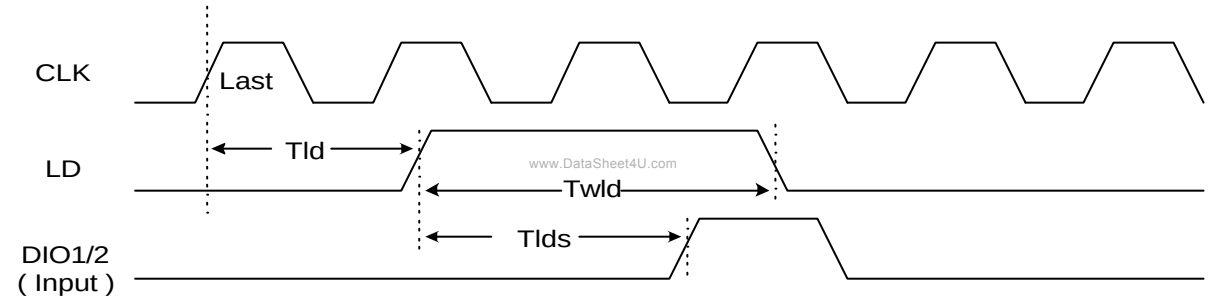
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	-	65	Mhz	
CLK period cycle	Tcph	15	-	-	ns	
CLK pulse width	Tcw	6	-	-	ns	
Data set-up time	Tsu	4	-	-	ns	D00 ~ D55, REVx and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	D00 ~ D55, REVx and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	6	-	11	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to DIO1/2	Tlds	2	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	4.5	9	us	96% final value or below with 30mV precision , CL=75pF, R=5K ohm
Output loading	CL	-	-	75	pF	For OUT1 ~ OUT402

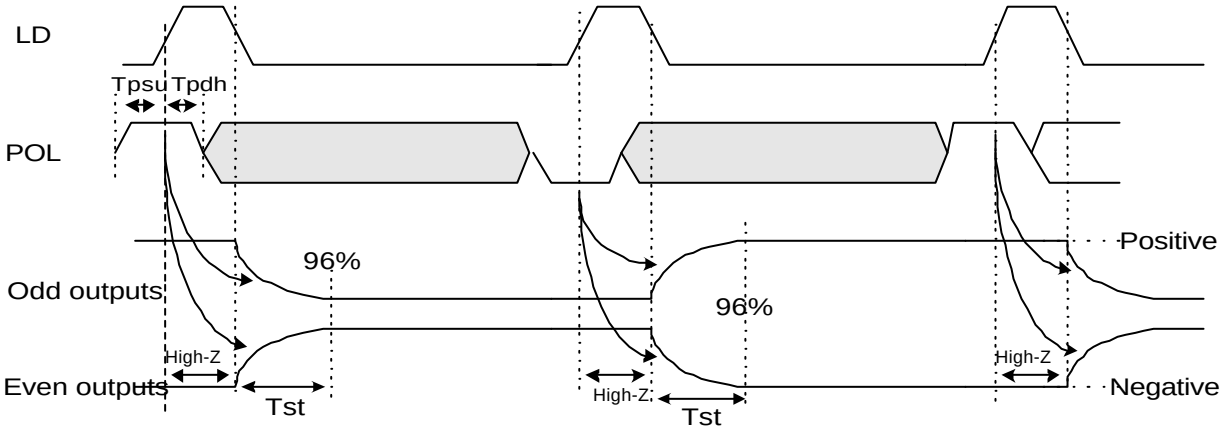
AC Electrical Characteristics 2 (V_{CC} =2.5~3.0V , AV_{DD}=6.5~10V, AVSS=GND=0V, T_A= -10~75°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	-	45	Mhz	
CLK period cycle	Tcph	22	-	-	ns	
CLK pulse width	Tcw	8	-	-	ns	
Data set-up time	Tsu	6	-	-	ns	D00 ~ D55, REVx and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	D00 ~ D55, REVx and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	-	-	15	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to DIO1/2	Tlds	2	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	4.5	9	us	96% final value or below with 30mV precision , CL=75pF, R=5K ohm
Output loading	CL	-	-	75	pF	For OUT1 ~ OUT402

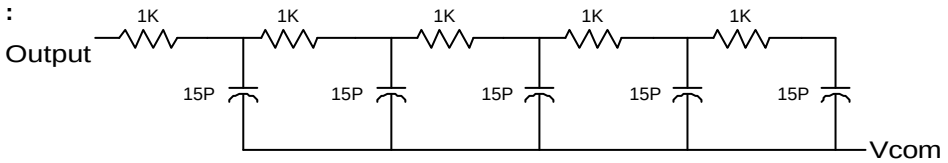
Timing Diagram







Output load condition :



Function operation