NOVATEK 聯詠科技

Data Sheet

NT50198

TFT-LCD 3-Channel Charge Pump Power IC

Draft Spec.

Version 0.05
2012/08/22

Index

Reversion History

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Preliminary Version	Green	Max Tang		2012/03/23
0.01	Update feature and pin define.	Green	Max Tang		2012/04/11
0.02	Update power on/off sequence and package	Green	Max Tang		2012/05/07
0.03	Update power on/off sequence and package	Green	Max Tang		2012/05/30
0.04	Update TDFN12/16 package Update thermal pad description (page:8/9/10)	Green	Max Tang		2012/06/19
0.05	Update external component selection guide (page.12) Update Dickson doubler application (page19,20) Update paralleling two devices (page.21) Update absolute maximum rating spec(page.27) Update electrical spec(page.28) Update typical characteristic (page.18~19) Update FPC stiffener suggestion and package information Add TDFN12 loading curve and pump efficiency(page20) .	Green	Max Tang		2012/009/07

1. General Description

The NT50198 is a high-performance step-up charge pump and inverter to generate two output voltages; it is including pumping controllers for positive and negative output voltage. The following content contains the detailed description and the information of component selection.

The positive charge-pump controller provides adjustable regulated output AVDD and fixed -1 ratio of AVEE to supply the TFT.

The pumping clock can be generated by internal circuit, to reduce the control signal from driver IC. Or the charge and pump state can be synchronized with LCD display TE signal (PSYNC), it can reduce the interference to display quality when states change.

The device requires only five (12 pins) or seven (16 pins) small and low-cost ceramic capacitors.

NT50198 is available in TDFN-12 / TDFN-16 / QFN-16 pins package for smart phone LCD panel's driver IC.

Note: According to the FPC layout experience, the components on the FPC may have chance to fall off when wind the FPC. So we strongly suggest to add the Stiffener under the FPC backside area of NT50198.

2. Features

- Charge pump x2 mode for positive AVDD and x-1 mode for negative AVEE .
- 2.5V to 4.8V input supply voltage range
  - AVDD output range：5.8V to 6.0V.
  - AVEE output range：-5.8V to -6.0V.
  - VCL output range：-2.5V to -3.2V.
- Charge pump clock synchronized with PSYNC for benefit of low noise.
- Positive and Negative regulated charge Pump with Diode free.
- External Capacitor 5C or 7C only.
- QFN-16 (3.0mm * 3.0mm * 0.8 mm) package is available.
- TDFN-12 (1.5mm * 2.4mm * 0.5 mm) package is available.
- TDFN-16 (1.5mm * 3.2mm * 0.5 mm) package is available.
- Control signals voltage 1.65V to 4.8V.

3. Block Diagram and Operating Circuit

3.1：12 pins block diagram

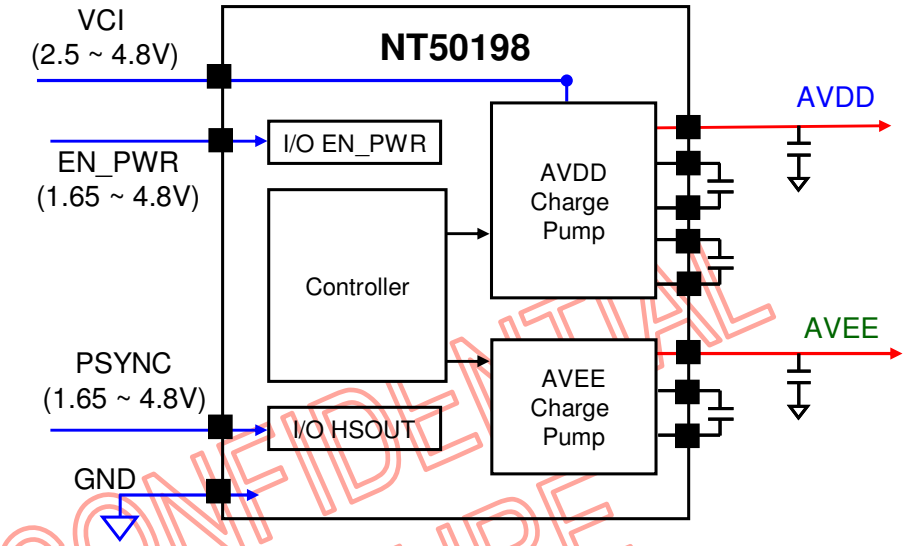


Figure1：12 pins block diagram

3.2：16 pins block diagram case1

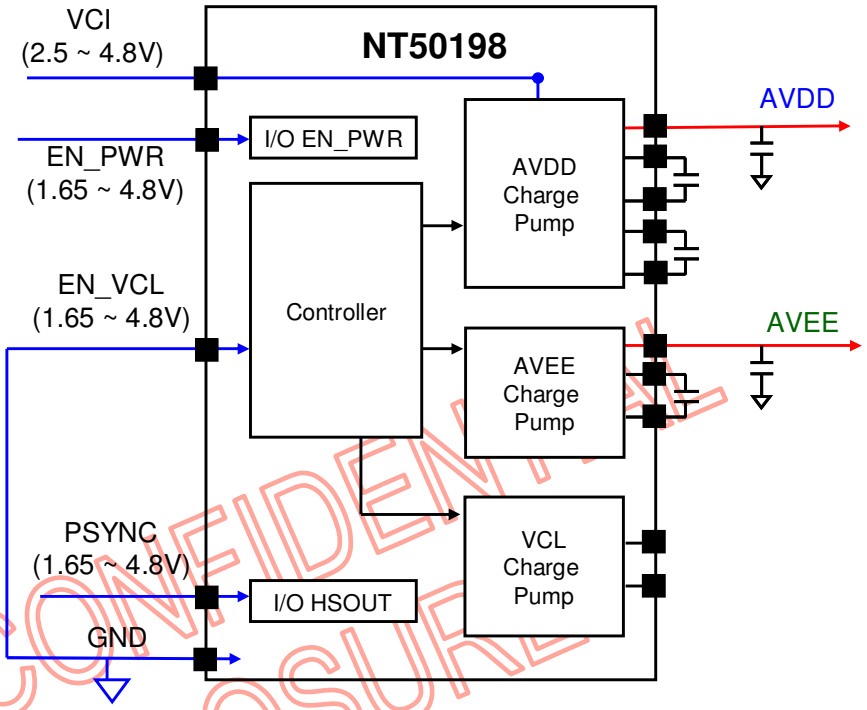


Figure2：16 pins block diagram for AVDD / AVEE

3.3：16 pins block diagram case2

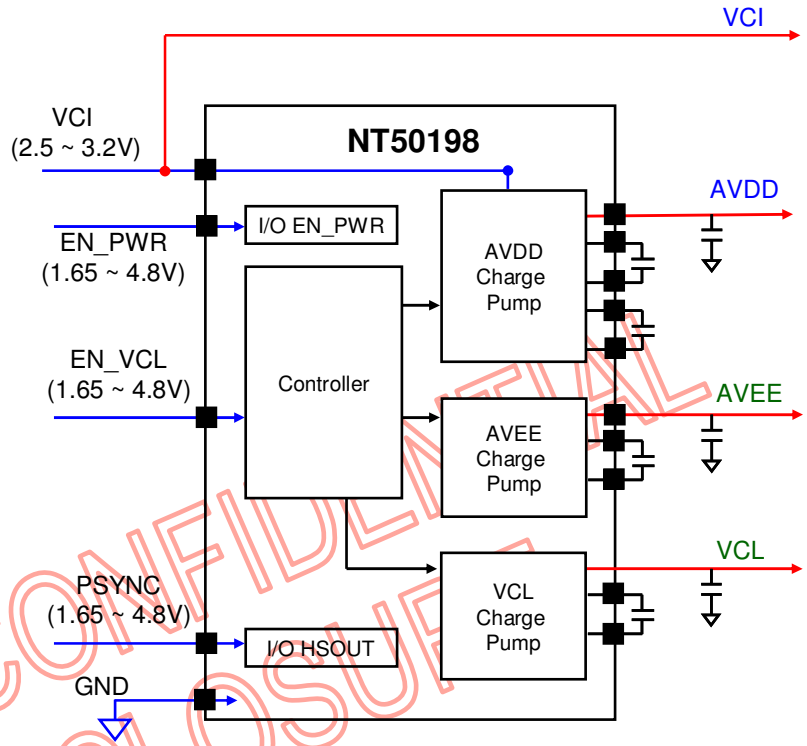


Figure3：16 pins block diagram for AVDD / AVEE / VCL / VCI

Note1: please use EN_VCL pin to control the output state of VCL output pin.

Note2: If VCI input voltage is larger than 3.2V, please tie EN_VCL to GND because of MV device stress.

(It means it can not output VCL voltage at VCI > 3.2v case, or power IC will be damaged)

4. Pin Description and package

4.1 TDFN-12 pin

Pad No.	Pad name	Description
1	C21P	Capacitor connection pin for the step-up circuit which generate AVEE.
2	AVDD	Positive AVDD output pin.
3	C11P	Capacitor connection pin for the step-up circuit which generate AVDD.
4	C11M	Capacitor connection pin for the step-up circuit which generate AVDD.
5	GND	Ground pin.
6	EN_PWR	Power enable control signal.
7	PSYNC	Power-sync control signal generated from driver IC. *Note : If not used this clock synchronized signal, please tie to GND.*
8	VCI	Power supply input pin.
9	C12M	Capacitor connection pin for the step-up circuit which generate AVDD.
10	C12P	Capacitor connection pin for the step-up circuit which generate AVDD.
11	AVEE	Negative AVEE output pin.
12	C21M	Capacitor connection pin for the step-up circuit which generate AVEE.
13	Thermal-pad	Connect to GND.

Table1 : TDFN-12 pins description

4.2 TDFN-12 package

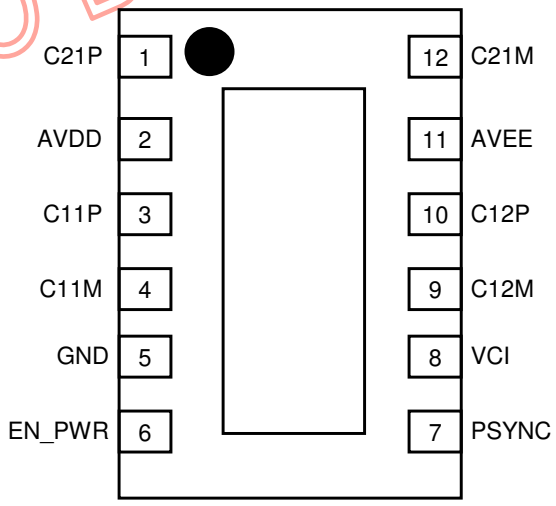


Figure4 : TDFN-12 pins assignment

4.3 TDFN-16 pin

Pad No.	Pad name	Description
1	C21P	Capacitor connection pin for the step-up circuit which generate AVEE.
2	AVDD	Positive AVDD output pin.
3	C11P	Capacitor connection pin for the step-up circuit which generate AVDD.
4	C11M	Capacitor connection pin for the step-up circuit which generate AVDD.
5	GND	Ground pin.
6	EN_VCL	Power enable control signal for AVDD and AVEE. *Note: If driver IC will use VCL voltage, please tie to EN_PWR pin.*
7	EN_PWR	Power enable control signal for AVDD and AVEE.
8	PSYNC	Power-sync control signal generated from driver IC. *Note : If not used this clock synchronized signal, please tie to GND.*
9	VCL	Negative VCL output pin. *Note: If not used, please let it open.*
10	C31M	Capacitor connection pin for the step-up circuit which generate VCL. *Note: If not used, please let it open.*
11	C31P	Capacitor connection pin for the step-up circuit which generate VCL. *Note: If not used, please let it open.*
12	VCI	Power supply input pin.
13	C12M	Capacitor connection pin for the step-up circuit which generate AVDD.
14	C12P	Capacitor connection pin for the step-up circuit which generate AVDD.
15	AVEE	Negative AVEE output pin.
16	C21M	Capacitor connection pin for the step-up circuit which generate AVEE.
17	Thermal-pad	Connect to GND.

Table2 : TDFN-16 pins description

4.4 TDFN-16 package

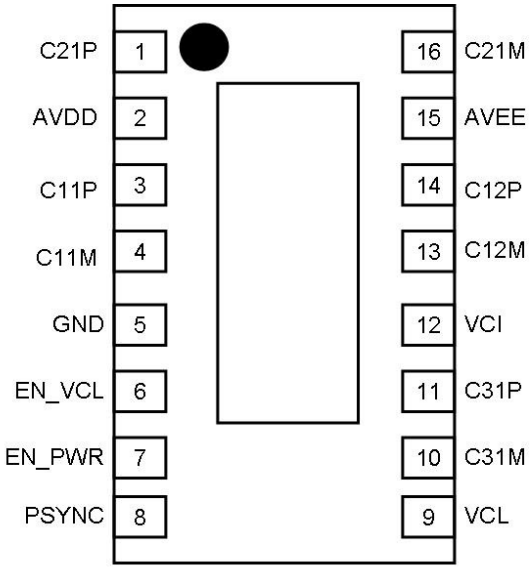


Figure5 : TDFN-16 pins assignment

4.5 QFN-16 pin

Pad No.	Pad name	Description
1	C11P	Capacitor connection pin for the step-up circuit which generate AVDD.
2	C11M	Capacitor connection pin for the step-up circuit which generate AVDD.
3	GND	Ground.
4	EN_VCL	Power enable control signal for AVDD and AVEE. *Note: If driver IC will use VCL voltage, please tie to EN_PWR pin.*
5	EN_PWR	Power enable control signal for AVDD and AVEE.
6	VCL	Negative VCL output pin. *Note: If not used, please let it open.*
7	PSYNC	Power-sync control signal generated from driver IC. *Note : If not used this clock synchronized signal, please tie to GND.*
8	C31M	Capacitor connection pin for the step-up circuit which generate VCL. *Note: If not used, please let it open.*
9	C31P	Capacitor connection pin for the step-up circuit which generate VCL.. *Note: If not used, please let it open.*
10	VCI	Power supply input pin.
11	C12M	Capacitor connection pin for the step-up circuit which generate AVDD.
12	C12P	Capacitor connection pin for the step-up circuit which generate AVDD.
13	AVEE	Negative AVEE output pin.
14	C21M	Capacitor connection pin for the step-up circuit which generate AVEE.
15	C21P	Capacitor connection pin for the step-up circuit which generate AVEE.
16	AVDD	Positive AVDD output pin.
17	Thermal-pad	Connect to GND.

Table3 : QFN-16 pins description

4.6 QFN-16 pins package

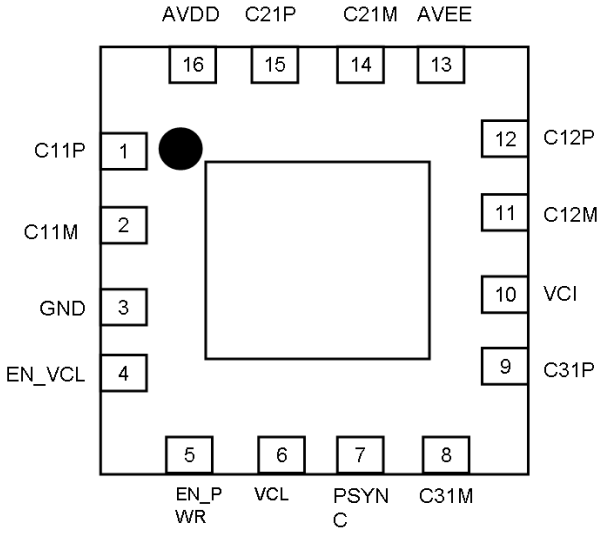


Figure7 : QFN-16 pins assignment

5. External Component List

5.1 12 pins component list

Number	Pad Name	Connection		Typical Value
1	AVDD	Connect a capacitor (Max. 10V):	AVDD -------| |-------- GND	2.2 uF
2	AVEE	Connect a capacitor (Max. 10V):	AVEE--------| |-------- GND	2.2 uF
3	C11P/M	Connect a capacitor (Max. 10V):	C11P -------| |-------- C11M	1.0 uF
4	C12P/M	Connect a capacitor (Max. 10V):	C12P -------| |-------- C12M	1.0 uF
5	C21P/M	Connect a capacitor (Max. 10V):	C21P--------| |-------- C21M	1.0 uF
6	VCI (option)	Connect a capacitor (Max. 10V):	VCI--------| |-------- GND	2.2 uF

5.2 16 pins component list

Number	Pad Name	Connection		Typical Value
1	AVDD	Connect a capacitor (Max. 10V):	AVDD -------| |-------- GND	2.2 uF
2	AVEE	Connect a capacitor (Max. 10V):	AVEE--------| |-------- GND	2.2 uF
3	C11P/M	Connect a capacitor (Max. 10V):	C11P -------| |-------- C11M	1.0 uF
4	C12P/M	Connect a capacitor (Max. 10V):	C12P -------| |-------- C12M	1.0 uF
5	C21P/M	Connect a capacitor (Max. 10V):	C21P--------| |-------- C21M	1.0 uF
6	VCL	Connect a capacitor (Max. 10V):	VCL----------| |-------- GND	1.0 uF
7	C31P/M	Connect a capacitor (Max. 10V):	C31P--------| |-------- C31M	1.0 uF
8	VCI (option)	Connect a capacitor (Max. 10V):	VCI--------| |-------- GND	2.2 uF

Note: Due to the pump efficiency is sensitive to the performance of capacitors, please select the capacitor which is not various by the frequency, temperature, and environments. (X7R series is recommended; do not use Y5V series of capacitor.)

capacitor	size	parts recommandation
1.0uF	0603	GRM188R61C105KA93D
2.2uF	0603	GRM188R61C225KE15D
2.2uF	0805	GRM21BR61C225KA88L

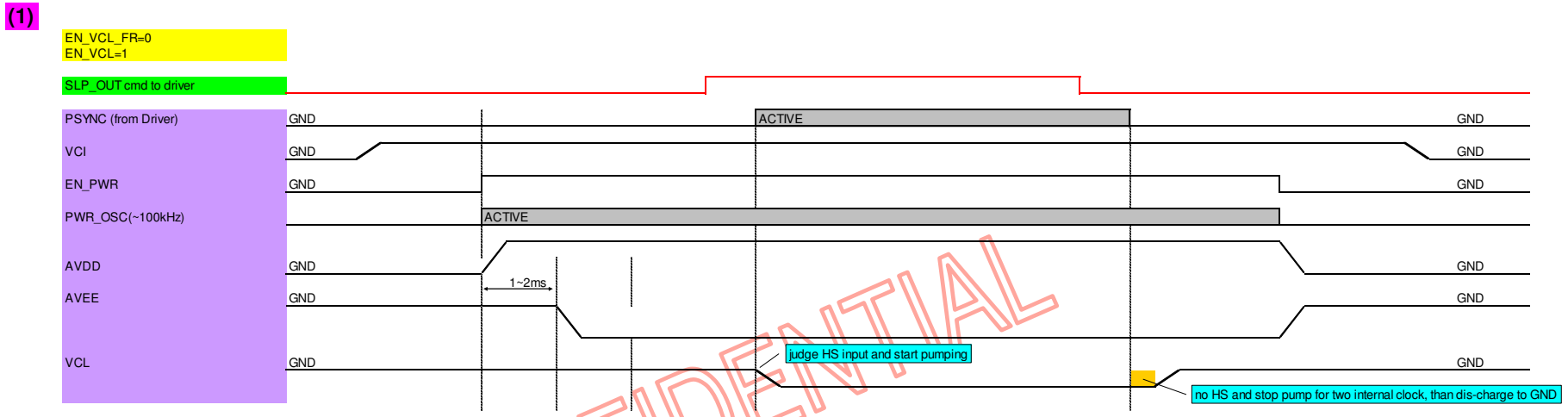
6. Application information

The NT50198 can provide a suitable and stable voltage level to TFT LCD driver IC, and NT50198 can refer to PSYNC signal to switch from charge state to pump state and vice versa. This function can avoid state changing noise to interfere display quality. If the driver IC or baseband can not provide PSYNC, please connect PSYNC signal to GND pin for free-running mode (Internal frequency =125 KHz). The difference between free-running mode and sync mode is that the display quality may be worse in free-running mode. It needs larger stable capacitor to reduce the ripple noise. In sync mode, due to the noise is generated at display porch area; it will not be observed on the panels.

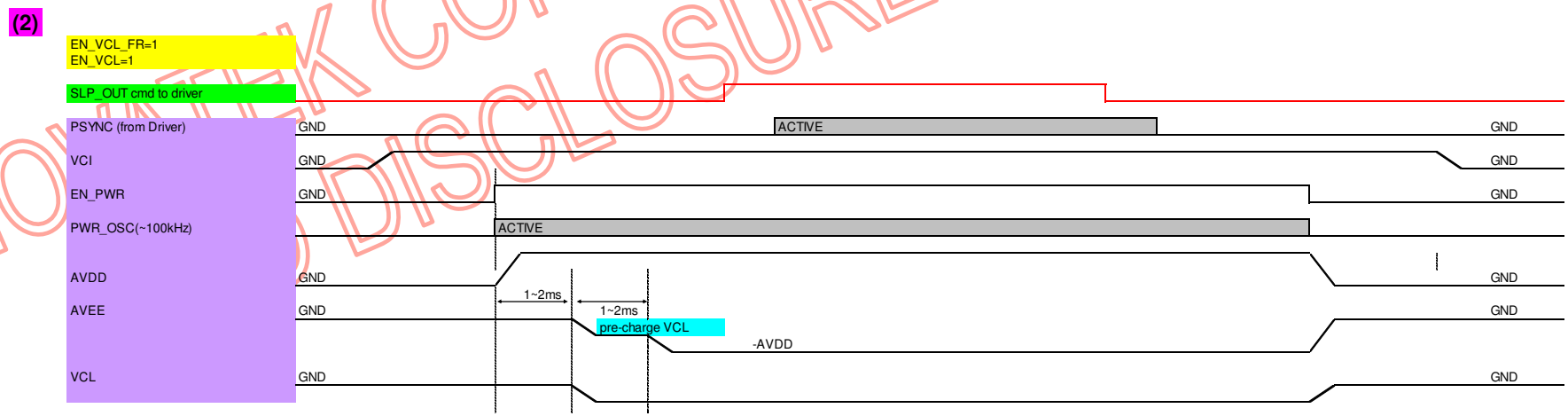
About the power on/off sequence, please refer to the next chapter in details.

6.1：Power on / off sequence：

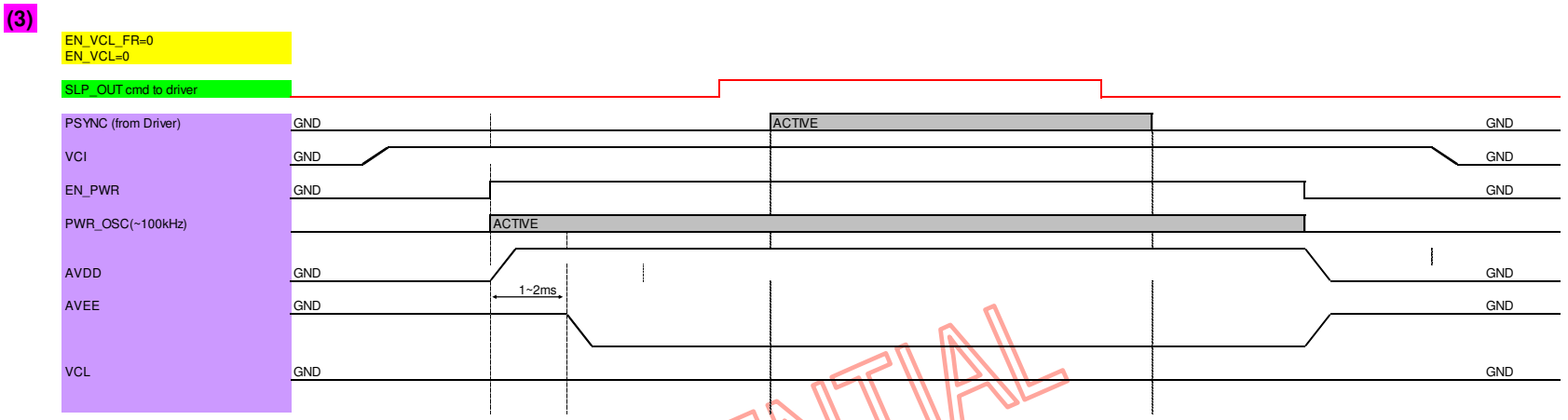
Case 1: EN_VCL = 1 and EN_VCL_FR = 0 (CP option):



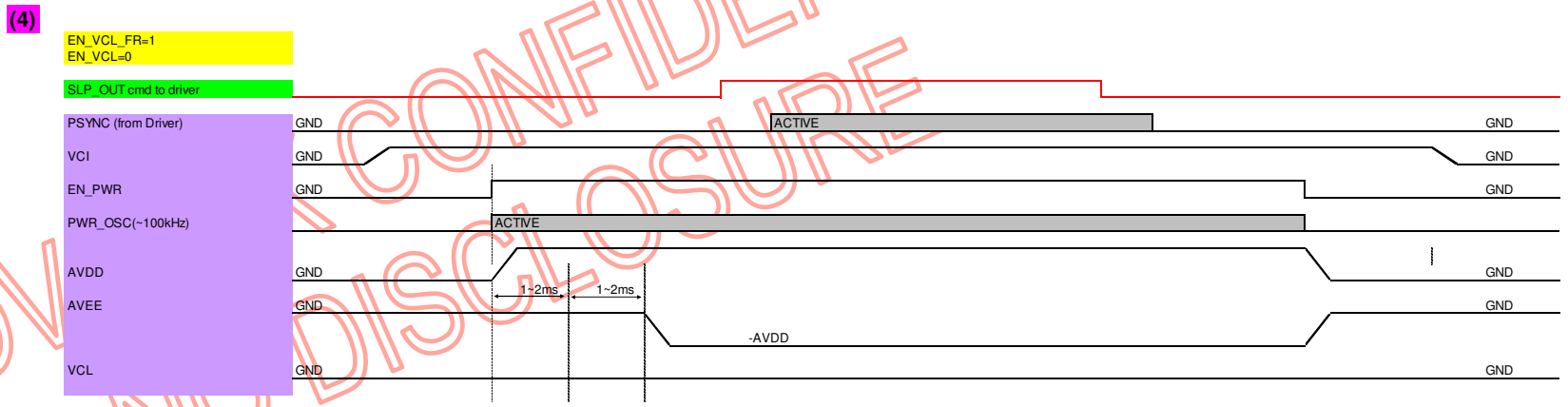
Case 2: EN_VCL = 1 and EN_VCL_FR = 1 (CP option):



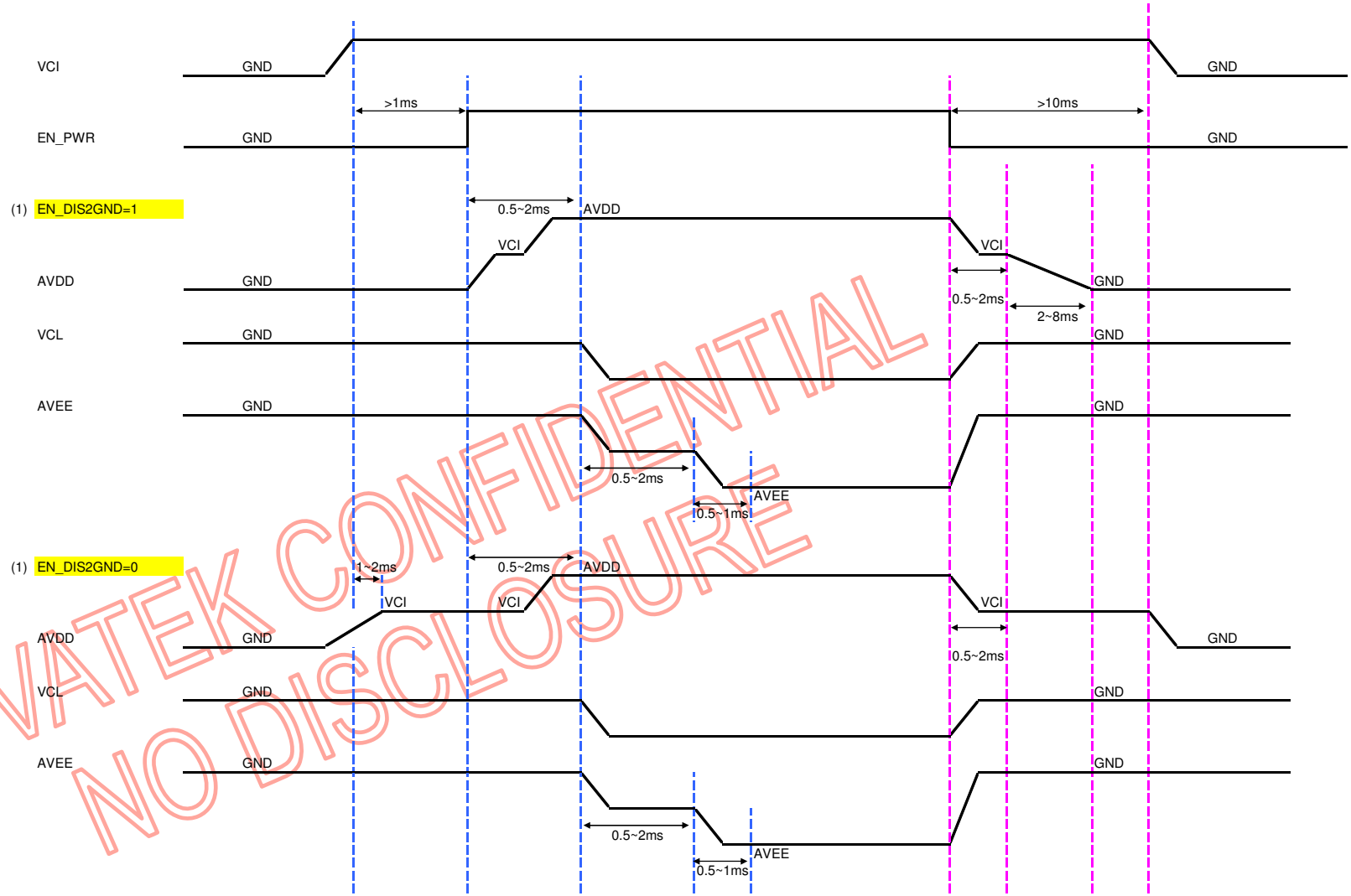
Case 3: EN_VCL = 0 and EN_VCL_FR = 0 (CP option):



Case 4: EN_VCL = 0 and EN_VCL_FR = 1 (CP option):



AVDD pre-charge to GND: control by EN_DIS2GND (CP option)



6.2：Positive Charge Pump Controller：

The NT50198 can provide a trimming-able pump ratio for AVDD. The ratio is adjusted 1.5x or 2.0x or 3.0x by CP option of VCI input voltage.

6.3：Negative Charge Pump Controller：

The NT50198 can provide a fixed pump ratio to generate AVEE. The ratio is fixed at -1.0x of AVDD.

6.4：Application Note：

The NT50198 has three control signals：EN_PWR / PSYNC / EN_VCL.

1. EN_PWR is used for enable AVDD and AVEE charge pump circuit. When EN_PWR keeps low, it will disable output voltage.
   Note: Please do not connect EN_PWR to VCI. Host should enable EN_PWR pin while VCI power is ready

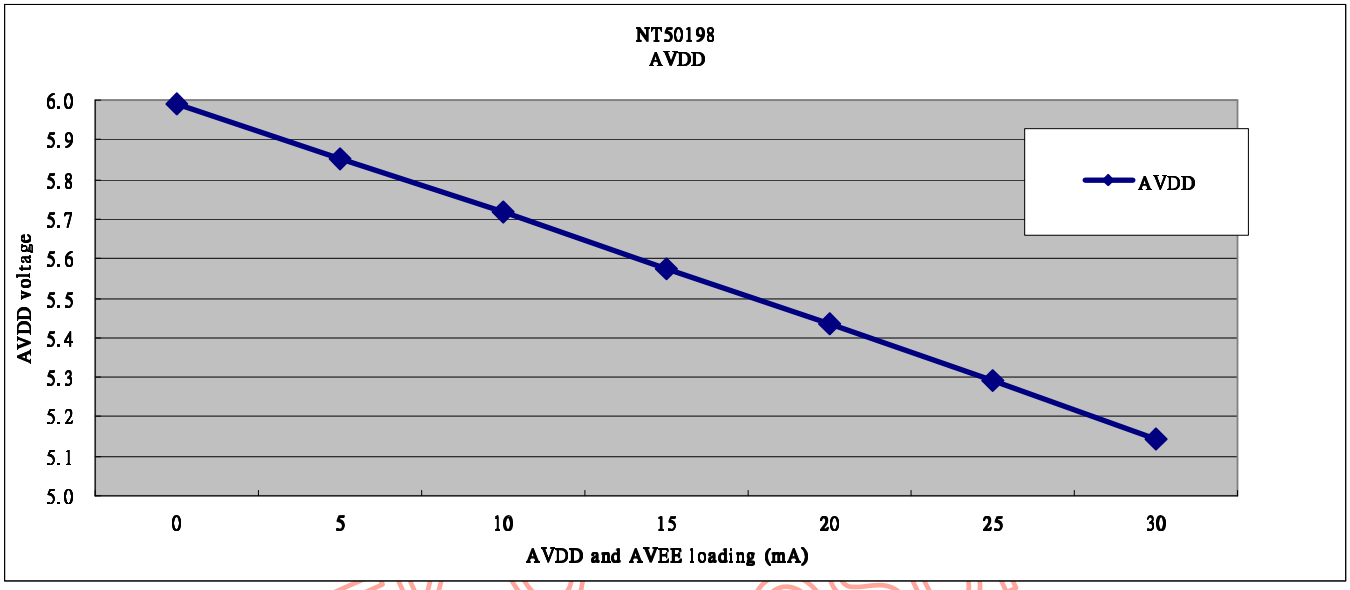
2. PSYNC is used for sync mode with VCL. If EN_VCL = 1 and EN_VCL_FR = 1 (optional pin), VCL enter free pumping mode for internal clock. It will start with EN_PWR pin. If EN_VCL = 1 and EN_PWR_VCL_FR = 0, VCL enter sync mode with PSYNC. In the beginning, VCL will not enable with EN_PWR pin. When PSYNC pin starts to toggle, VCL will pump and follow the frequency of PSYNC. When PSYNC stops toggling, VCL will wait two or more clock and discharge to ground.

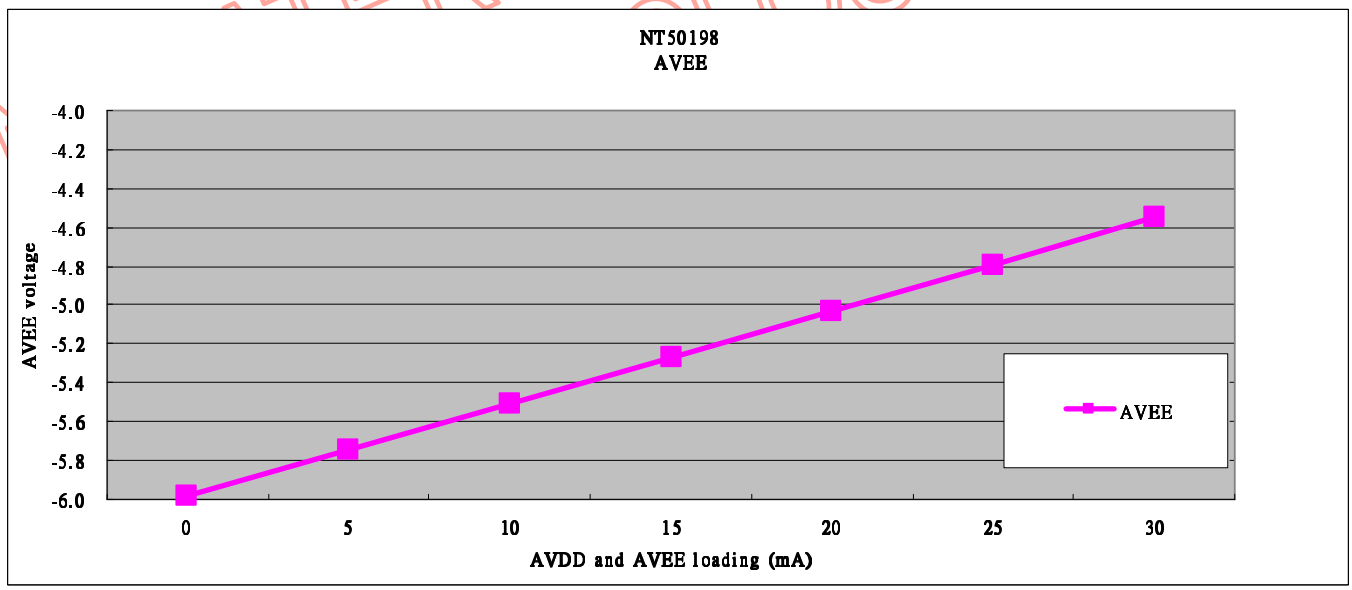
3. EN_VCL is used for enable VCL charge pump circuit. When EN_VCL keeps low, it will disable output voltage of VCL. EN_VCL can be connected to VCI for power-on start. (This function is available for 16 pins package only)

Protection function：Over voltage protection (clamp function) is included in NT50198.

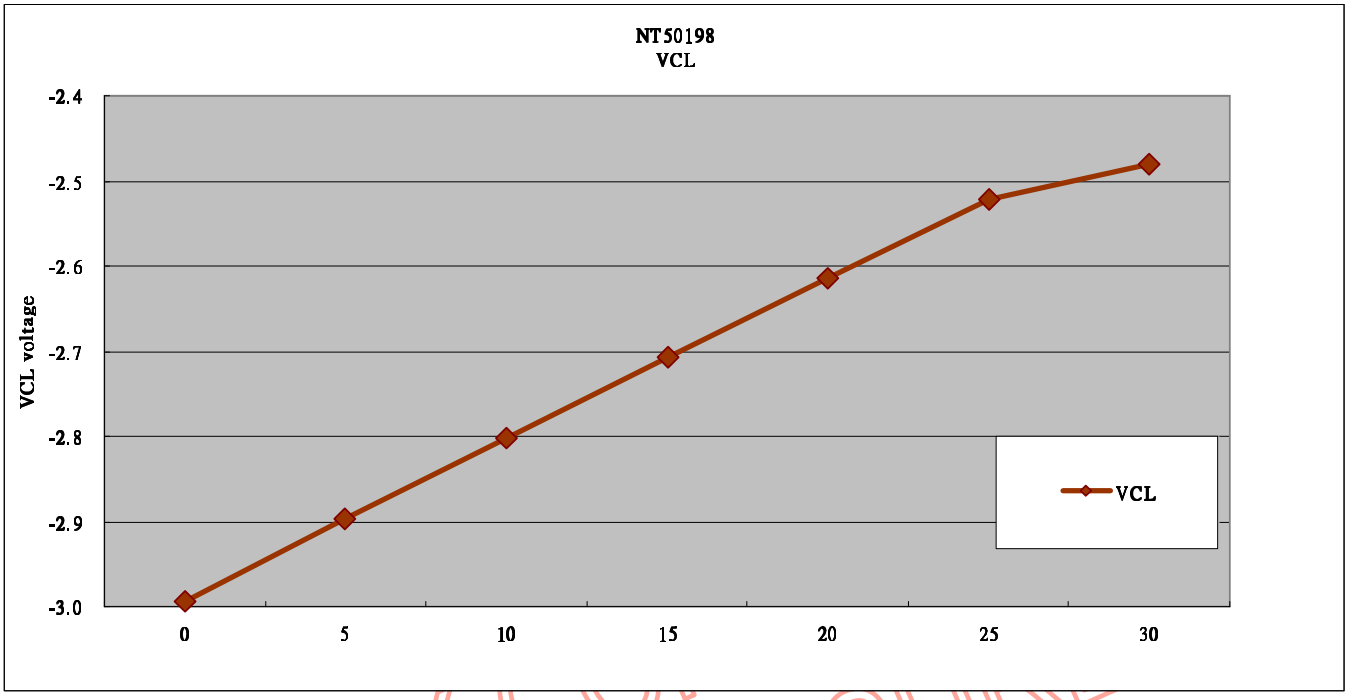
6.5：Typical characteristic:

6.5.1 Output voltage V.S. Output current with VCL (Vin = 3V , room temperature)

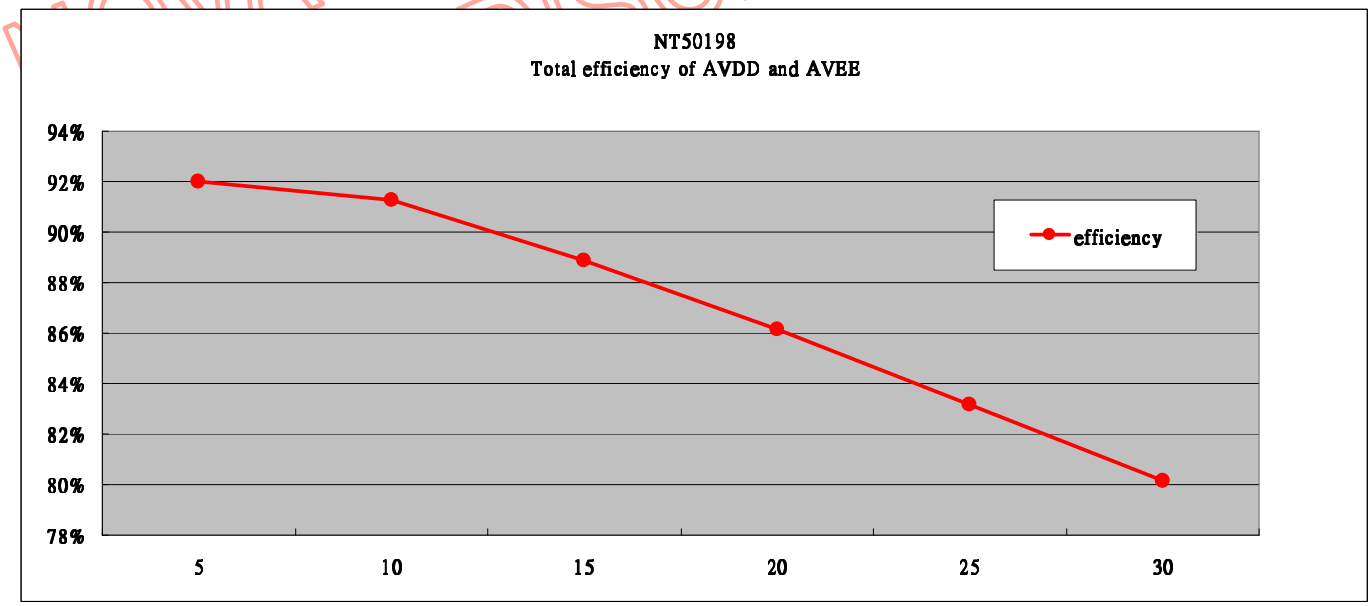




Note : It means when AVDD and AVEE output 20 mA at the same time ,
AVDD will drop to 5.435V and AVEE will drop to -5.03V .



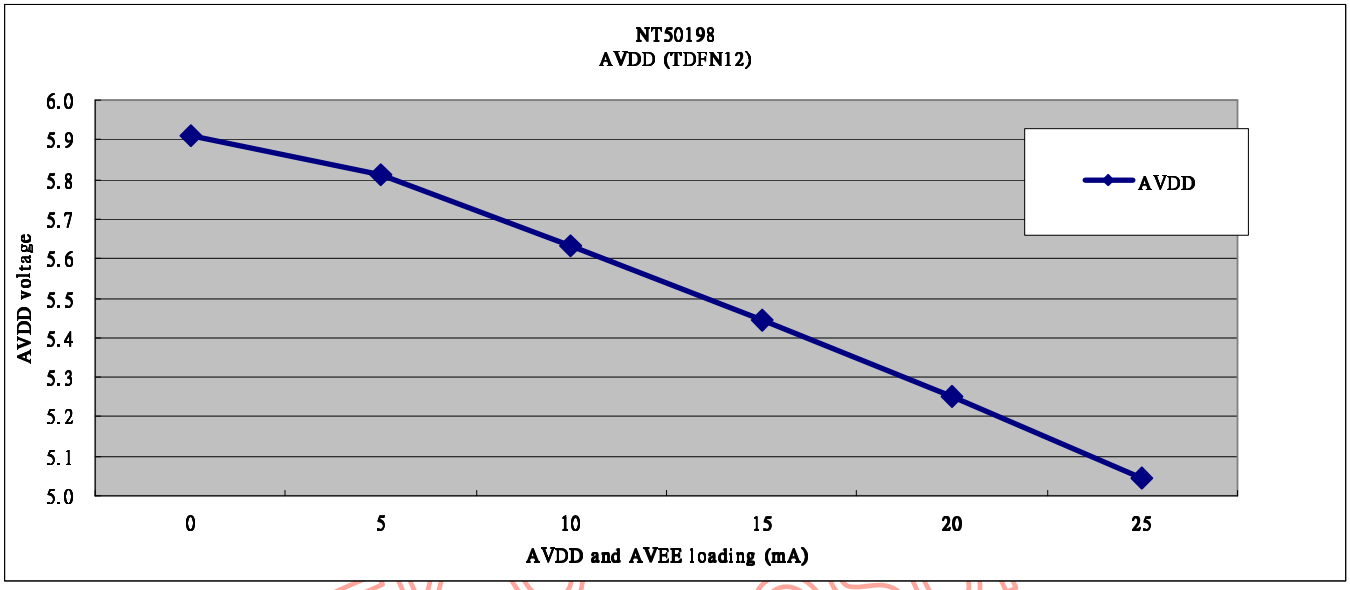
6.5.2 Efficiency V.S. output current with VCL(Vin = 3V , room temperature)

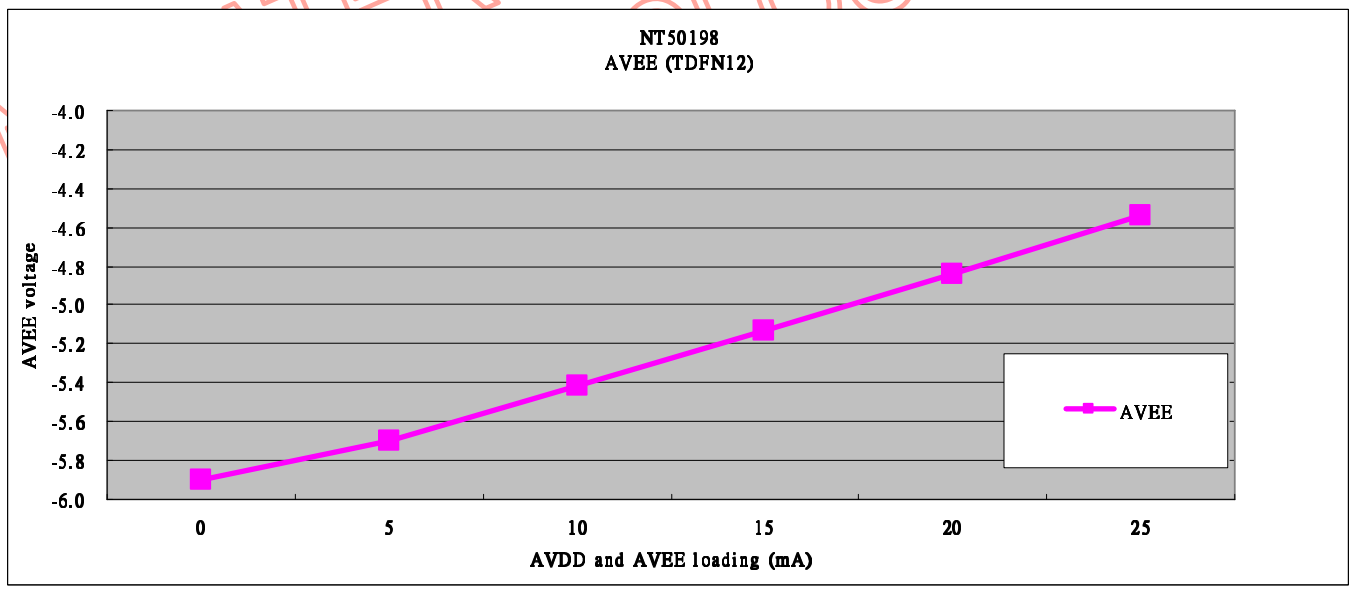


6.5.3 Output voltage V.S. Output current of without VCL (Vin = 3V , room temperature)

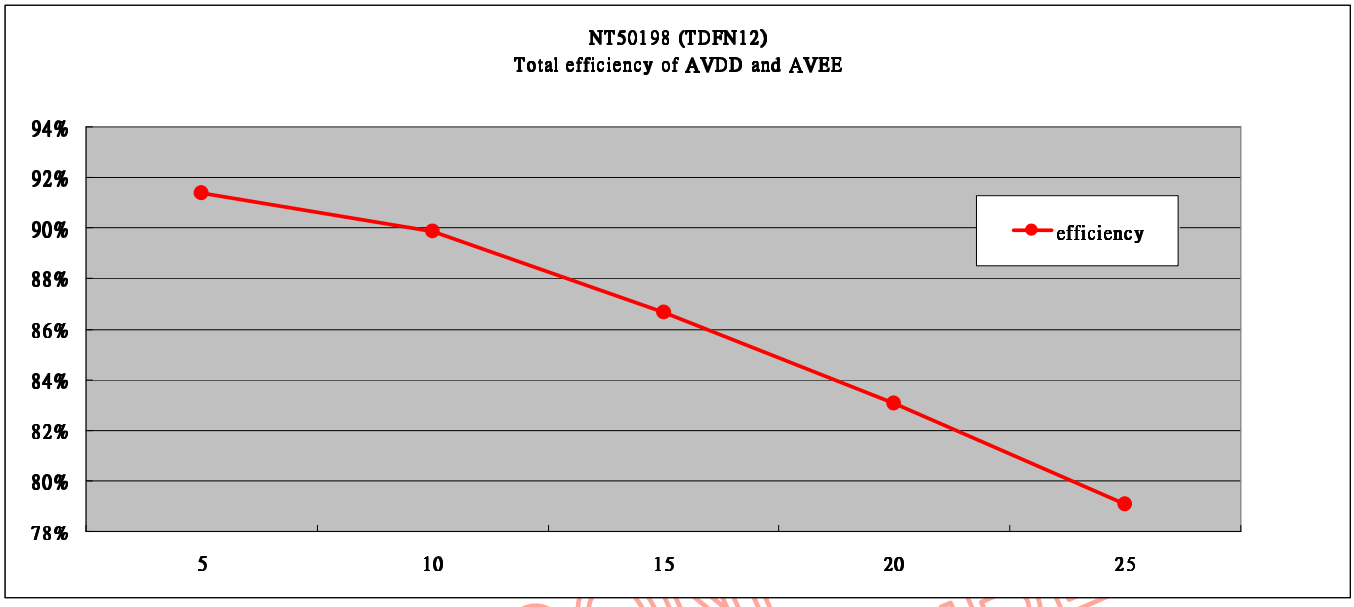
Note : if the capacitor of VCL(C31) does not assembly , it will degrade the AVDD output voltage level and pump efficiency .

the NT50198 behavior without VCL is showed as below , the same as TDFN12 .





6.5.4 Efficiency V.S. output current of without VCL (Vin = 3V , room temperature)



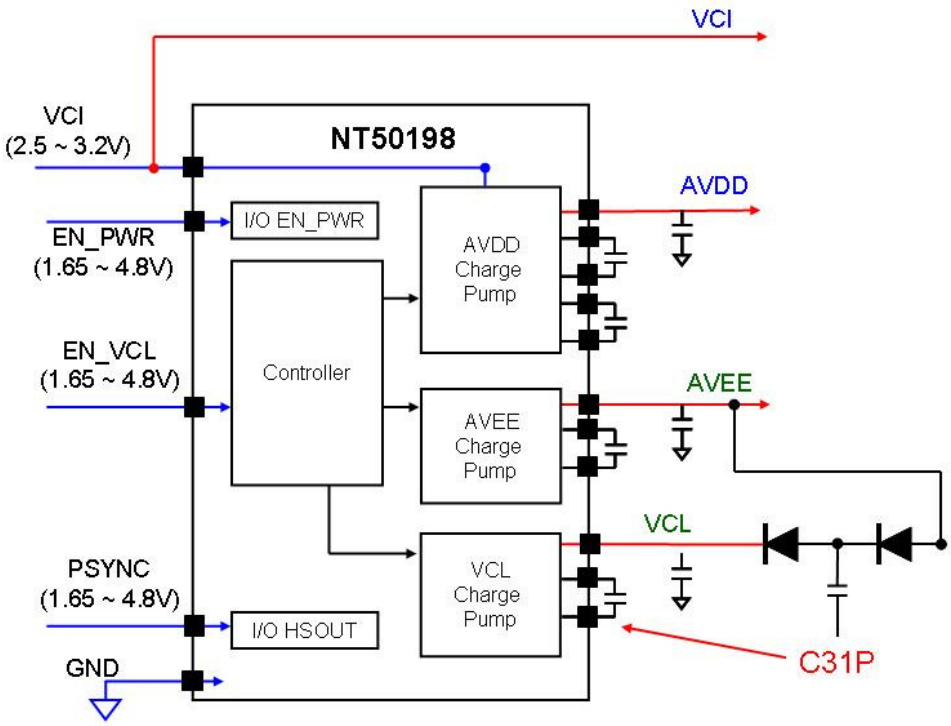
6.6：Two ways to enhance output current capability:

6.6.1: Dickson doubler circuit:

With heavy loading of AVDD and AVEE, NT50198 provide another option circuit to enhance AVEE circuit ability.

Using VCL voltage doubler to generate 2*VCL, and connect with AVEE output pin.

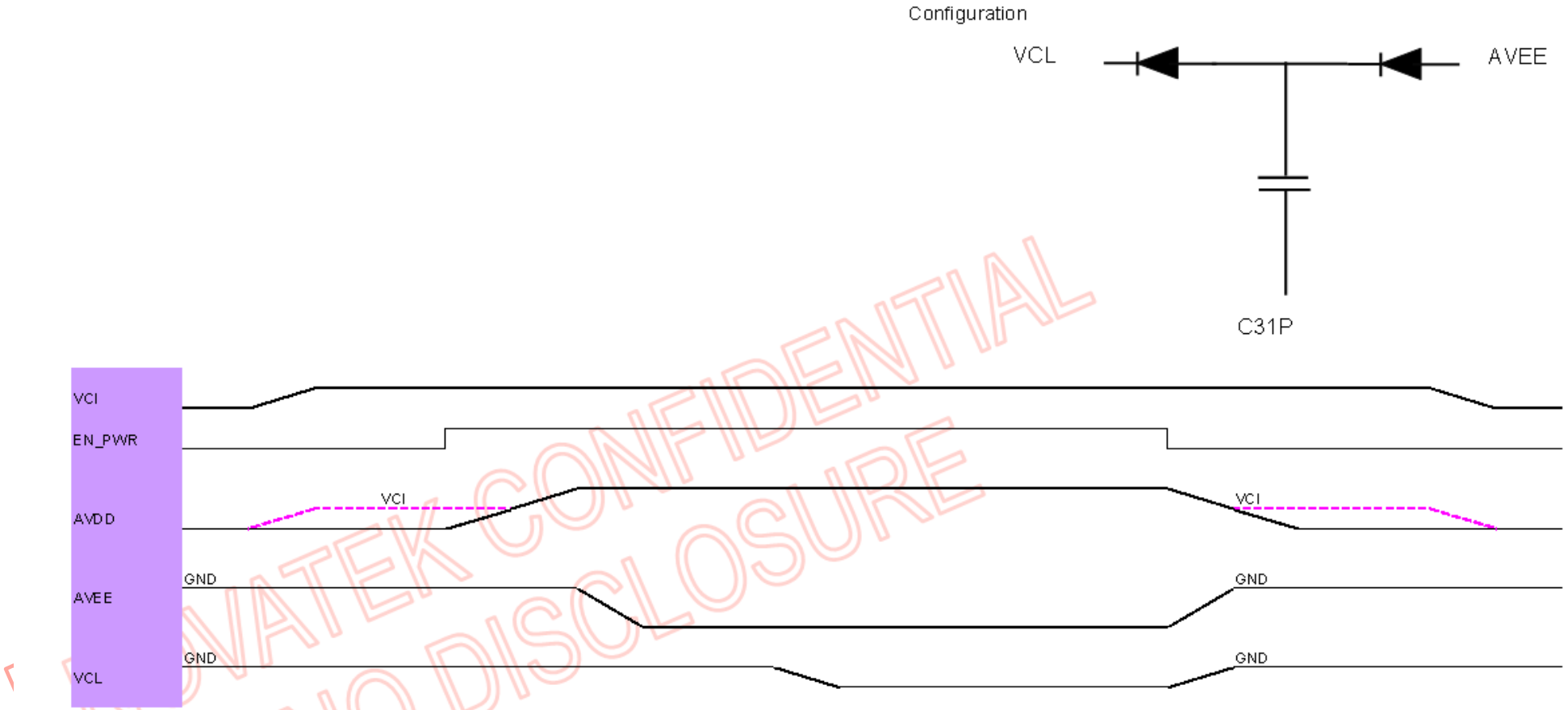
It needs to add 2 extra diodes, 1 capacitor and change AVEE capacitor from 2.2uF to 4.7uF and needs to be controlled by C31P signal. (Only available for 16 pin package IC)



6.6.2: External component table of Dickson doubler circuit:

Number	Pad Name	Connection	Typical Value
1	AVDD	Connect a capacitor (Max. 10V): AVDD -------| |-------- GND	2.2 uF
2	AVEE	Connect a capacitor (Max. 10V): AVEE--------| |-------- GND	2.2 uF
3	C11P/M	Connect a capacitor (Max. 10V): C11P -------| |-------- C11M	1.0 uF
4	C12P/M	Connect a capacitor (Max. 10V): C12P -------| |-------- C12M	1.0 uF
5	C21P/M	Connect a capacitor (Max. 10V): C21P--------| |-------- C21M	1.0 uF
6	VCL	Connect a capacitor (Max. 10V): VCL----------| |-------- GND	2.2 uF
7	C31P/M	Connect a capacitor (Max. 10V): C31P--------| |-------- C31M	1.0 uF
8	VCI (option)	Connect a capacitor (Max. 10V): VCI--------| |-------- GND	2.2 uF
9	C31P	Connect a capacitor (Max. 10V): C31P--------| |-------- Dickson	1.0 uF
10	DIODE	Connect a Schottky diode: AVEE -------►|------ Dickson	VF < 0.4V at 20mA, VR ≥ 30V
11	DIODE	Connect a Schottky diode: Dickson -------►|------ VCL	VF < 0.4V at 20mA, VR ≥ 30V

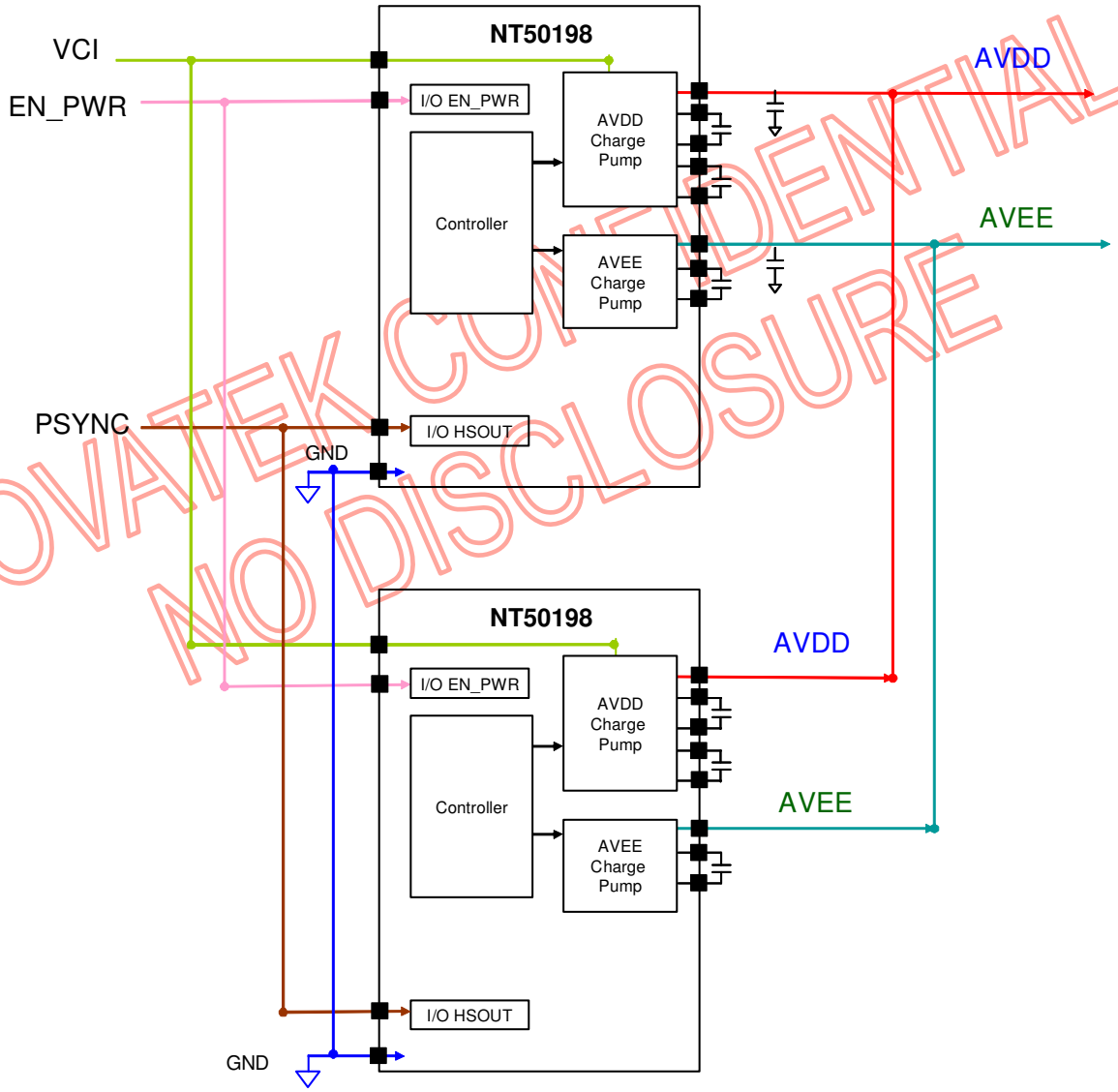
6.6.3: Power On / off sequence with external Dickson mode:



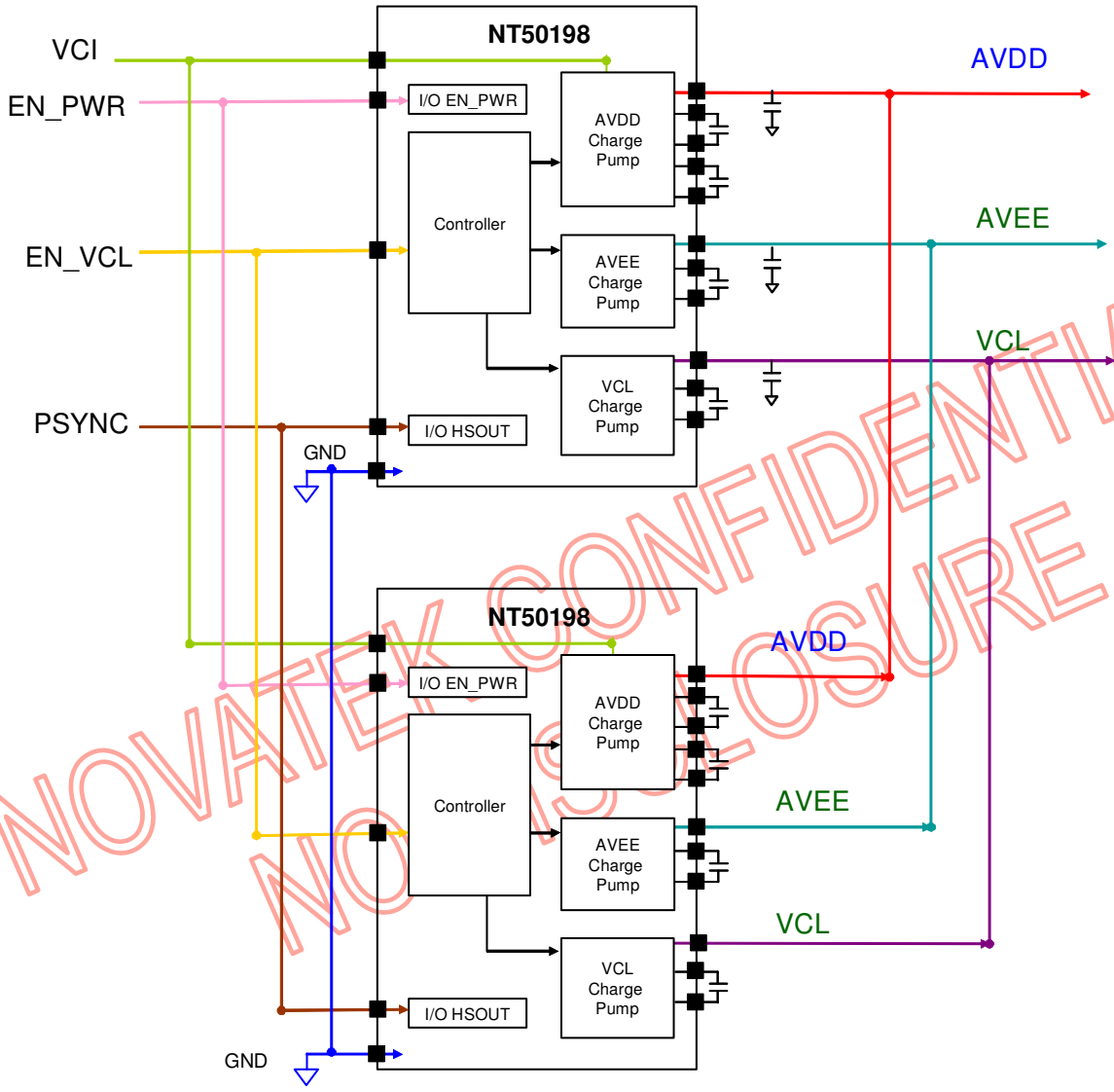
Note : please notice the power on sequence of VCL , it must enable after AVEE , please contact with us for correct NT50198 part number .

6.6.4: Paralleling two device circuit:

An increase in converter output current capability with a reduction in output resistance can be obtained by paralleling two devices. The output current capability is approximately equal to double for AVDD and AVEE. A single shared output capacitor is sufficient for proper operation but each device does require its own pump capacitor. Note that the output ripple frequency will be complex since the oscillators are not synchronized.



<TDFN 12pin application circuit>



<TDFN 16pin application circuit>
<QFN 16pin application circuit>

6.6.5: External component of Paralleling two device circuit:

Number	Pad Name	Connection	Typical Value
1	AVDD	Connect a capacitor (Max. 10V): AVDD -------| |-------- GND	2.2 uF
2	AVEE	Connect a capacitor (Max. 10V): AVEE--------| |-------- GND	2.2 uF
3	C11P/M for First IC	Connect a capacitor (Max. 10V): C11P -------| |-------- C11M	1.0 uF
4	C12P/M for First IC	Connect a capacitor (Max. 10V): C12P -------| |-------- C12M	1.0 uF
5	C21P/M for First IC	Connect a capacitor (Max. 10V): C21P--------| |-------- C21M	1.0 uF
6	VCI (option)	Connect a capacitor (Max. 10V): VCI--------| |-------- GND	2.2 uF
7	C11P/M for Second IC	Connect a capacitor (Max. 10V): C11P -------| |-------- C11M	1.0 uF
8	C12P/M for Second IC	Connect a capacitor (Max. 10V): C12P -------| |-------- C12M	1.0 uF
9	C21P/M for Second IC	Connect a capacitor (Max. 10V): C21P--------| |-------- C21M	1.0 uF

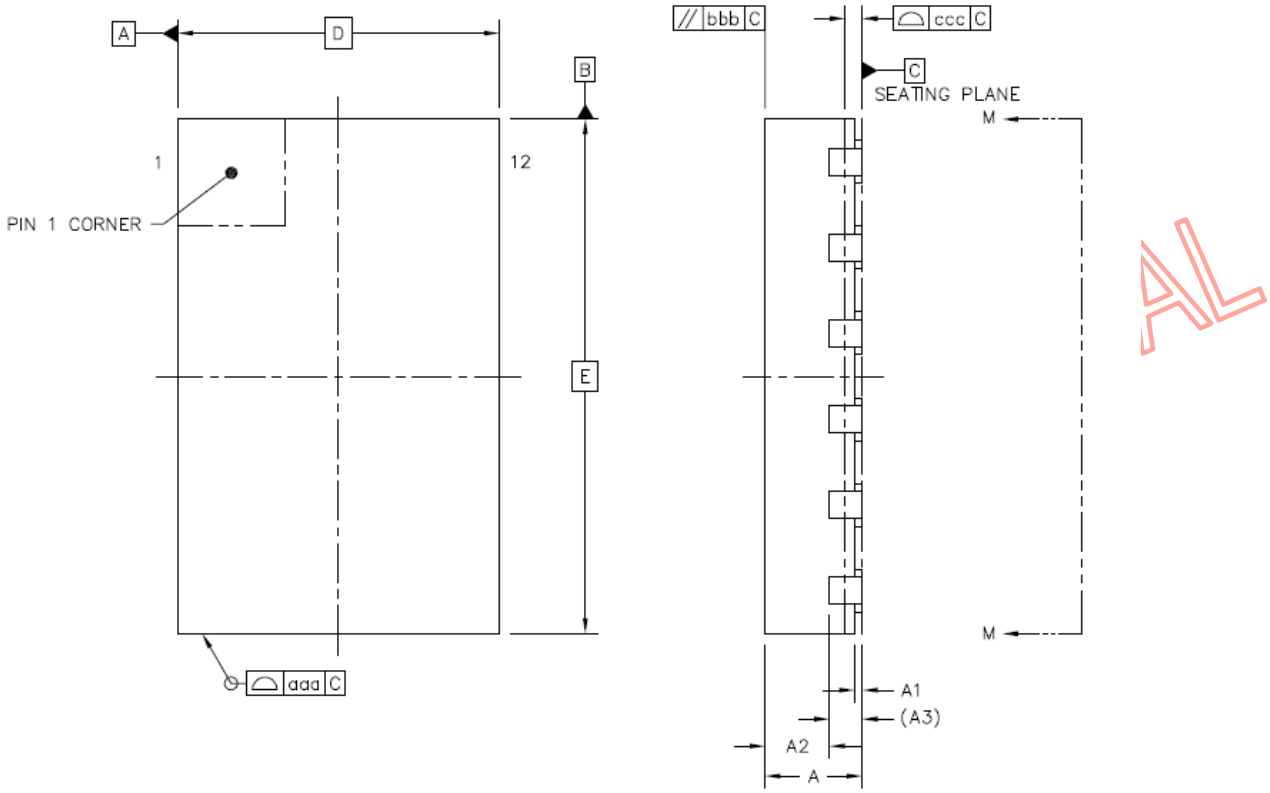
<12pin external component table>

Number	Pad Name	Connection	Typical Value
1	AVDD	Connect a capacitor (Max. 10V): AVDD -------| |-------- GND	2.2 uF
2	AVEE	Connect a capacitor (Max. 10V): AVEE--------| |-------- GND	2.2 uF
3	C11P/M for First IC	Connect a capacitor (Max. 10V): C11P -------| |-------- C11M	1.0 uF
4	C12P/M for First IC	Connect a capacitor (Max. 10V): C12P -------| |-------- C12M	1.0 uF
5	C21P/M for First IC	Connect a capacitor (Max. 10V): C21P--------| |-------- C21M	1.0 uF
6	VCL	Connect a capacitor (Max. 10V): VCL----------| |-------- GND	2.2 uF
7	C31P/M for First IC	Connect a capacitor (Max. 10V): C31P--------| |-------- C31M	1.0 uF
8	VCI (option)	Connect a capacitor (Max. 10V): VCI--------| |-------- GND	2.2 uF
9	C11P/M for Second IC	Connect a capacitor (Max. 10V): C11P -------| |-------- C11M	1.0 uF
10	C12P/M for Second IC	Connect a capacitor (Max. 10V): C12P -------| |-------- C12M	1.0 uF
11	C21P/M for Second IC	Connect a capacitor (Max. 10V): C21P--------| |-------- C21M	1.0 uF
12	C31P/M for Second IC	Connect a capacitor (Max. 10V): C31P--------| |-------- C31M	1.0 uF

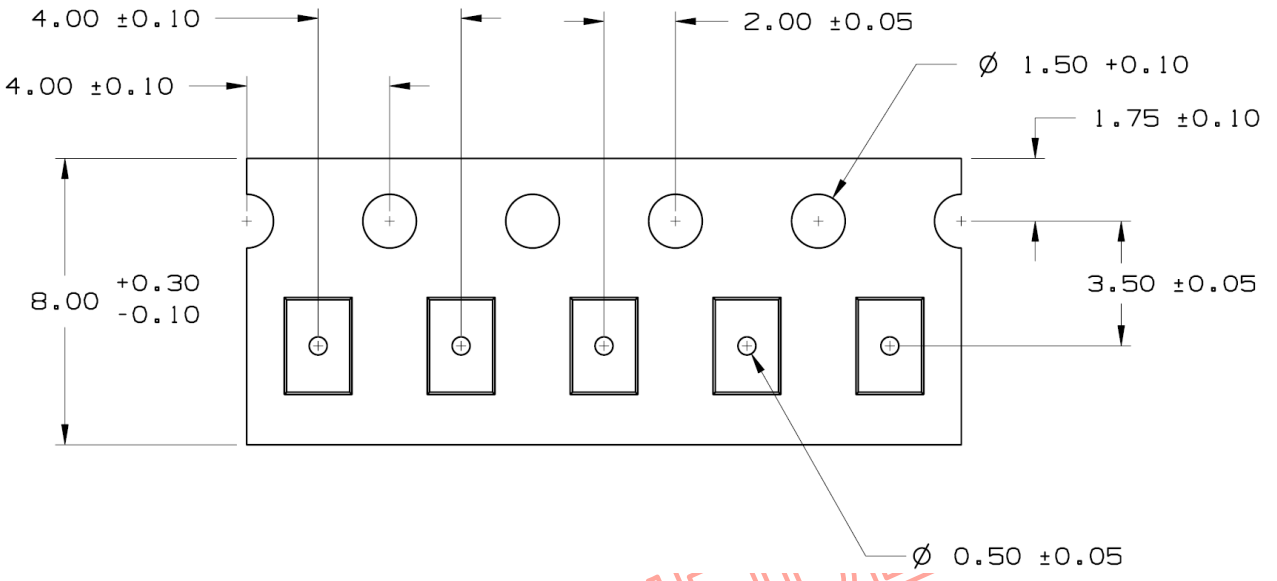
<16pin external component table>

7. Package Information：

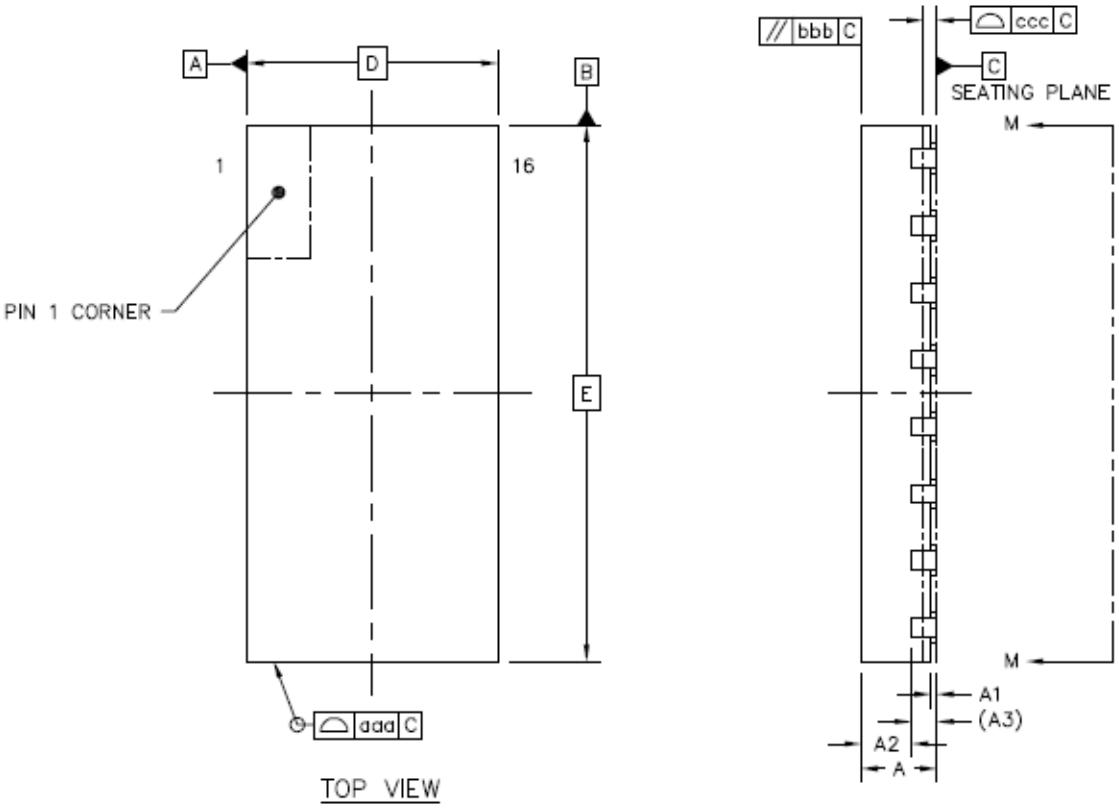
7.1 TDFN-12 pins package

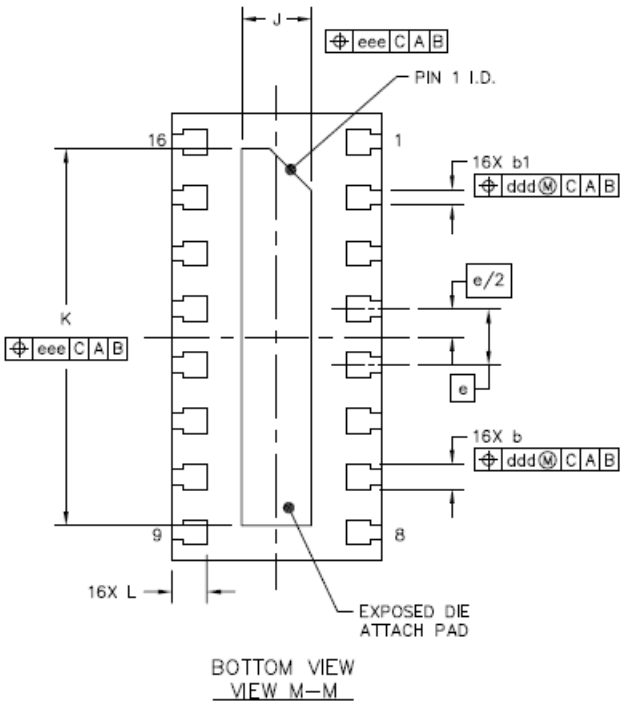


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.4	0.45	0.5
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.3	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.2	0.25
		b1	0.075	0.125	0.175
BODY SIZE	X	D		1.5 BSC	
	Y	E		2.4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	0.4	0.5	0.6
	Y	K	1.7	1.8	1.9
LEAD LENGTH		L	0.2	0.25	0.3
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

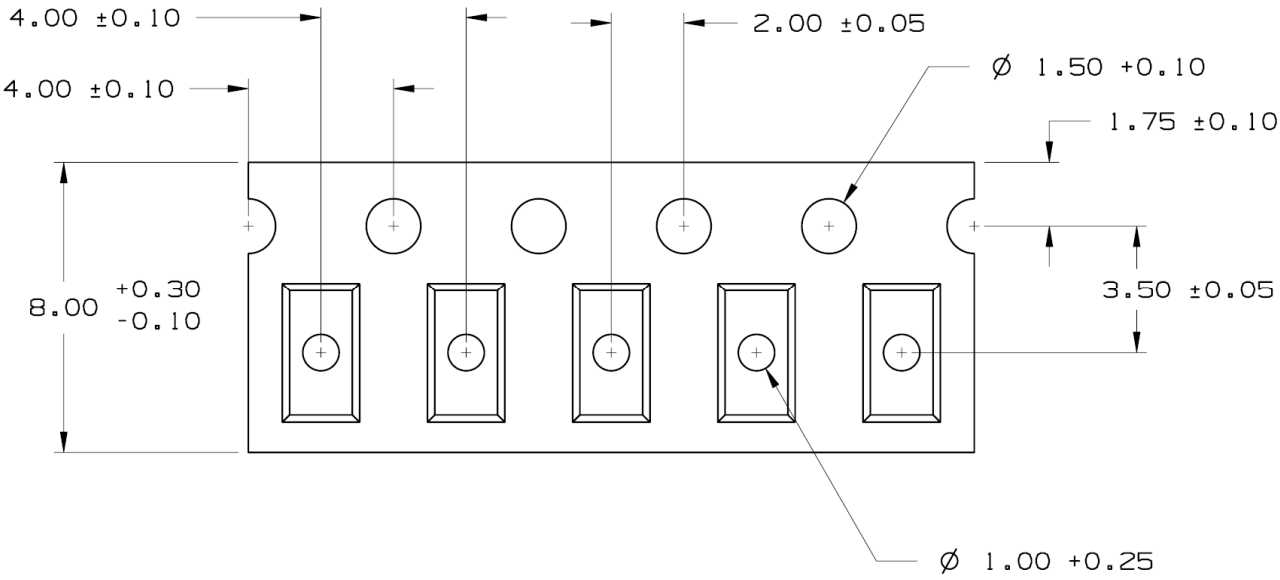


7.2 TDFN-16 pins package

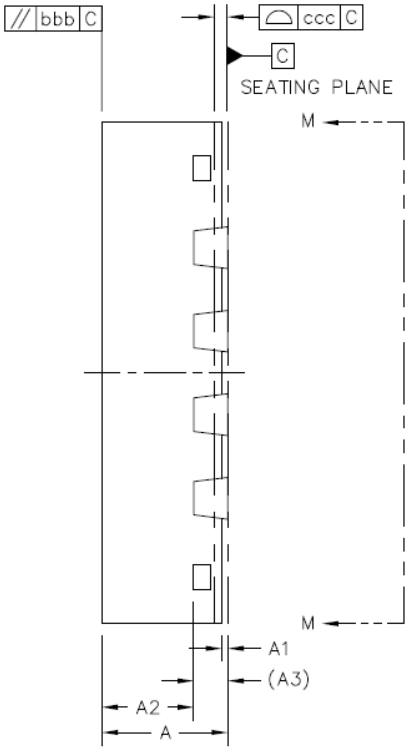




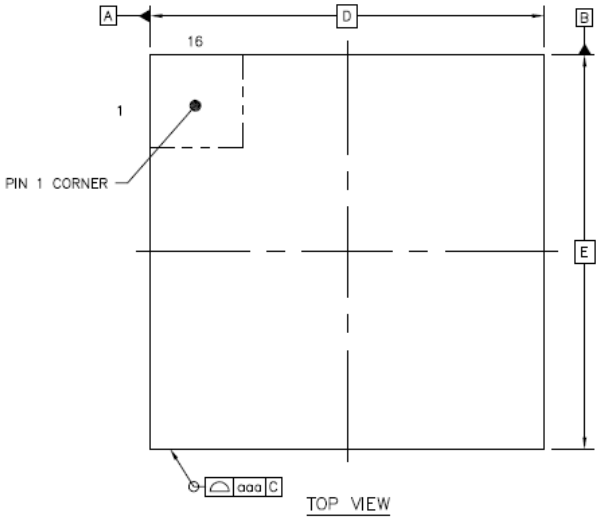
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.4	0.45	0.5
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.3	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
		b1	0.06	0.11	0.16
BODY SIZE	X	D		1.5 BSC	
	Y	E		3.2 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	0.4	0.5	0.6
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.2	0.25	0.3
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

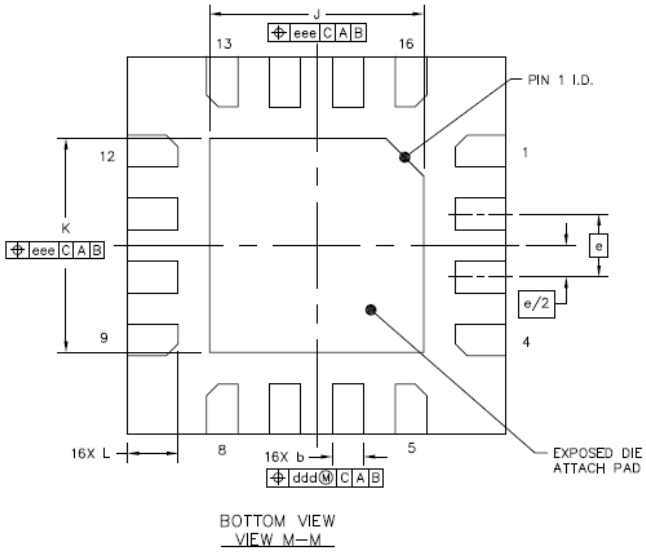


7.3 QFN-16 pins package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	1.6	1.7	1.8
	Y	K	1.6	1.7	1.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	





8. Absolute Maximum Ratings：

Parameter	Symbol	Value	Unit
Supply voltage	VCI	-0.3~6	V
Control signals output current (charge pump clock for fly caps)	Output current	TBD	mA
Control signals voltage range (EN_PWR , EN_VCL , PSYNC)	Logic input	-0.3~6	V
Output control driver	Output voltage AVDD	0~6	V
	Output voltage AVEE	0~-6	
	Output voltage VCL	0~-3	

9. Thermal Information：

Parameter	Symbol	Spec			Units
		Min	Typical	Max	
Operating junction temperature	T_J	TBD	-	TBD	℃
Operating temperature range	T_{OP}	-40	-	85	℃
Storage temperature range	T_{STG}	-65	-	160	℃
Lead soldering temperature , 10 second	-	-	-	260	℃

10. Electrical Specifications：

Parameter	Symbol	Condition	Spec			Units
			Min	Typical	Max	
Input power supply						
Supply voltage	VCI	-	2.5		4.8	V
Supply current	I_VCI	-			150	mA
Output Power Supply						
Positive output voltage	AVDD	Input = 3V			6.0	V
Negative output voltage	AVEE	Input = 3V			-6.0	V
Positive output current	I_AVDD	Input = 3V			30	mA
Negative output current	I_AVEE	Input = 3V			30	mA
Negative output current	I_VCL	Input = 3V			30	mA
Control Signal Voltage Level						
Input high voltage	V_{IH}	-	1.1	-	VCI	V
Input low voltage	V_{IL}	-	0	-	0.3	V
Output Power Supply						
Output / Input	Efficiency	-				%