NOVATEK
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Data Sheet

NT51021

1803CH Source Driver with TCON

MIPI Interface with GIP function

V0.9

Preliminary Spec

Revise History

Version	Content	PAGE	Date
0.0	New Spec.	-	2013/04/30
0.1	Correct for non supporting BTA function. Remove 3-wire interface. Correct STBYB control descriptions Update I2C communication method Update itmes of Features Update application block diagram Update pin descriptions Update Chip Outline Dimensions Update pad coordinate	58~ 14, 27~, 50 18 27,28 6 8 11~15 58 59	2013/07/15
0.2	Update "The relationship between Pin and Register" tables. Update "The Route of Panel and Driving Method" diagrams. Update pin descriptions Update power on/off sequence Update chip outline dimension Update pad sequence	17 40~41 11~15 36 6, 58 10	2013/8/2
0.3	Update Pad Sequence/ Pad Coordinate Update chip outline dimension Append V_{IH3}/V_{IL3} for I2C input interface Append total bump area Update Power On/Off Seqneuce Update MIPI / I2C register table Update register descriptions Update Pin Descriptions	10, 59~75 58 46 58 37,38 25,28 30~37 11~17	2013/8/21
0.4	Revise I2C Register Address mapping.	28,29~37	2013/8/23
0.5	Correct register R89H description Update application block diagram Append RTERM[1:0] pin description Feature update for not support BTA function Revise I2C_SDA not in use Remove CABC register control. Adjust statement Update digital output timing table Update MIPI register tables Update input timing tables	31 8 17,12,18 6 13 18,29,32 42, 46~48 57 26, 29, 30 44,45	2013/9/6
0.6	Append note for I2C read/write operation Correct data of item E Update wiring resistance table Append R8CH control register Correct bump Y-size of Pad No.1~377. Correct figure "Chip Outline Dimensions"	28 59 17 26,29,31 60~62 59	2013/11/11
0.7	Update table of "MIPI Interface DC characteristic". (V_{OD}, V_{IDTH}, V_{IDTL}) Revise table of "Data-Clock Timing Specifications". (T_{SKEW}, T_{SETUP}, T_{HOLD}, t_R / t_F) Correct typo of register R93H. Append limit of V1 minimun setting value. Update input timing table	48 51 33 28 44,45	2013/12/6
0.8	Update V1/V14 register default value Revise title of lists Update input timing table Append V1/V4/V7/V8/V11/V14 , AGND1, INVSEL[1:0] pin description Update VQH/L, VGH_R/L pin description	38 36,37 44,45 14~17 14~17	2013/12/31
0.9	Update AGND1 pin in table of pad coordinate Update V4/V11 wiring resistance Revise HS(Horizontal Sync) to Hsync, VS to Vsync. Append GIPIO driving/sink ability	60~ 17 44,45 47	2014/1/3

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1. Features

- **Special design for middle size TFT LCD Panel with MIPI interface**
- **The chip Integrate 1803 channel source driver and timing controller**
- **Support panel resolution (HxV) :**
  1200(RGB)x1920, 600(RGB)x1024, 1080(RGB)x1920, 1200(RGB)x1600
- **8-bit resolution 256 gray-scale**
- **Operating frequency: MIPI: 1Gbps/Lane (Max.)**
- **Support 2, 3 or 4 data lanes for MIPI interface**
- **Power for digital circuit(VCC/VCC_IF): 1.4V ~ 1.6V**
- **Power for digital circuit(VDD): 2.7V ~ 3.6V**
- **Power for analog circuit(AVDD): 7.0 ~ 10.0V**
- **Support RGB independent gamma correction function**
- **Support CABC function**
- **Support Color Enhancement function**
- **Support Advance BIST function**
- **Support Zig-Zag driving method**
- **Support GIP function**
- **Not support MIPI BTA function**
- **COG package**
- **Chip size = 28500 um x 775 um**
- **Output bump pitch = 12 um**

2. General Description

The NT51021 integrats 1803 source channels, a timing controller, and GIP control circuits for color TFT LCD panel with normal or GIP panel structure. The chip without frame memory and support MIPI interface.

The NT51021 is a highly integrated solution for small size to middle size TFT LCD panels. The chip is special designed for low cost portable product application.

3. Function Block Diagram

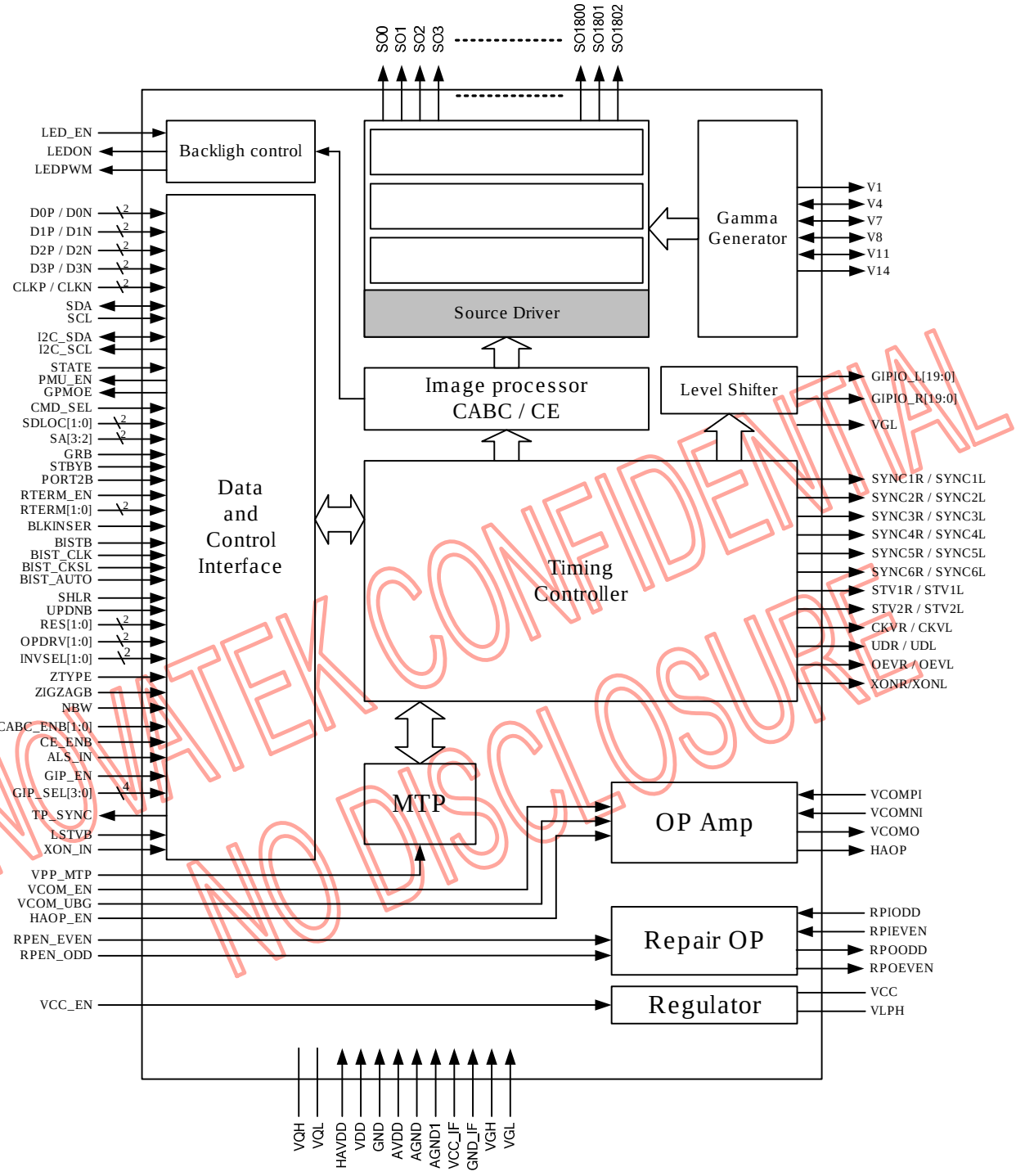


Figure 1. System Function Block Diagram

4. Application Block Diagram

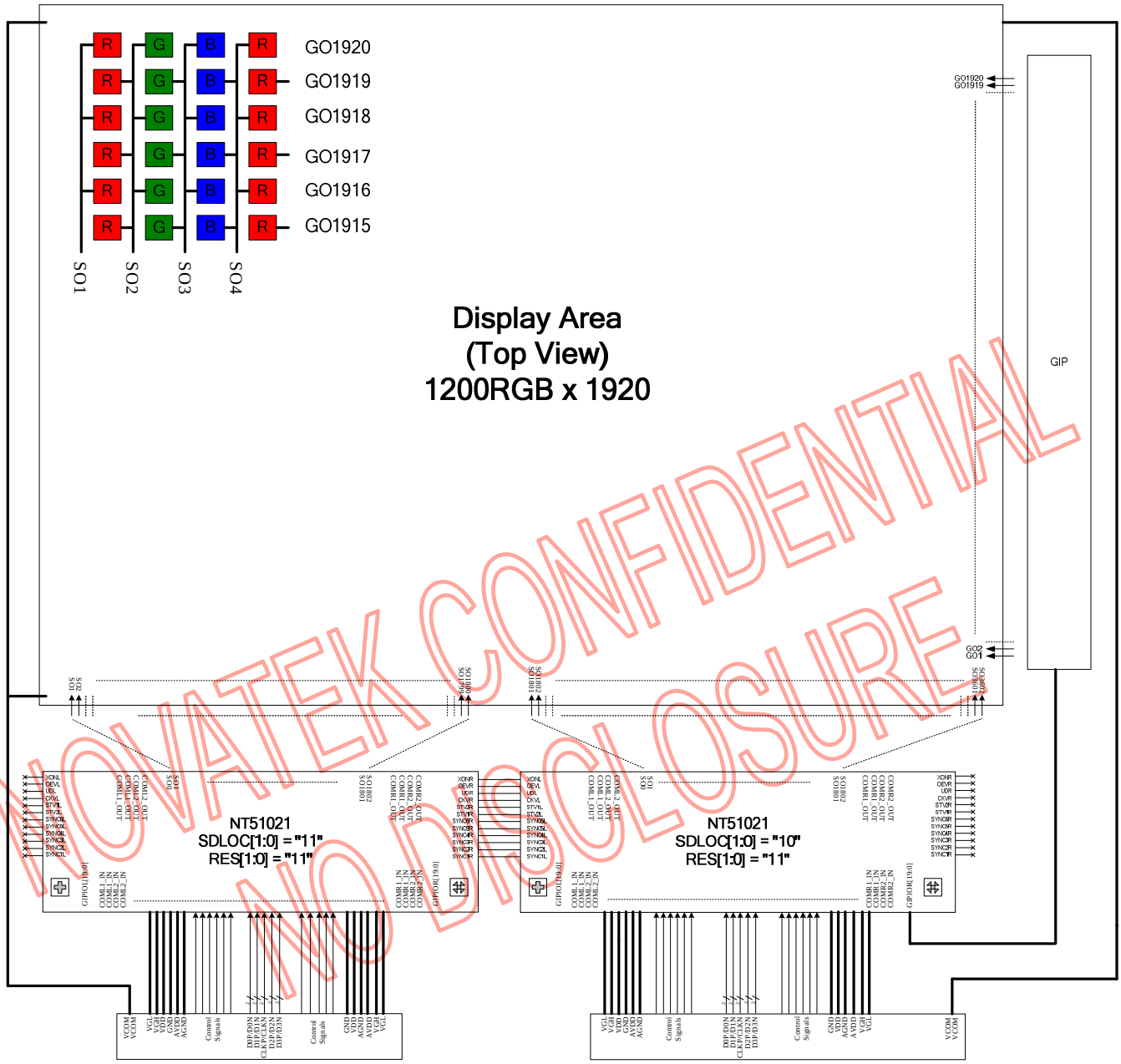


Figure 2. Application block diagram for WUXGA GIP panel

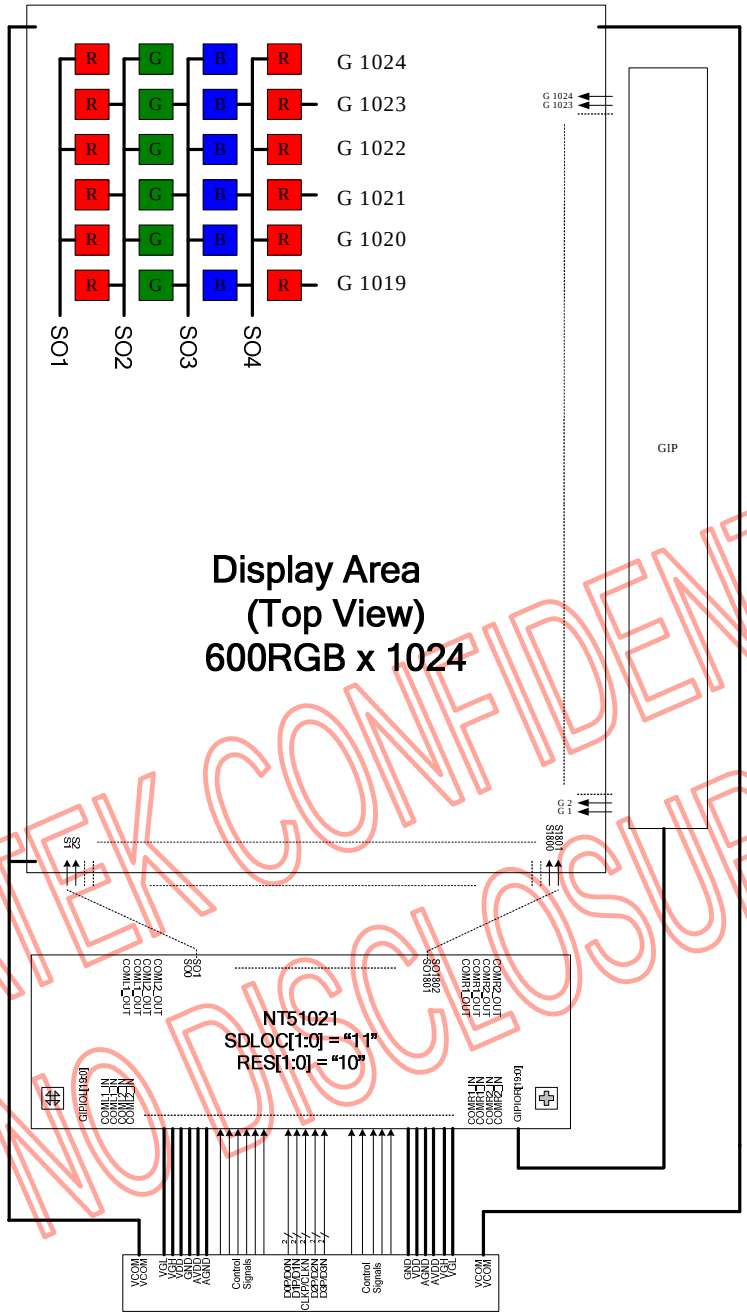


Figure 3. Application block diagram with WSVGA Gate Driver IC

5. Pad Sequence (Bump Side)

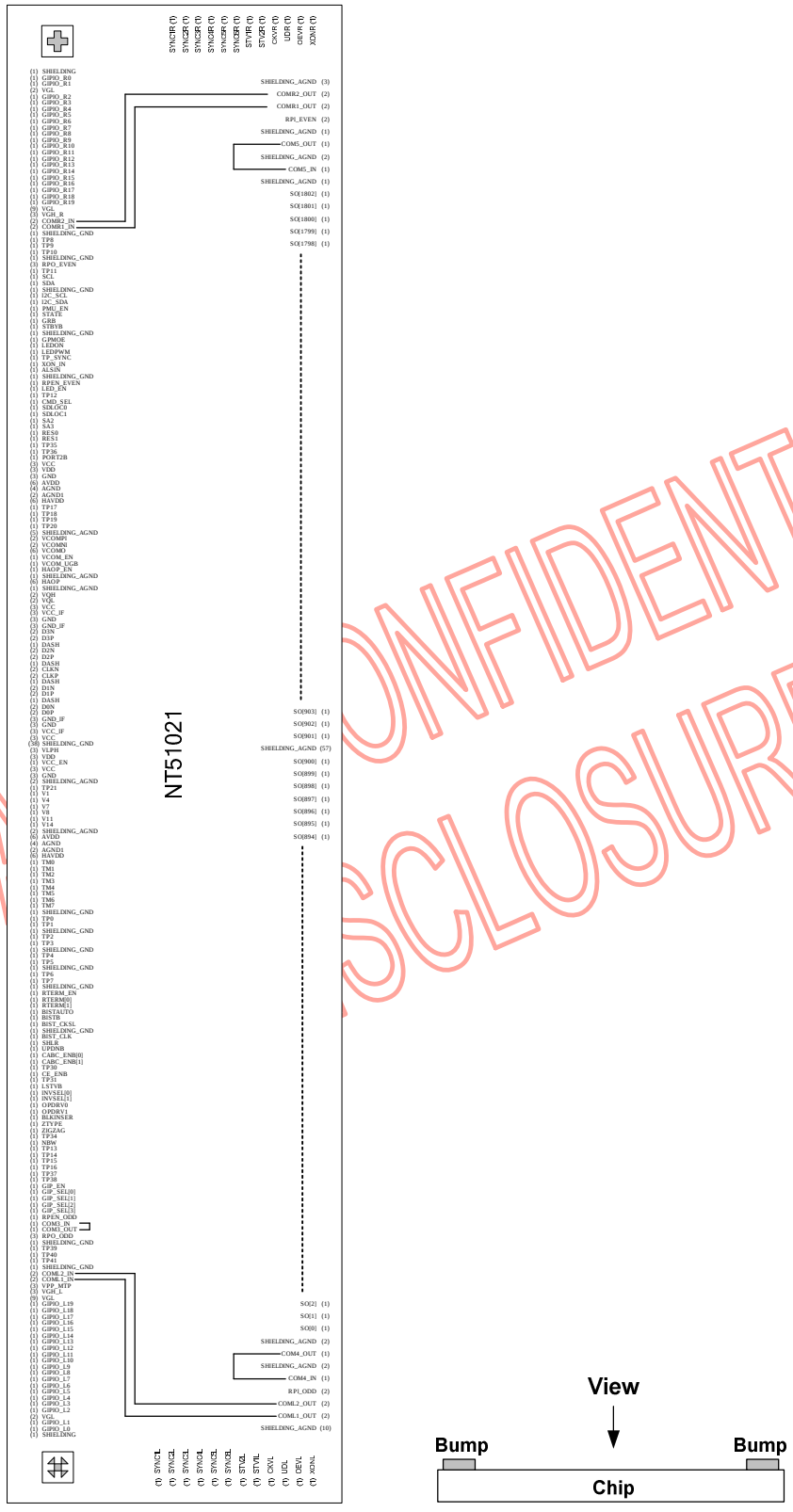


Figure 4. Pad Sequence

6. Pin Descriptions

Table 1. Pin Descriptions

<table>
<tr><th>Designation (Domain)</th><th>I/O</th><th>Description</th></tr>
<tr><td>D0P/D0N
D1P/D1N
D2P/D2N
D3P/D3N
(VCC_IF)</td><td>I</td><td>MIPI data input pins
Please set to VCC_IF voltage level if pin is NOT in use.</td></tr>
<tr><td>CLKP/CLKN
(VCC_IF)</td><td>I</td><td>MIPI clock input pins.</td></tr>
<tr><td>SHLR
(VCC)</td><td>I</td><td>Source Right or Left sequence control. Normally pull high
SHLR = "L", shift left: last data = S1←S2←S3..... ←S1800 = first data.
SHLR = "H", shift right: first data = S1→S2→S3..... →S1800 = last data.(Default)</td></tr>
<tr><td>UPDNB
(VCC)</td><td>I</td><td>Griver Up or Down sequence control. Normally pull high.
UPDNB = "L", STV1 pin output vertical start pulse and UD pin output logical "1".
UPDNB = "H", STV2 pin output vertical start pulse and UD pin output logical "0".(Default)</td></tr>
<tr><td>ZIGZAG
(VCC)</td><td>I</td><td>Zig-zag driving method setting. Normally pull high.
ZIGZAG = "L", Normal driving method.
ZIGZAG = "H", Zig-Zag driving method. (Default)</td></tr>
<tr><td>ZTYPE
(VCC)</td><td>I</td><td>Zig-Zag panel layout type selection. Normally pull high.
ZTYPE = "L", Zig-Zag layout type0.
ZTYPE = "H", Zig-Zag layout type1.(Default)</td></tr>
<tr><td>RES[1:0]
(VCC)</td><td>I</td><td>Display resolution selection
<table>
<tr><th>RES[1]</th><th>RES[0]</th><th>Resolution</th><th>Disable channels</th></tr>
<tr><td>L</td><td>L</td><td>1200(RGB)x1600</td><td>No disable channel</td></tr>
<tr><td>L</td><td>H</td><td>1080(RGB)x1920</td><td>811~990</td></tr>
<tr><td>H</td><td>L</td><td>600(RGB)x1024</td><td>No disable channel</td></tr>
<tr><td>H</td><td>H</td><td>1200(RGB)x1920</td><td>No disable channel (Default)</td></tr>
</table></td></tr>
<tr><td>GRB
(VDD)</td><td>I</td><td>Global reset pin. Normally pull high.
GRB = "L", The controller is in reset state.
GRB = "H", Normal operation.(Default)
Suggest to connecting with an RC reset circuit (10Kohm, 1uF) for stability.</td></tr>
<tr><td>STBYB
(VDD)</td><td>I</td><td>Standby mode, Normally pull high.
STBYB = "L", timing controller, and source driver will turn off, all output are High-Z
STBYB = "H", normal operation. (Default)</td></tr>
<tr><td>PORT2B
(VCC)</td><td>I</td><td>One/Tow port interface selection. Normally pull high.
PORT2B = "L", Two port interface.
PORT2B = "H", One port interface.(Default)</td></tr>
<tr><td>SDLOC[1:0]
(VCC)</td><td>I</td><td>Source driver location definition pin. Normally pull high. (for Pin Control only)
<table>
<tr><th>SDLOC[1]</th><th>SDLOC[0]</th><th>Location</th></tr>
<tr><td>L</td><td>L</td><td>Source driver location on #4</td></tr>
<tr><td>L</td><td>H</td><td>Source driver location on #3</td></tr>
<tr><td>H</td><td>L</td><td>Source driver location on #2</td></tr>
<tr><td>H</td><td>H</td><td>Source driver location on #1(Default)</td></tr>
</table></td></tr>
<tr><td>SA[3:2]
(VCC)</td><td>I</td><td>The I2C Slave Address selection. Normally pull high. (for Pin Control only)
<table>
<tr><th>SA[3]</th><th>SA[2]</th><th>Location</th></tr>
<tr><td>L</td><td>L</td><td>SA[6:0]=110_00XX</td></tr>
<tr><td>L</td><td>H</td><td>SA[6:0]=110_01XX</td></tr>
<tr><td>H</td><td>L</td><td>SA[6:0]=110_10XX</td></tr>
<tr><td>H</td><td>H</td><td>SA[6:0]=110_11XX (Default)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Designation (Domain)</th><th>I/O</th><th>Description</th></tr>
<tr><td>BLKINSER
(VCC)</td><td>I</td><td>Black insertion control. Normally pull high.
BLKINSER = "L", disable black insertion.
BLKINSER = "H", enable black insertion. (Default)</td></tr>
<tr><td>BISTB
(VCC)</td><td>I</td><td>Normal Operation/BIST pattern select. Normally pull high.
BISTB = "L", BIST(DCLK input is not needed)
BISTB = "H", Normal Operation(Default).</td></tr>
<tr><td>BIST_CLK
(VCC)</td><td>I</td><td>External Clock input for BIST mode. Normally pull high.</td></tr>
<tr><td>BIST_CKSL
(VCC)</td><td>I</td><td>BIST Clock select. Normally pull high.
BTCK_ENB="L", BIST operation with external input clock.
BTCK_ENB="H", BIST operation with internal clock. (Default)</td></tr>
<tr><td>BIST_AUTO
(VCC)</td><td>I</td><td>Setting for BIST pattern automatical display @ BIST mode. Normally pull high.
BTPN_AUTO = "L", BIST Pattern is fixed current pattern.
BTPN_AUTO = "H", BIST Pattern is changed automatically. (Default)</td></tr>
<tr><td>NBW
(VCC)</td><td>I</td><td>Normally black or normally white setting. Normally pull high.
NBW = "L": Normally white.
NBW = "H": Normally black. (Default)</td></tr>
<tr><td>RTERM_EN
(VCC)</td><td>I</td><td>Terminal resistor disable/enable select pin. Normally pull high. (for Pin Control only)
RTERM_EN="L", Terminal resistor disable.
RTERM_EN="H", Terminal resistor enable. (Default)
Note: This setting is only for MIPI interface.</td></tr>
<tr><td>RTERM[1:0]
(VCC)
TP29,TP28</td><td>I</td><td>Terminal resistor select pin. Normally pull high.
<table>
<tr><th>RTERM[1] (TP29)</th><th>RTERM[0] (TP28)</th><th>Ratio</th></tr>
<tr><td>L</td><td>L</td><td>Terminal resistor is 75Ω.</td></tr>
<tr><td>L</td><td>H</td><td>Terminal resistor is 150Ω.</td></tr>
<tr><td>H</td><td>L</td><td>Terminal resistor is 250Ω.</td></tr>
<tr><td>H</td><td>H</td><td>Terminal resistor is 100Ω. (Default)</td></tr>
</table>
Note: This setting is only for MIPI interface.</td></tr>
<tr><td>INVSEL[1:0]
(VCC)
TP33,TP32</td><td>I</td><td>Inversion method selection. Normally pull high.
<table>
<tr><th>INVSEL[1]</th><th>INVSEL[0]</th><th>Function</th></tr>
<tr><td>H</td><td>H</td><td>Column inversion. (Default)</td></tr>
<tr><td>H</td><td>L</td><td>2 line 1 dot inversion.</td></tr>
<tr><td>L</td><td>H</td><td>1 + 2 line 1 dot inversion.</td></tr>
<tr><td>L</td><td>L</td><td>1 line 1 dot inversion.</td></tr>
</table></td></tr>
<tr><td>OPDRV[1:0]
(VCC)</td><td>I</td><td>Source OP Driving selection. Normally pull high.
<table>
<tr><th>OPDRV[1]</th><th>OPDRV[0]</th><th>Ratio</th></tr>
<tr><td>L</td><td>L</td><td>75%</td></tr>
<tr><td>L</td><td>H</td><td>125%</td></tr>
<tr><td>H</td><td>L</td><td>150%</td></tr>
<tr><td>H</td><td>H</td><td>100% (Default)</td></tr>
</table></td></tr>
<tr><td>VCC_EN
(VDD)</td><td>I</td><td>VDD LDO on/off control pin. Normally pull high. (for Pin Control only)
VCC_EN="L", VCC LDO disable.
VCC_EN="H", VCC LDO. Enable (Default)</td></tr>
<tr><td>VCOM_EN
(VCC)</td><td>I</td><td>VCOM OP on/off control. Normally pull high. (for Pin Control only)
VCOM_EN = "L", VCOM OP disable.
VCOM_EN = "H", VCOM OP enable. (Default)</td></tr>
<tr><td>HAOP_EN
(VCC)</td><td>I</td><td>HAVDD OP on/off control. Normally pull high. (for Pin Control only)
HAOP_EN = "L", HAVDD OP disable.
HAOP_EN = "H", HAVDD OP enable. (Default)</td></tr>
</table>

<table>
<tr><th>Designation (Domain)</th><th>I/O</th><th>Description</th></tr>
<tr><td>VCOM_UGB
(VCC)</td><td>I</td><td>VCOM OP type selection. Normally pull high. (for Pin Control only)
VCOM_UGB = "L", VCOM OP is Operational Amplifier
VCOM_UGB = "H", VCOM OP is Unit Gain Buffer. (Default)</td></tr>
<tr><td>CABC_ENB[1:0]
(VCC)</td><td>I</td><td>CABC H/W enable pin. Normally pull high.
<table>
<tr><th>CABC_ENB[1]</th><th>CABC_ENB[0]</th><th>Function</th></tr>
<tr><td>L</td><td>L</td><td>Moving Image.</td></tr>
<tr><td>L</td><td>H</td><td>Still Picture.</td></tr>
<tr><td>H</td><td>L</td><td>User interface Image.</td></tr>
<tr><td>H</td><td>H</td><td>CABC OFF(Default)</td></tr>
</table></td></tr>
<tr><td>CE_ENB
(VCC)</td><td>I</td><td>Color enhancement function enable pin. Normally pull high.
CE_ENB = "L", Color enhancement function enabled.
CE_ENB = "H", Color enhancement function disabled. (Default)</td></tr>
<tr><td>ALSIN
(VDD)</td><td>I</td><td>ALS sensor PWM signal input.</td></tr>
<tr><td>CMD_SEL
(VCC)</td><td>I</td><td>Registers command interface selection. Normally pull high. (for Pin Control only)
<table>
<tr><th>CMD_SEL</th><th>Register Command interface</th></tr>
<tr><td>L</td><td>I2C</td></tr>
<tr><td>H</td><td>MIPI(Default)</td></tr>
</table></td></tr>
<tr><td>SCL
(VDD)</td><td>I</td><td>I2C Serial communication clock input.
If not in use, fixed this pin to GND.</td></tr>
<tr><td>SDA
(VDD)</td><td>I/O</td><td>I2C Serial communication data input/output.
If not in use, pulled this pin to GND.</td></tr>
<tr><td>I2C_SCL
(VDD)</td><td>O</td><td>Serial input clock in I2C-Bus interface operation.
This pin is for PMU/LED setting only.</td></tr>
<tr><td>I2C_SDA
(VDD)</td><td>I/O</td><td>Serial input/output data in I2C-Bus interface operation.
This pin is for PMU setting only.
If not in use, please float this pin.</td></tr>
<tr><td>LED_EN
(VCC)</td><td>I</td><td>LEDON signal on/off control. Normally pull high. (for Pin Control only)
LED_EN = "L", Disable LEDON signal.
LED_EN = "H", Enable LEDON signal.(Default)</td></tr>
<tr><td>LEDON
(VDD)</td><td>O</td><td>This pin is connected to the external LED driver.
It is a LED driver control signal which is used for turning on/off the LED backlight.
If not in use, please float this pin.</td></tr>
<tr><td>LEDPWM
(VDD)</td><td>O</td><td>This pin is connected to the external LED driver.
PWM control signal for brightness of the LED backlight.
If not in use, please float this pin.</td></tr>
<tr><td>PMU_EN
(VDD)</td><td>O</td><td>PMU enable/disable control.
PMU_EN ="L", PMU disable.
PMU_EN ="H" PMU enable.</td></tr>
<tr><td>STATE
(VDD)</td><td>I</td><td>PMU Status indicator, Normally pull high.
After enable to PMU IC by I2C-Bus, the STATE pin can pull high.</td></tr>
<tr><td>GPMOE
(VDD)</td><td>O</td><td>Output signal for gate pulse shaping control.
This pin is for external GPM use.</td></tr>
<tr><td>GIP_EN
(VCC)</td><td>I</td><td>GIP mode enable/disable pin. Normally pull high.
GIP_EN="L", Normal mode.
GIP_EN="H", GIP mode.(Default)</td></tr>
<tr><td>GIP_SEL[3:0]
(VCC)</td><td>I</td><td>GIP mode selection pin. Normally pull high. (for Pin Control only)
Please refer to the related application notice.</td></tr>
</table>

Designation (Domain)	I/O	Description
TP_SYNC (VDD)	O	Sync signal for touch panel. Note: Recommended to connect this pin to FPC.
V1/V4/V7/ V8/V11/V14 TP22,TP23,TP24 TP25,TP26,TP27	R	Reference point for internal gamma string. Note: 1. Connect V4/V7/V8/V11 for all IC together was suggested. 2. Connect V4/V11 for all IC together was recommended. 3. Method: SDLOC="HH" SDLOC="HL" V4 ←→ V4 V11 ←→ V11
LSTVB (VCC)	I	STV pulse width selection. **Normally pull high.** LSTVB = "0", Long STV pulse width LSTVB = "1", Single STV pulse width. (Default)
XON_IN (VDD)	I	XON input signal. **Normally pull high.** XON_IN = "L", XON function enabled XON_IN = "H", XON function disabled. (Default)
SYNC1R ~ SYNC6R	I/O	Driver IC sync signal. It is necessary to connect between each Driver IC.
SYNC1L ~ SYNC6L	I/O	Driver IC sync signal. It is necessary to connect between each Driver IC.
OEVR / OEVL (VDD)	I/O	Gate driver control or sync signal. It is necessary to connect between each Driver IC.
UDR / UDL (VDD)	I/O	Gate driver control or sync signal. It is necessary to connect between each Driver IC.
CKVR / CKVL (VDD)	I/O	Gate driver control or sync signal. It is necessary to connect between each Driver IC.
STV1R / STV1L (VDD)	I/O	Gate driver control or sync signal. It is necessary to connect between each Driver IC.
STV2R / STV2L (VDD)	I/O	Gate driver control or sync signal. It is necessary to connect between each Driver IC.
XONR / XONL (VDD)	I/O	Gate driver control or sync signal. It is necessary to connect between each Driver IC.
GIPIO_L[19:0] GIPIO_R[19:0] (VGH-VGL)	O	GIP control signal. Please refer to the related application notice.
VGL	O	VGL voltage for GIP control circuit. (Between GIPIOs)
VDD	PI	Power supply for digital circuits.
GND	PI	Ground pins for digital circuits.
AVDD	PI	Power supply for analog circuits.
AGND	PI	Ground pins for analog circuits.
AGND1	PI	Ground pins for gamma generation circuits. Pad No. 97, 98, 256, and 257.
HAVDD	PI	Power supply for analog circuit.
VCC_IF	PI	Power supply for MIPI interface.
GND_IF	PI	Ground pins for MIPI interface.
VCC	PI	VCC LDO output for internal digital circuit use.
VLPH	P	VLPH LDO output for MIPI interface.

Designation (Domain)	I/O	Description
VGH_R/L	I	Power supply for GIP circuits. Note: 1. No matter GIP function was in use or not, this supply voltage needed be applied. 2. VGH_R and VGH_L both need supply voltage.
VGL	I	Power supply for GIP circuits. Note: No matter GIP function was in use or not, this supply voltage needed be applied. VGL have to connect a Schottky Diode to AGND.
VQH	C	Power setting capacitor connect pin. Note: Connect VQH for all IC together.
VQL	C	Power setting capacitor connect pin. Note: Connect VQL for all IC together.
VCOMPI	I	VCOM OP positive input.
VCOMNI	I	VCOM OP negative input.
VCOMO	O	VCOM OP output
HAOP	O	HAVDD OP output
RPEN_ODD (VCC)	I	ODD Repair OP on/off control. **Normally pull high.** (for Pin Control only) RPEN_ODD = "L", ODD Repair OP disable. RPEN_ODD = "H", ODD Repair OP enable. (Default) Note: ODD Repair OP be used only for Odd source channels (SO[1], SO[3], SO[5], …)
RPI_ODD	I	ODD Repair OP input
RPO_ODD	O	ODD Repair OP output
RPEN_EVEN (VCC)	I	EVEN Repair OP on/off control. **Normally pull high.** (for Pin Control only) RPEN_EVEN = "L", EVEN Repair OP disable. RPEN_EVEN = "H", EVEN Repair OP enable. (Default) Note: EVEN Repair OP be used only for Even source channels (SO[0], SO[2], SO[4], …)
RPI_EVEN	I	EVEN Repair OP input.
RPO_EVEN	O	EVEN Repair OP output.
VPP_MTP	I	Power supply for MTP circuit. Float this pin for normal operation.
SO[1802:0]	O	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
COMR1_IN COMR1_OUT	S	Internal link together between input side and output side. Input range: AVDD ~ AGND.
COMR2_IN COMR2_OUT	S	Internal link together between input side and output side. Input range: AVDD ~ AGND.
COML1_IN COML1_OUT	S	Internal link together between input side and output side. Input range: AVDD ~ AGND.
COML2_IN COML2_OUT	S	Internal link together between input side and output side. Input range: AVDD ~ AGND.
COM3_IN COM3_OUT	S	Internal link together between input and output. Input range: AVDD ~ AGND.
COM4_IN COM4_OUT	S	Internal link together between input and output. Input range: AVDD ~ AGND.
COM5_IN COM5_OUT	S	Internal link together between input and output. Input range: AVDD ~ AGND.
TP[41:0]	T	Test pin for Novatek only. Float these pins for normal operation.
TM[7:0]	T	Test pin for Novatek only. Float these pins for normal operation.

Designation (Domain)	I/O	Description
SHIELDING	SH	IC Shielding pads. Float these pins for normal operation.
SHIELDING_GND	SH	IC Shielding pads. Float these pins for normal operation.
SHIELDING_AGND	SH	IC Shielding pads. Float these pins for normal operation.
DASHD	SH	Data Bus Shielding pad. Those pins are internally connected to the GND. RECOMMAND to add shielding lines on the FPC to reduce EMI.

Legend: I: Input, O: Output, I/O: Input/Output, PI: Power Input, SH: Shielding Pin, C: Capacitor, S: Pass line, T: Testing, R: Reference point, L: Low level, H: High Level.

Note: 1. The GRB pin was suggested to have the external reset control. If no external reset control, the RC circuit was suggested. The suggested RC value was 10Kohm, 1uF.
2. All Power input pins was requested to apply voltage externally.
3. The I2C Slave Address combine by "110" + SA[3:2] + SDLOC[1:0].
For instance, with SA[3:2] = "11" and SDLOC[1:0]="11", Slave address = "110_1111".

Table 2. Pass Line Description:

Pass Line No:	Pad Name		Note
1	COMR1_IN	COMR1_OUT	COMR1_IN is connected to COMR1_OUT internally.
2	COMR2_IN	COMR2_OUT	COMR2_IN is connected to COMR2_OUT internally.
3	COML1_IN	COML1_OUT	COML1_IN is connected to COML1_OUT internally.
4	COML2_IN	COML2_OUT	COML2_IN is connected to COML2_OUT internally.
5	COM3_IN	COM3_OUT	COM3_IN is connected to COM3_OUT internally.
6	COM4_IN	COM4_OUT	COM4_IN is connected to COM4_OUT internally.
7	COM5_IN	COM5_OUT	COM5_IN is connected to COM5_OUT internally.

6.1. Value of Wiring Resistance

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Table 3. Wiring Resistance

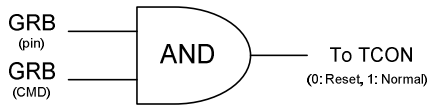
Pin Name	Wiring resistance (Ω)	Pin Name	Wiring resistance (Ω)	Pin Name	Wiring resistance (Ω)
D0P/D0N	<5	VCOM_UGB	<100	STV1L/STV1R	<100 (**)
D1P/D1N	<5	RPEN_ODD	<100	STV2L/STV2R	<100 (**)
D2P/D2N	<5	RPEN_EVEN	<100	XONR/XONL	<100 (**)
D3P/D3N	<5	CABC_ENB[1:0]	<100	GIPIO_L[19:0]	<50 (***)
CLKP/CLKN	<5	CE_ENB	<100	GIPIO_R[19:0]	<50 (***)
SHLR	<100	ALSIN	<100	VGL(For GIP)	<50 (***)
UPDNB	<100	CMD_SEL	<100	VDD	<5
ZIGZAG	<100	SDA	<50	GND	<5
ZTYPE	<100	SCL	<50	AGND	<5
RES[1:0]	<100	I2C_SDA	<50	AVDD	<5
GRB	<100	I2C_SCL	<50	HAVDD	<5
STBYB	<100	LED_EN	<100	VCC_IF	<3
PORT2B	<100	LEDON	<100	GND_IF	<3
SDLOC[1:0]	<100	LEDPWM	<100	VCC	<5
SA[3:2]	<100	PMU_EN	<100	VLPH	<5
BLKINSER	<100	STATE	<100	VGH_R/L	<5
BISTB	<100	GPMOE	<100	VGL	<5
BIST_CLK	<10	GIP_EN	<100	VQH	<5
BIST_ENB	<100	GIP_SEL[3:0]	<100	VQL	<5
BIST_CKSL	<100	TP_SYNC	<100	VCOMPI	<5
BIST_AUTO	<100	V1/V7/V8/V14	<50	VCOMNI	<5
NBW	<100	V4 / V11	<20	VCOMO	<5
RTERM_EN	<100	LSTVB	<100	HAOP	<5
RTERM[1:0]	<100	XON_IN	<100	RPI_ODD	<5
OPDRV[1:0]	<100	SYNC1L~SYNC6L	<100 (*)	RPI_EVEN	<5
INVSEL[1:0]	<100	SYNC1R~SYNC6R	<100 (*)	RPO_ODD	<5
VCC_EN	<100	OEVL/OEVR	<100 (*) (**)	RPO_EVEN	<5
VCOM_EN	<100	UDR/UDL	<100 (*) (**)	VPP_MTP	<5
HAOP_EN	<100	CKVL/CKVR	<100 (*) (**)		

Note: (*)Connection between Source ICs.
(**)Source IC to Gate IC.
(***)Source IC to panel (GIP).

6.2. The relationship between Pin and Register

6.2.1. GRB pin/CMD control

Combination Logic



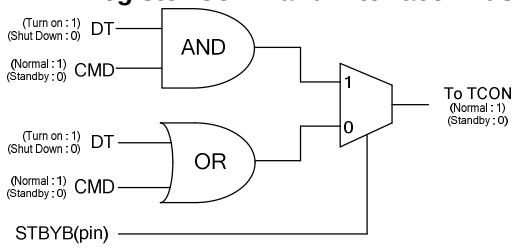
Truth Table

GRB(pin)	GRB(CMD)	TCON
0	0	0
0	1	0
1	0	0
1	1	1

6.2.2. STBYB pin/DT/CMD control

Combination Logic

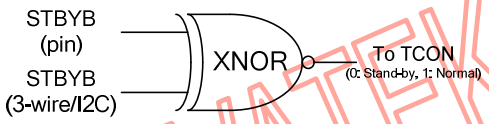
For MIPI Register Command interface in use.



Truth Table

STBYB(pin)	DT	CMD	TCON
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

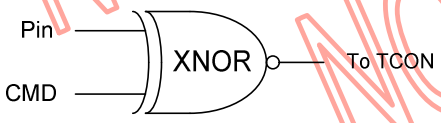
For I2C Register Command interface in use.



STBYB(pin)	STBYB(I2C)	TCON
0	0	1
0	1	0
1	0	0
1	1	1

6.2.3. Function pin/CMD control

Combination Logic

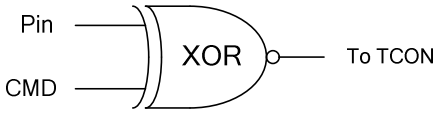


Truth Table

Pin	Register	TCON
0	0	1
0	1	0
1	0	0
1	**1**	**1**

Function list: SHLR, UPDNB, BISTB, BIST_CKSL, BLKINSER, PORT2B, ZIGZAG, ZTYPE, NBW, RES[1:0], RTERM_EN, LSTVB.

Combination Logic



Truth Table

Pin	Register	TCON
0	0	0
0	1	1
1	**0**	**1**
1	1	0

Function list: RTERM[1:0](TP29,TP28).

Note: "CMD" is the function register; include MIPI, I2C command.
"Pin" is the function control pin; "0" = "L" state, "1" = "H" state.
"DT" is the Data Type of MPI command.

7. MIPI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers. Systems using Command Mode write to, and read from the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Note: The NT51021 IC only supports Video Mode operation.

Table 4. MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0	Unidirectional Lane ■ Forward High-Speed ■ Forward Escape Mode ■ Forward LPDT
Data Lane1	Unidirectional ■ Forward High speed
Data Lane2	Unidirectional ■ Forward High speed
Data Lane3	Unidirectional ■ Forward High speed

7.1. Lane Configuration for DSI

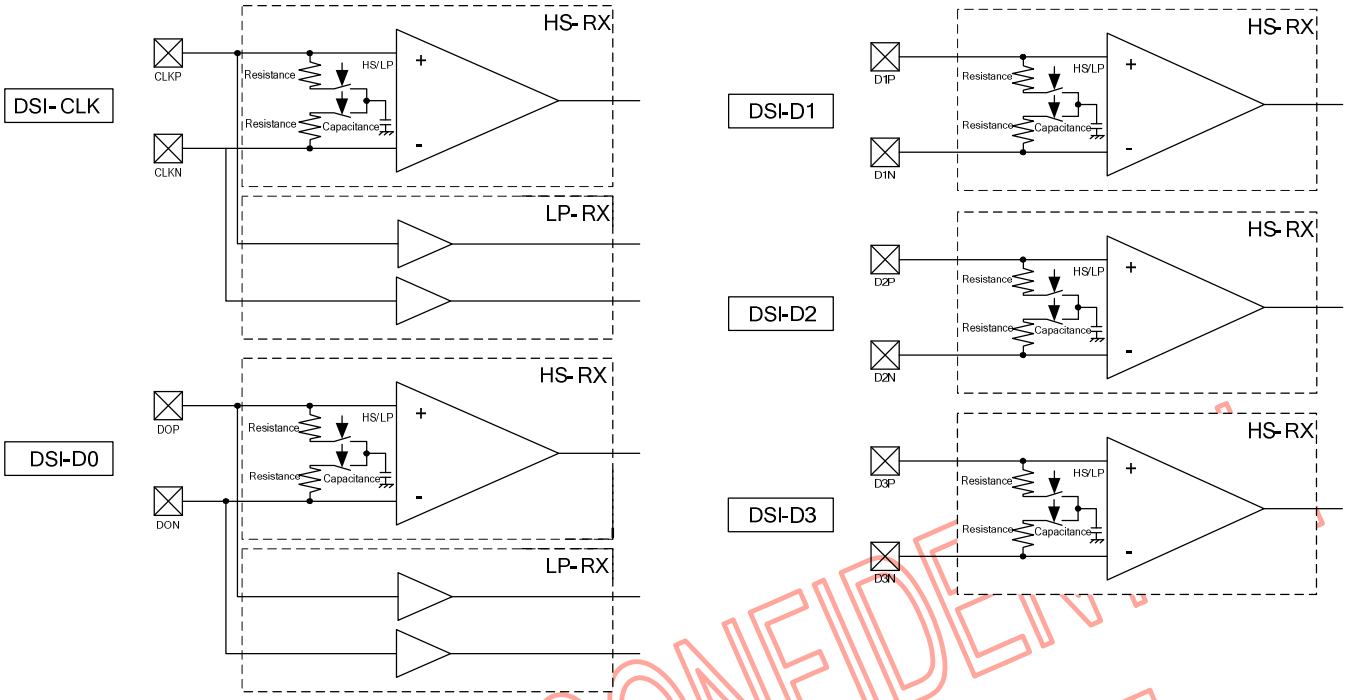


Figure 5. Pin Configuration for DSI

7.2. Display Serial Interface (DSI)

7.2.1. Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

• Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
• Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
• Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

During the BLLP the DSI Link may do any of the following:
• Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
• Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
• Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
• Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with HSS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scanline of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.

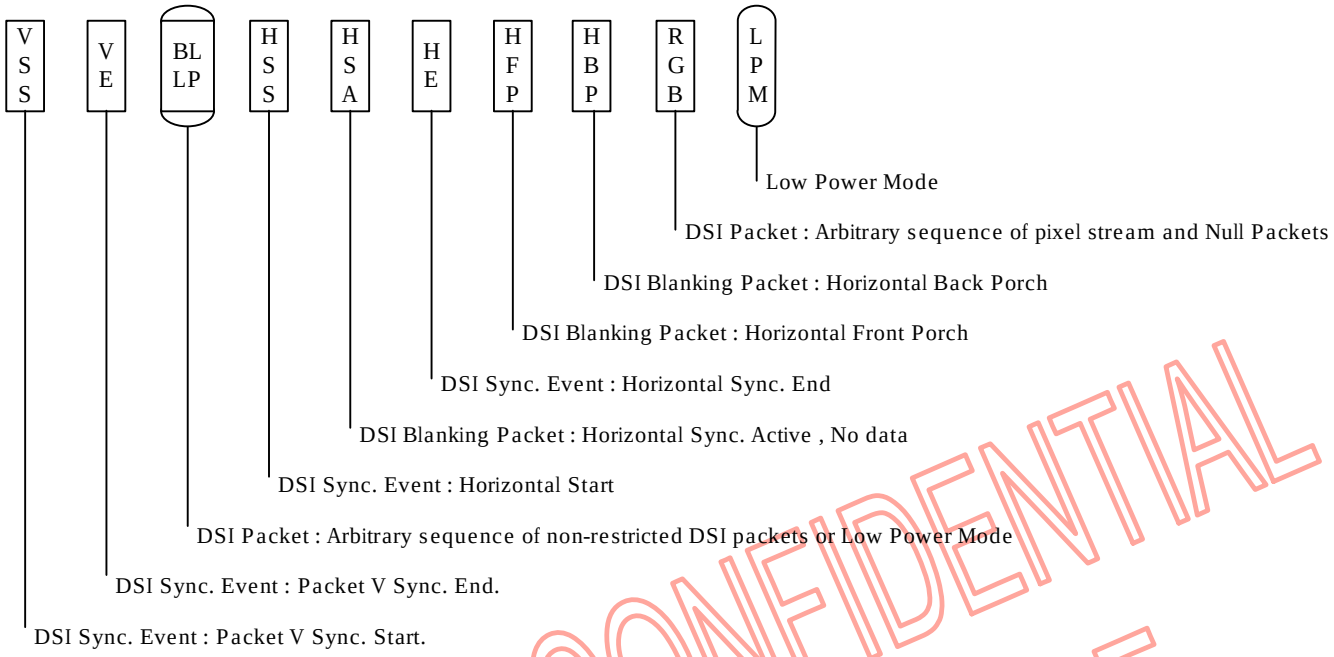


Figure 6. DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

Clock/Data Requirements

A DSI host processor shall support continuous clock/Data on the Clock/Data Lane for display module that require it. But every frame, the host must return to Low Power mode at once for MIPI signal synchronizing.

Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

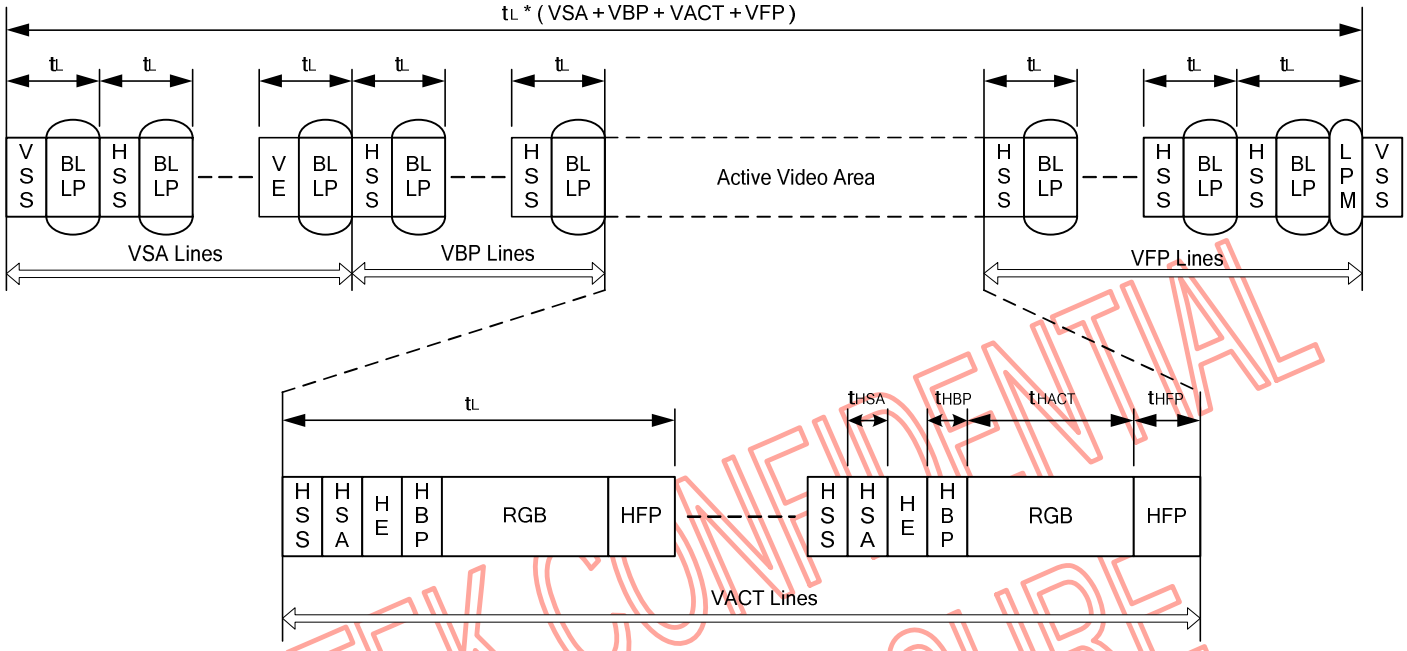


Figure 7. Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

Non-Burst Mode with Sync Events

This mode is a simplification of the format described in section "Non-Burst Mode with Sync Pulse" .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

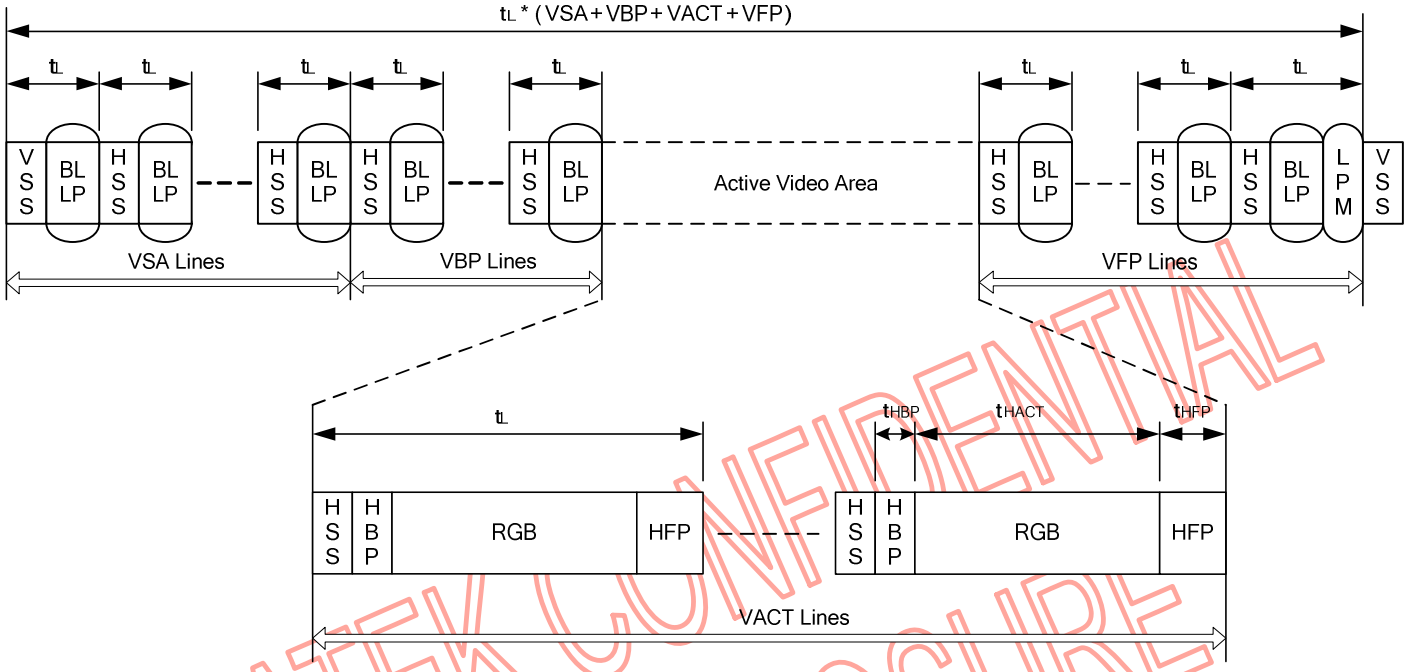


Figure 8. Non-Burst Transmission with Sync Event

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.

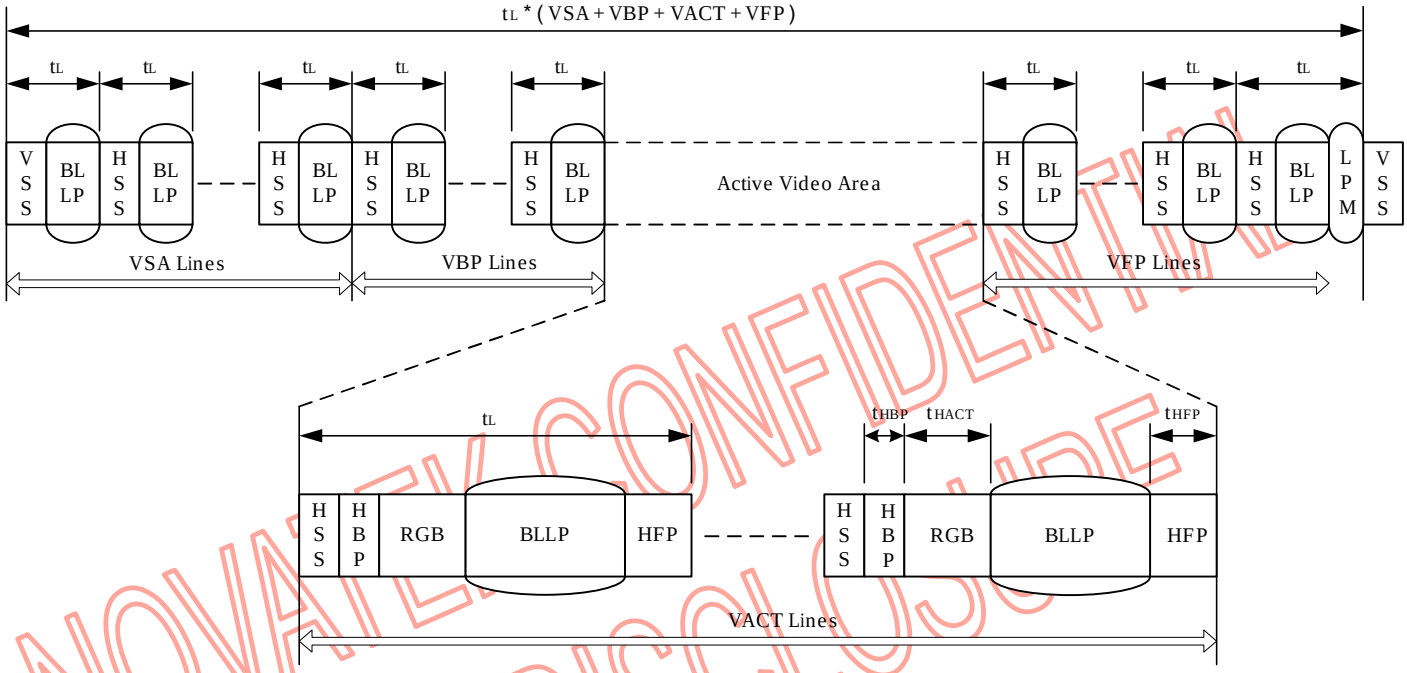


Figure 9. Burst Mode Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8. Command Descriptions

8.1. MIPI Control Registers

Following table list all the MIPI control registers and bit name definition for NT51021. Refer to the next section for detail register function description, please.

Setting of all the MIPI registers will take effect at the coming valid Vsync signal except GRB bit.

Table 5. MIPI control registers and bit name definition

No.	Register address								Register data							
									MSB							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R01H	0	0	0	0	0	0	0	1	GRB							
R10H	0	0	0	1	0	0	0	0	ENTER_SLEEP_MODE							
R11H	0	0	0	1	0	0	0	1	EXIT_SLEEP_MODE							
R8CH	1	0	0	0	1	1	0	0	0	0	0	0	V1_V14_SET (0)	GAM_SET (0)	HAOP_SET (0)	VCOM_SET (0)
R90H	1	0	0	1	0	0	0	0	1	1	1	1	1	1	UPDNB (1)	SHLR (1)
R91H	1	0	0	1	0	0	0	1	0	0	0	0	0	1	BIST_CKSL (1)	BISTB (1)
R92H	1	0	0	1	0	0	1	0	1	1	0	0	CABC[1:0] (11)		1	BLKINSER (1)
R93H	1	0	0	1	0	0	1	1	PORT2B (1)	ZIGZAG (1)	ZTYPE (1)	NWB (1)	1	1	RES[1:0] (11)	
R97H	1	0	0	1	0	1	1	1	RTERM11B[1:0] (00)		RTERMB10B[1:0] (00)		RTERMB01B[1:0] (00)		RTERMB00B[1:0] (00)	
RADH	1	0	1	0	1	1	0	1	LSTVB (1)	OE_WIDTH1[6:0] (0010000)						
RAEH	1	0	1	0	1	1	1	0	0	OE_WIDTH2[6:0] (1010100)						
RAFH	1	0	1	0	1	1	1	1	GPMOE_WIDTH[7:0] (01110000)							
RF0H	1	1	1	1	0	0	0	0	VCOM_SEL[7:0] (1100 1000)							
RFAH	1	1	1	1	1	0	1	0	0	0	0	HAOP_SEL[4:0] (01010)				
RFDH	1	1	1	1	1	1	0	1	V14_SEL[2:0] (000)			V1_SEL[4:0] (11111)				

8.2. I2C Interface protocol

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal output to the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I2C-Bus Protocol:
There are four slave address can be selected by Host of bus. The slave addressing is always carried out with the first byte transmitted after the START procedure.

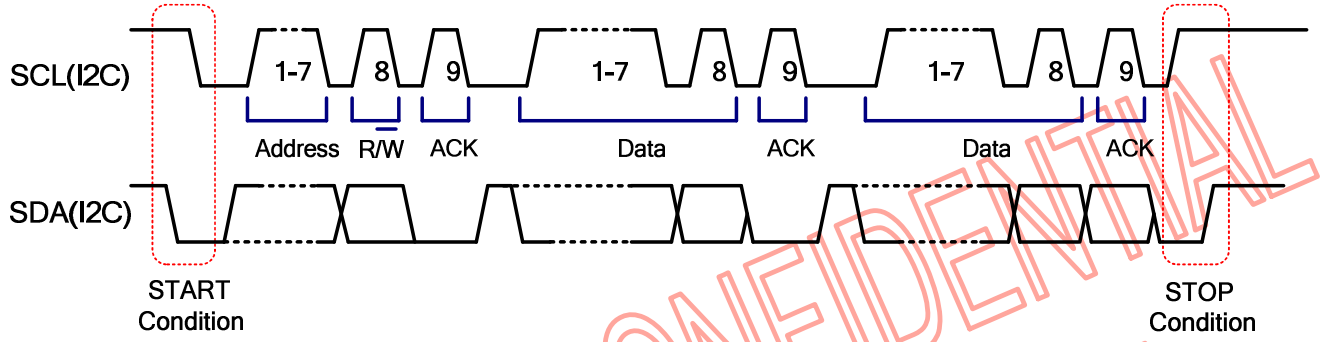


Figure 10. Definition of I2C-Bus Protocol

(b) Definitions:
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a bus transfer, generates clock signals and terminates a bus transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

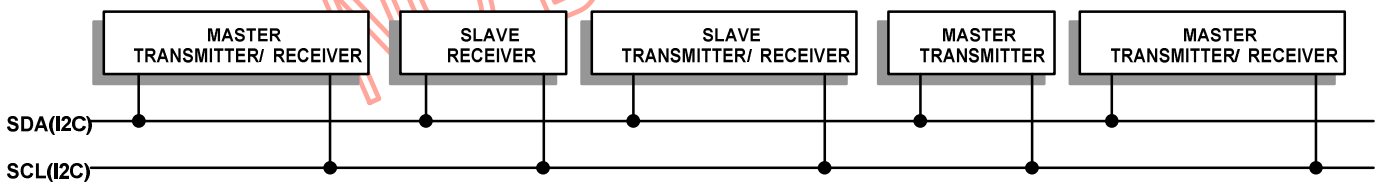


Figure 11. I2C bus connection

8.2.1. Register Write Sequence of I2C Interface

NT51021 supports register write sequence via I2C-bus transfer. The register writing support single register write mode and multi-register write mode.

The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in following figure.
(2) After the START condition, a slave address is sent. R/W bit is setting to "0" for WRITE.
(3) The slave issues an ACK to master.
(4) 8 bits register address transfer first then transfer the register data parameter.
(5) A data transfer is always terminated by a STOP condition.
(6) The chip SA[6:0]=110_11XX (in case of pin setting SA[3:2] = "HH".)

Figure 12. Single Register Writing Timing

8.2.2. Register Read Sequence of I2C Interface

NT51021 supports register read sequence via I2C-bus transfer. The register reading only support single register read mode. Register data reading transfers follow the format and is shown in following figure.

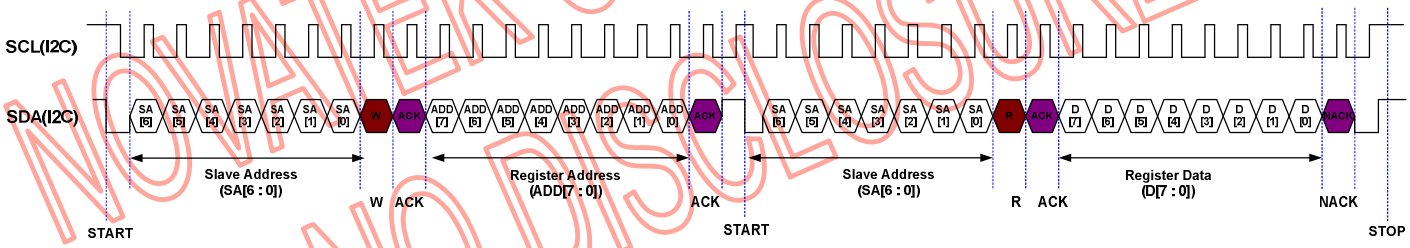


Figure 13. Single Register Reading Timing

Note: 1. For write operation, all IC with the same SA[6:2] will receive the data .
2. For read operation, only the IC match SA[6:0] will return the data.
3. ACK is low active, NACK is high active.
4. Only the IC match Slave Address will return ACK.

8.3. I2C Control Registers

Following tables list all the I2C control registers and bit name definition for NT51021. Refer to the next section for detail register function description, please.

Setting of all the I2C registers will take effect at the coming valid Vsync signal except GRB bit.

Table 6. I2C control registers and bit name definition

No.	Register address									Register data							
										MSB							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
R80H	0	0	0	0	0	0	0	0	1	RDID[7:0] (00000000)							
R89H	0	0	0	0	1	0	0	1	1/0	0	0	0	0	0	0	STBYB (1)	GRB (1)
R8CH	1	0	0	0	1	1	0	0	1/0	0	0	0	0	V1_V14_SET (0)	GAM_SET (0)	HAOP_SET (0)	VCOM_SET (0)
R90H	0	0	0	1	0	0	0	0	1/0	1	1	1	1	1	1	UPDNB (1)	SHLR (1)
R91H	0	0	0	1	0	0	0	1	1/0	0	0	0	0	0	1	BIST_CKSL (1)	BISTB (1)
R92H	0	0	0	1	0	0	1	0	1/0	1	1	0	0	1	1	1	BLKINSER (1)
R93H	0	0	0	1	0	0	1	1	1/0	PORT2B (1)	ZIGZAG (1)	ZTYPE (1)	NBW (1)	1	1	RES[1:0] (11)	
R97H	1	0	0	1	0	1	1	1	1/0	RTERMB11[1:0] (00)		RTERMB10[1:0] (00)		RTERMB01[1:0] (00)		RTERMB00[1:0] (00)	
RADH	0	0	1	0	1	1	0	1	1/0	LSTVB (1)	OE_WIDTH1[5:0] (0010000)						
RAEH	0	0	1	0	1	1	1	0	1/0	0	OE_WIDTH2[5:0] (1010100)						
RAFH	0	0	1	0	1	1	1	1	1/0	GPMOE_WIDTH[7:0] (01110000)							
RF0H	1	1	1	1	0	0	0	0	1/0	VCOM_SEL[7:0] (1100 1000)							
RFAH	1	1	1	1	1	0	1	0	1/0	0	0	0	HAOP_SEL[4:0] (01010)				
RFDH	1	1	1	1	1	1	0	1	1/0	V14_SEL[2:0] (000)			V1_SEL[4:0] (11111)				

8.4. Control Register Function

Table 7. GRB: Software Reset

Address (MIPI I/F)	01H					Access Attribute			W
Address (I2C I/F)	-					Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								N/A
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset register values and all source outputs are set to High-z.								
Restriction	It will be necessary to wait 20msec before sending new command following software reset.								

Table 8. ENTER_SLEEP_MODE: Enter the Sleep-In Mode

Address (MIPI I/F)	10H					Access Attribute			W
Address (I2C I/F)	-					Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								Sleep-In Mode
Description	This command initiates the power-down sequence. The Sleep In profile will be executed when this command is received.								
Restriction	1. This command has no effect when the display module is already in Sleep Mode. 2. This function will be influence by STBYB pin setting. (Please refer to section 6.2.The relationship between Pin and Register)								

Table 9. EXIT_SLEEP_MODE: Exit the Sleep-In Mode

Address (MIPI I/F)	11H					Access Attribute			W
Address (I2C I/F)	-					Number of Parameter(s)			0
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	No Argument								Sleep-In Mode
Description	This command initiates the power-up sequence. The Sleep Out profile will be executed when this command is received. The Sleep Out will load register value. It will be necessary to wait 5msec before sending next command.								
Restriction	1. This command will not cause any visible effect on the display when the display is not in Sleep Mode. 2. This function will be influence by STBYB pin setting. (Please refer to section 6.2.The relationship between Pin and Register)								

Table 10. (R80H) RDID: Read ID

Address (MIPI I/F)	-					Access Attribute			R
Address (I2C I/F)	80H					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	00h
Description	This read byte is used to track the display module/driver version. It is defined by display supplier and changed by request								
Restriction	-								

Table 11. (R89H) Control Register

Address (MIPI I/F)	-					Access Attribute			R/W
Address (I2C I/F)	89H					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	0	0	0	0	0	STBYB	GRB	03h
Description	**STBYB:** Standby mode. STBYB = "0", timing controller is off, and source driver outputs are High-Z STBYB = "1", normal operation. (Default) **GRB:** Global reset. GRB = "0", The controller is in reset state, all register are reset to default state. GRB = "1", Normal operation.(Default)								
Restriction	-								

Table 12. (R8CH) Control Register

Address (MIPI I/F)	8CH								R/W
Address (I2C I/F)	8CH					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	0	0	0	V1_V14_SET	GAM_SET	HAOP_SET	VCOM_SET	00h
Description	**V1_V14_SET:** Control source of V1/V14 setting. V1_V14_SET ="0", V1/V14 control by OTP memory. (Default) V1_V14_SET ="1", V1/V14 control by control register (RFDH). **GAM_SET:** Control source of Gamma circuit setting. GAM_SET ="0", Gamma control by OTP memory. (Default) GAM_SET ="1", Gamma control by control register (RFDH). **HAOP_SET:** Control source of HAOP setting. HAOP_SET ="0", HAOP control by OTP memory. (Default) HAOP_SET ="1", HAOP control by control register (RFDH). **VCOM_SET:** Control source of VCOM OP setting. VCOM_SET ="0", VCOM OP control by OTP memory. (Default) VCOM_SET ="1", VCOM OP control by control register (RFDH). Note: If the function didn't trimmed, it will directly controlled by register even set xxx_SET as "1".								
Restriction	-								

Table 13. (R90H) Control Register

Address (MIPI I/F)	90H					Access Attribute			R/W
Address (I2C I/F)	90H					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	1	1	1	1	1	1	UPDNB	SHLR	FFh
Description	**UPDNB:** This bit flips the image shown on the display device top to bottom. UPDNB: 0 – STV1 output vertical start pulse and UD pin output logical "1" to Gate driver. UPDNB: 1 – STV2 output vertical start pulse and UD pin output logical "0" to Gate driver.(Default) **SHLR:** This bit flips the image shown on the display device left to right. SHLR: 0 – Shift left: Last data=S1←S2←S3← … ←S1200=First data. SHLR: 1 – Shift right: First data=S1→S2→S3→ … →S1200=Last data.(Default)								
Restriction	-								

Table 14. (R91H) Control Register

Address (MIPI I/F)	91H					Access Attribute			R/W
Address (I2C I/F)	91H					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	0	0	0	0	1	BIST_CKSL	BISTB	07h
Description	**BIST_CKSL:** BIST clock selection. BIST_CKSL="0", BIST operates with external clock. BIST_CKSL="1", BIST operates with internal clock. (Default) **BISTB:** Normal Operation/BIST pattern selection. BISTB="0", BIST operation. BISTB="1", Normal Operation. (Default)								
Restriction	-								

Table 15. (R92H) Control Register

Address (MIPI I/F)	92H					Access Attribute			R/W
Address (I2C I/F)	92H					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	1	1	0	0	1	1	1	BLKINSER	CFh
Description	**BLKINSER:** Black insertion control when power on. BLKINSER="0", Disable black insertion when power on. BLKINSER="1", Enable black insertion when power on. (Default)								
Restriction	-								

Table 16. (R93H) Control Register

Address (MIPI I/F)	93H					Access Attribute			R/W
Address (I2C I/F)	93H					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	PORT2B	ZIGZAG	ZTYPE	NBW	1	1	RES[1:0]		FFh

Description

PORT2B:
Two/One port interface setting.

Pin	Register	Function
0	0	1 port interface
0	1	2 port interface
1	0	2 port interface
1	1	1 port interface (Default)

ZIGZAG:
Zig-Zag driving method setting.
ZIGZAG="0", Column driving method.
ZIGZAG="1", Zig-Zag driving method. (Default)

ZTYPE:
Zig-Zag panel layout type selection.
ZTYPE="0", Zig-Zag layout type0.
ZTYPE="1", Zig-Zag layout type1. (Default)

NBW:
Normally black or normally white setting.
NBW = "0", Normally white.
NBW = "1", Normally black. (Default)

RES[1:0]
Display resolution selection.

RES[1]	RES[0]	Resolution	Disable channels
L	L	1200(RGB)x1600	No disable channel
L	H	1080(RGB)x1920	811~990
H	L	600(RGB)x1024	No disable channel
H	H	1200(RGB)x1920	No disable channel (Default)

Restriction: -

Table 17. (R97H) Control Register

Address (MIPI I/F)	97H	Access Attribute	R/W
Address (Other I/F)	97H	Number of Parameter(s)	1

Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	RTERM11B[1:0]		RTERM10B[1:0]		RTERM01B[1:0]		RTERM00B[1:0]		00h

Description

RTERM11B[1:0]:
SDLOC[1:0] = "11" driver, terminal resistor selection.

RTERM11B[1]	RTERM11B[0]	Function
0	0	Terminal resistor is 100Ω. (Default)
0	1	Terminal resistor is 250Ω.
1	0	Terminal resistor is 150Ω.
1	1	Terminal resistor is 75Ω.

RTERM10B[1:0]:
SDLOC[1:0] = "10" driver, terminal resistor selection.

RTERM10B[1]	RTERM10B[0]	Function
0	0	Terminal resistor is 100Ω. (Default)
0	1	Terminal resistor is 250Ω.
1	0	Terminal resistor is 150Ω.
1	1	Terminal resistor is 75Ω.

RTERM01B[1:0]:
SDLOC[1:0] = "01" driver, terminal resistor selection.

RTERM01B[1]	RTERM01B[0]	Function
0	0	Terminal resistor is 100Ω. (Default)
0	1	Terminal resistor is 250Ω.
1	0	Terminal resistor is 150Ω.
1	1	Terminal resistor is 75Ω.

RTERM00B[1:0]:
SDLOC[1:0] = "00" driver, terminal resistor selection.

RTERM00B[1]	RTERM00B[0]	Function
0	0	Terminal resistor is 100Ω. (Default)
0	1	Terminal resistor is 250Ω.
1	0	Terminal resistor is 150Ω.
1	1	Terminal resistor is 75Ω.

Restriction	This register setting only available in MIPI LP mode transmission or I2C interface

Table 18. (RADH) Control Register

Address (MIPI I/F)	ADH					Access Attribute			R/W
Address (I2C I/F)	ADH					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	LSTVB	OE_WIDTH1[6:0]							90h

Description

LSTVB:
STV pulse width selection.
LSTVB = "0", Long STV pulse width
LSTVB = "1", Single STV pulse width. (Default)

OE_WIDTH1[6:0]:
OE1 width selection.

OE_WIDTH1[6:0]	Function
00h	Not support
01h	Not support
02h	2 x 12UI
03h	3 x 12UI
:	:
10h	16 x 12UI(Default)
:	:
7Eh	126 x 12UI
7Fh	127 x 12UI

Restriction

-

Table 19. (RAEH) Control Register

Address (MIPI I/F)	AEH					Access Attribute			R/W
Address (I2C I/F)	AEH					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	OE_WIDTH2[6:0]							54h

Description

OE_WIDTH2[6:0]:
OE2 width selection.

OE_WIDTH2[6:0]	Function
00h	Not support
01h	Not support
02h	4 x 12UI
03h	6 x 12UI
:	:
54h	168 x 12UI(Default)
:	:
7Eh	252 x 12UI
7Fh	254 x 12UI

Restriction

-

Table 20. (RAFH) Control Register

Address (MIPI I/F)	AFH					Access Attribute			R/W
Address (I2C I/F)	AFH					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	GPMOE_WIDTH[7:0]								70h
Description	**TCKVOE[3:0]:** TCKV_OE timing adjustment for Gate Pulse Modulation function.								
Restriction	-								

GPMOE_WIDTH[7:0]	Function
00h	0 x 12UI
01h	1 x 12UI
:	:
70h	112 x 12UI(Default)
:	:
FEh	254 x 12UI
FFh	255 x 12UI

Table 21. VCOM OP Control Register

MIPI I/F Address	F0h					Access Attribute			R/W
Address (Other I/F)	F0h					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	VCOM_SEL[7:0]								C8h
Description	**VCOM_SEL[7:0]:** The VCOM OP output voltage select								

VCOM_SEL[7:0]	VCOMO output voltage (V)
00h	1.50
01h	1.51
02h	1.52
:	:
C7h	3.49
C8h(Default)	3.50
C9h	3.51
:	:
FEh	4.04
FFh	4.05

Note:
HAVDD-0.5V ≥ VCOMO

Table 22. HAOP OP Control Register

MIPI I/F Address	FAh					Access Attribute			R/W
Address (Other I/F)	FAh					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	0	0	0	HAOP_SEL[4:0]					0Ah

Description

HAOP_SEL[4:0]:
HAVDD OP output voltage select.

HAOP_SEL[4:0]	HAOP output voltage (V)
00h	3.45
01h	3.525
:	:
08h	4.05
09h	4.125
0Ah(Default)	4.2
:	:
14h	4.95
15h	5.025
16h	5.025
:	:
1Fh	5.025

Note :
1. 5V ≥ AVDD - HAVDD ≥ 3.5V, 5V ≥ HAVDD - AGND ≥ 3.5V
2. Voltage Interval: 75mV / step.

Table 23. V1/V14 Control Register

MIPI I/F Address	FDh					Access Attribute			R/W
Address (Other I/F)	FDh					Number of Parameter(s)			1
Parameter	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
	V14_SEL[2:0]			V1_SEL[4:0]					0Fh

Description

V1_SEL[4:0]:
V1 voltage selection.

V1_SEL[4:0]	V1 voltage (V)
00h	6.7
01h	6.8
:	:
0Fh(Default)	8.2
10h	8.3
:	:
1Eh	9.7
1Fh	9.8

V14_SEL[2:0]:
V14 voltage selection.

V14 SEL[2:0]	V14 voltage (V)
0h(Default)	0.2
1h	0.3
2h	0.4
3h	0.5
4h	0.6
5h	0.7
6h	0.8
7h	0.8

Note :
1. Voltage Interval: 100mV / step.
2. AVDD ≥ V1+0.5V.
3. V1 ≥ 0.75 * (AVDD-HAVDD)+HAVDD.

9. Function Description

9.1. Power-On/Off Timing Sequence:

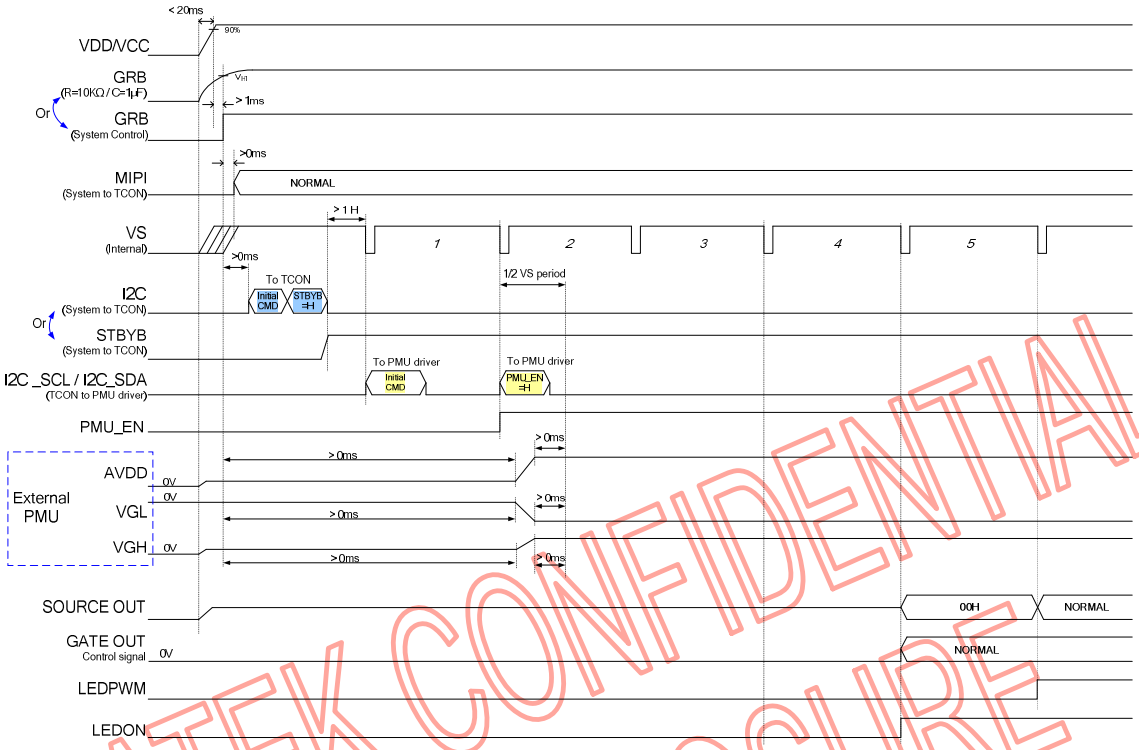


Figure 14. Power On Timing Sequence

Figure 15. Power Off Timing Sequence

9.2. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Gamma Table differ for each customer. Contact Novatek for more detail information.

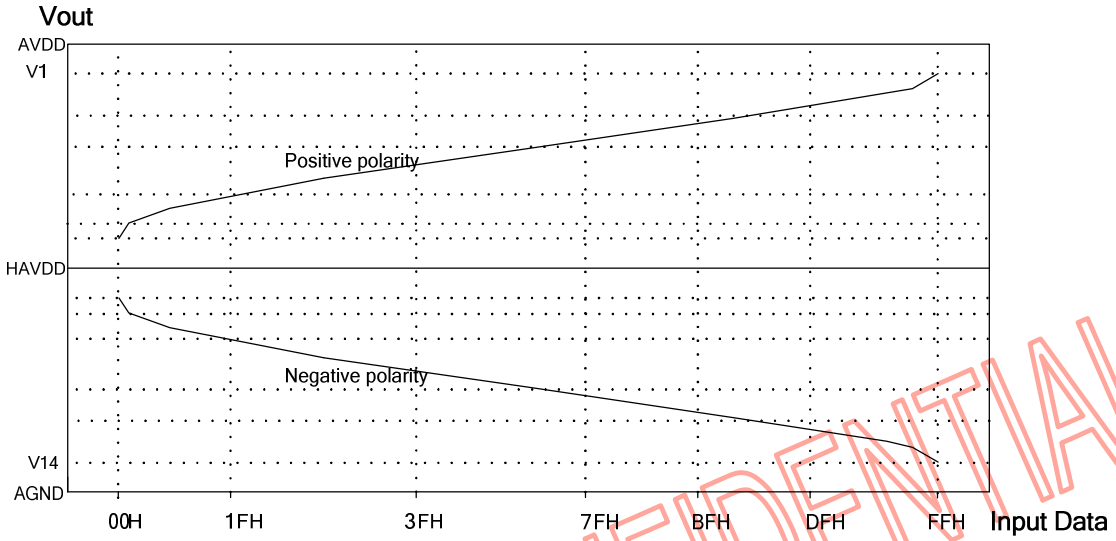


Figure 16. Input Data VS Output Voltage

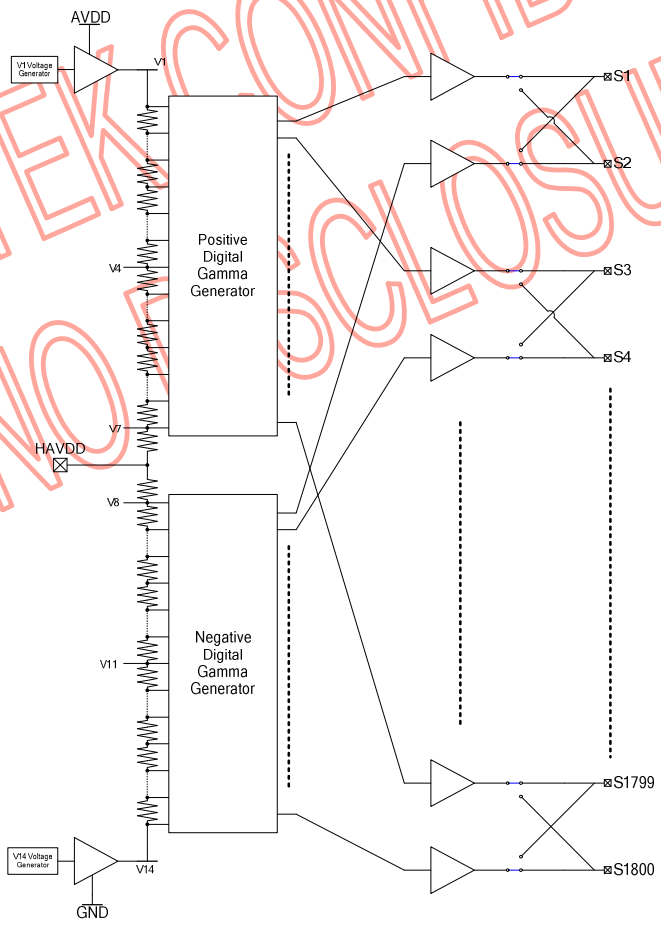


Figure 17. Gamma Generation

9.3. Content Adaptive Brightness Control (CABC) Function

The NT51021 embedded Content Adaptive Brightness Control (CABC) function. The function is used to generate a proper PWM signal based on internal CABC algorithms. User could apply this PWM signal to control other device(s) (Such as power IC or LED driver IC). When the CABC function is enabled and cooperate with external circuits (such as LED driver circuit), the power consumption of backlight will be reduced with keeping acceptable display quality.

The function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously decreasing brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image. The NOVATek CABC algorithm can adjust the brightness of each gray level without changing the original image contents.

The NOVATek CABC function provides four operation modes, and these modes can be selected by the register and pin. These four modes are described as:

- Off Mode:

Content Adaptive Brightness Control functionality is completely turn-off. In this mode, the NT51021 will use the original Gamma 2.2 registers setting for display. And if the function of "forced PWM duty" is turn-off (i.e. "FORCE_CABC_PWM" is set as ‘0’), the PWM duty of the "LEDPWM" pin is 100%.

- UI [User interface] Image Mode (UI-Mode):

This mode is applied to optimize for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.

- Still Picture Mode (Still-Mode):

This mode is used to gain a better display quality for still picture. Some image quality degradation would be acceptable. Ideal power consumption reduction ratio is more than 30%. The NT51021 will automatically estimate a better gamma setting and PWM duty based on different image contents, so the reduction ratio of the power consumption of backlight is not a constant ratio, this ratio will vary between 10% ~ 40% with different image contents.

- Moving Image Mode (Moving-Mode):

User can select this mode to keep the moving image quality and reduce the power consumption of backlight. It is focused on the biggest power reduction with image quality degradation. Idea power consumption reduction ratio is more than 30%.

9.4. The Route of Panel and Driving Method

The NT51021 support normal driving method and Zig-Zag driving method, and their route of panel are described as below:

9.4.1. Normal driving method: ZIGZAG = 0, ZTYPE = 0/1

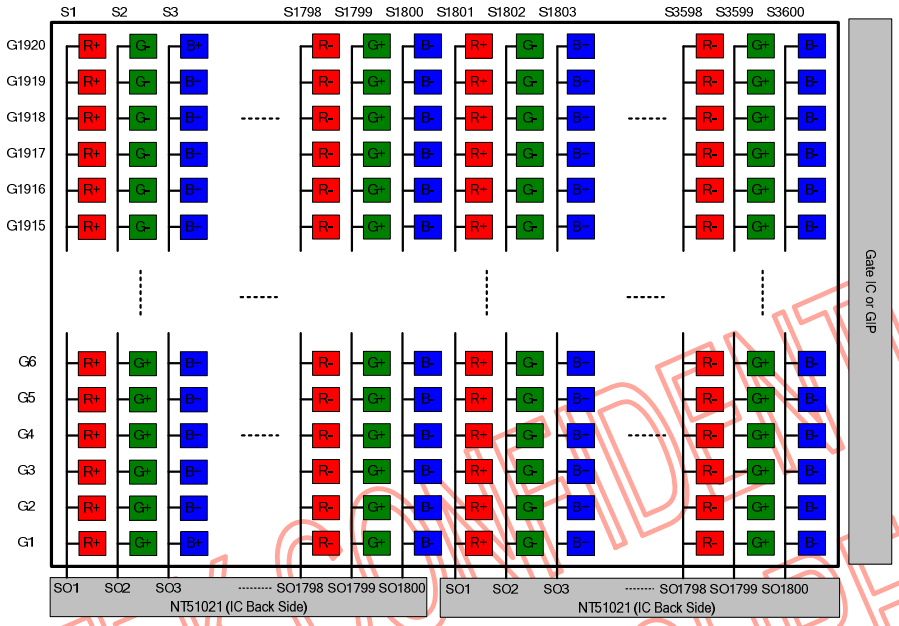


Figure 18. The route of panel for 1200RGBx1920 column driving method

9.4.2. Zig-Zag driving method: ZIGZAG = 1, ZTYPE = 1

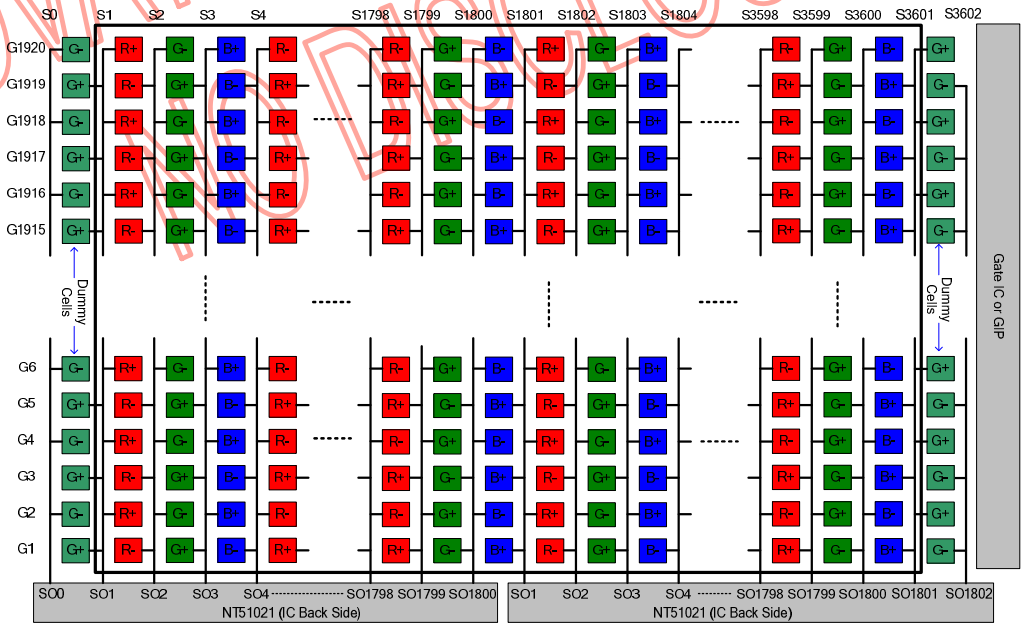


Figure 19. The route of panel for 1200RGBx1920 Zig-Zag type1 driving method

Note: 1. To implement Dummy Cell or not is basing on Panel's design concept.
2. UPDNB = "1", scan direction G1920 → G1919 → … → G1.

9.4.3. Zig-Zag driving method: ZIGZAG = 1, ZTYPE = 0

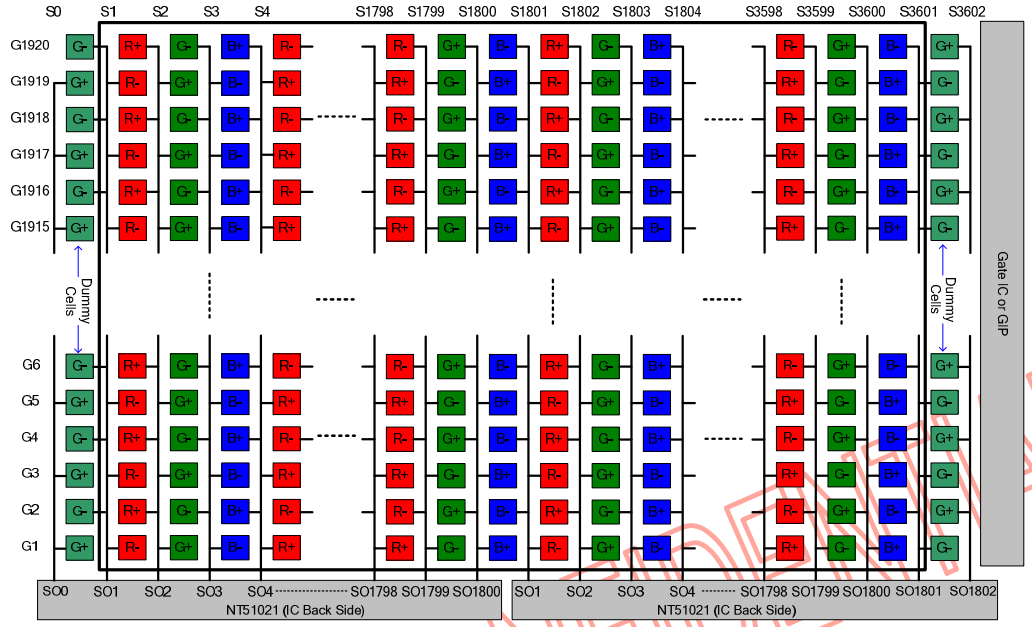


Figure 20. The route of panel for 1200RGBx1920 Zig-Zag type0 driving method

10. Data Input Format

10.1. Data Input Format for MIPI

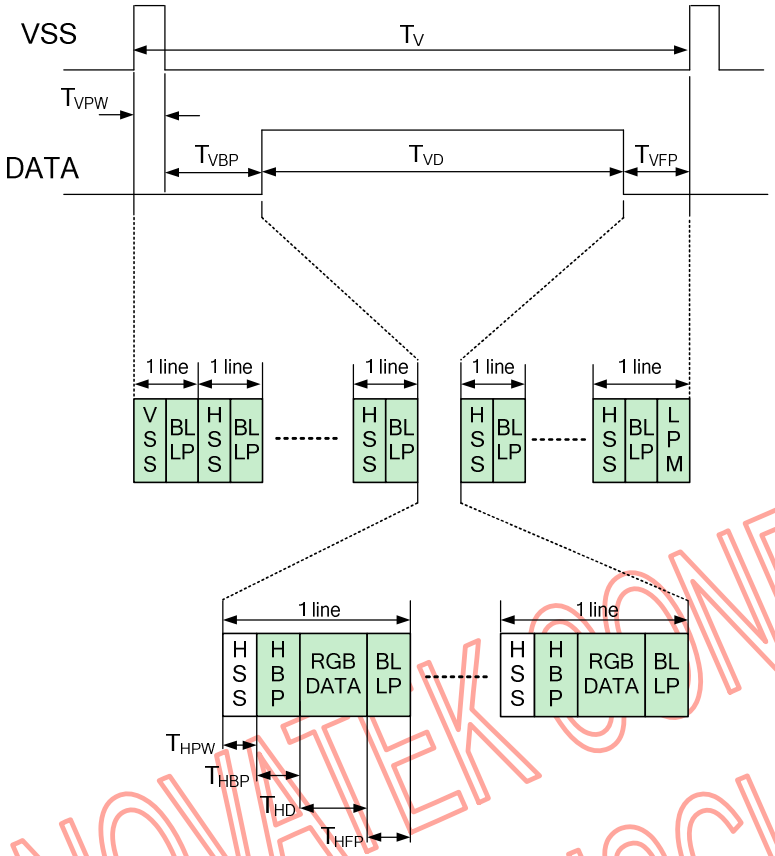


Figure 21. Data Input Format for MIPI

10.2. Input Timing Table

Table 24. 1200RGBx1920 (4 Data Lanes)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI data frequency	F_{DATA}	955	999	1000	Mbps
Horizontal display area	T_{HD}		1200		pixel
Hsync period time	T_H	1275	1341	1342	pixel
Hsync pulse width	T_{HPW}	1	1	1	pixel
Hsync back porch	T_{HBP}	32	60	60	pixel
Hsync front porch	T_{HFP}	42	80	81	pixel
Vertical display area	T_{VD}		1920		H
Vsync period time	T_V	1981	1981	1982	H
Vsync pulse width	T_{VPW}	1	1	1	H
Vsync back porch	T_{VBP}		25		H
Vsync front porch	T_{VFP}	35	35	36	H

Table 25. 600RGBx1024 (4 Data Lanes)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI data frequency	F_{DATA}	277	304	420	Mbps
Horizontal display area	T_{HD}		600		pixel
Hsync period time	T_H	675	741	901	pixel
Hsync pulse width	T_{HPW}	1	1	1	pixel
Hsync back porch	T_{HBP}	32	60	100	pixel
Hsync front porch	T_{HFP}	42	80	200	pixel
Vertical display area	T_{VD}		1024		H
Vsync period time	T_V	1085	1085	1225	H
Vsync pulse width	T_{VPW}	1	1	1	H
Vsync back porch	T_{VBP}		25		H
Vsync front porch	T_{VFP}	35	35	200	H

Table 26. 1080RGBx1920 (4 Data Lanes)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI data frequency	F_{DATA}	865	914	990	Mbps
Horizontal display area	T_{HD}		1080		pixel
Hsync period time	T_H	1155	1221	1321	pixel
Hsync pulse width	T_{HPW}	1	1	1	pixel
Hsync back porch	T_{HBP}	32	60	60	pixel
Hsync front porch	T_{HFP}	42	80	180	pixel
Vertical display area	T_{VD}		1920		H
Vsync period time	T_V	1981	1981	2001	H
Vsync pulse width	T_{VPW}	1	1	1	H
Vsync back porch	T_{VBP}		25		H
Vsync front porch	T_{VFP}	35	35	55	H

Table 27. 1200RGBx1600 (4 Data Lanes)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI data frequency	F_{DATA}	801	842	990	Mbps
Horizontal display area	T_{HD}		1200		pixel
Hsync period time	T_H	1275	1341	1461	pixel
Hsync pulse width	T_{HPW}	1	1	1	pixel
Hsync back porch	T_{HBP}	32	60	60	pixel
Hsync front porch	T_{HFP}	42	80	200	pixel
Vertical display area	T_{VD}		1600		H
Vsync period time	T_V	1661	1661	1801	H
Vsync pulse width	T_{VPW}	1	1	1	H
Vsync back porch	T_{VBP}		25		H
Vsync front porch	T_{VFP}	35	35	175	H

Note: 1. Above time table was based on GIP default setting.
2. The CABC and CE function was disabled.

11. Absolute Maximum Ratings

Table 28. Voltage
(GND = AGND = 0V, TA = 25°C)

	Min.	Max.	Unit
TCON supply voltage, VCC	-0.3	1.7	V
Interface supply voltage, VCC_IF	-0.3	1.7	V
Digital supply voltage, VDD	-0.3	5.5	V
Digital signal voltage. (VDD domain)	-0.3	VDD+0.3	V
Digital signal voltage. (VCC domain)	-0.3	VCC+0.3	V
Digital signal voltage. (VCC_IF domain)	-0.3	VCC_IF+0.3	V
Analog supply voltage, AVDD	-0.3	11	V
VGH supply voltage, VGH_R/L	-0.3	VGL+32	V
VGL supply voltage, VGL	-16	0.3	V

Table 29. Temperature

	Min.	Max.	Unit
Operating temperature	-20	85	°C
Storage temperature	-55	125	°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12. Recommended Operating Range

Table 30. Recommended Operating Range
(GND = AGND = 0V, TA = -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Digital supply voltage	VDD	2.7	3.3	3.6	V	
TCON supply voltage	VCC	1.4	1.5	1.6	V	External supply voltage
MIPI supply voltage	VCC_IF	1.4	1.5	1.6	V	External supply voltage
Analog supply voltage	AVDD	7	-	10	V	5V ≥ AVDD - HAVDD ≥ 3.5V
Analog supply voltage	HAVDD	3.5	AVDD/2	5	V	5V ≥ HAVDD - AGND ≥ 3.5V
VGH Voltage	VGH	15	15	26	V	VGH-VGL < 32V, to VGH_R/L pin.
VGL Voltage	VGL	-11.5	-5	-4	V	VGH-VGL < 32V
OTP supply voltage	VMTP	7.4	7.5	7.6	V	For VPP_MTP pin.

13. DC Electrical Characteristics

13.1. Basic DC Characteristic

Table 31. Basic DC characteristic

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD High level input voltage	V_{IH1}	0.7xVDD	-	VDD	V	For the VDD domain inputs.
VDD Low level input voltage	V_{IL1}	0	-	0.3xVDD	V	For the VDD domain inputs.
VCC High level input voltage	V_{IH2}	0.8xVCC	-	VCC	V	For the VCC domain inputs.
VCC Low level input voltage	V_{IL2}	0	-	0.2xVCC	V	For the VCC domain inputs.
I2C High level input voltage	V_{IH3}	1.65	-	VDD	V	For SDA/SCL inputs
I2C Low level input voltage	V_{IL3}	0	-	0.2	V	For SDA/SCL inputs
Input leakage current	I_I	-	-	±1	uA	For the digital, I/O circuit (Not include the pull-up/down)
Differential input leakage current	I_{DIFFI}	-10	-	+10	uA	For DxP, DxN, CLKP, CLKN (With steady state inputs)
High level output voltage	V_{OH}	VDD-0.4	-	-	V	I_{OH}= -400uA For VDD/VDDIO domain outputs.
Low level output voltage	V_{OL}	-	-	GND+0.4	V	I_{OL}= +400uA For VDD/VDDIO domain outputs.
Pull low/high resistor	R_I	100K	250K	500K	ohm	For the digital input pin @ VDD=3.3V / VCC=1.5V
Output Voltage deviation	V_{OD1}	-	±20	±35	mV	Vo = AGND+0.2V ~ AGND+1.5V Vo = HAVDD-0.2V ~ HAVDD-1.5V Vo = HAVDD+0.2V ~ HAVDD+1.5V Vo = AGND+0.2V ~ AGND+1.5V
Output Voltage deviation	V_{OD2}	-	±15	±20	mV	Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Output Voltage Offset between Chips	V_{OC}	-	-	±20	mV	Vo = AGND+1.5V ~ HAVDD-1.5V Vo = HAVDD+1.5V ~ AVDD-1.5V
Dynamic Range of Source Output	V_{DR}	0.2	-	AVDD-0.2	V	SO0~SO1802
Sinking Current of Source Outputs	I_{SOS}	80	-	-	uA	SO0~SO1802; Vo=0.2V v.s 1.1V, AVDD=10V
Driving Current of Source Outputs	I_{SOD}	80	-	-	uA	SO0~SO1202; Vo=9.8V v.s8.9V, AVDD=10V
Sinking Current of GIP Outputs	I_{GOS}	1	-	-	mA	GIPIO0~GIPIO19; Vo=20V vs. 19.7V, VGH_R/L=20V, VGL= -5V
Driving Current of GIP Outputs	I_{GOD}	1	-	-	mA	GIPIO0~GIPIO19; Vo=-5 vs. -4.7V , VGH_R/L=20V, VGL= -5V
Digital stand-by current	I_{VDDST}			(TBD)	uA	VDD=3.3V. All operating are stopped.
	I_{VCCST}			(TBD)	uA	VCC=1.5V. All operating are stopped.
Analog Stand-by Current	I_{AST}	-	-	(TBD)	uA	AVDD=10V. All operating are stopped.
Analog Operating Current	I_{AVDD}	-	(TBD)	(TBD)	mA	No load, F_{DCLK}=480Mbps, AVDD=10V, HAVDD=5V, Input pattern: 00h->FFh->00h->FFh

13.2. MIPI Interface DC Characteristic

Table 32. MIPI Interface DC characteristic

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
MIPI digital operation current	I_{VCCIF}	-	TBD	TBD	mA	VCC=VCC_IF=1.5V, Data Rate=500Mbps, Input pattern: 55h→AAh→55h→AAh
MIPI digital stand-by current	$I_{VCCIFST}$	-	200	-	uA	VCC_IF input current. All input signal are stopped.
MIPI Characteristics for High Speed Receiver						
Single-endedl input low voltage	V_{ILHS}	-40	-	-	mV	
Single-endedl input high voltage	V_{IHHS}	-	-	460	mV	
Common-mode voltage	V_{CMRXDC}	155	-	330	mV	
Differential input impedance	Z_{ID}	80	100	125	ohm	
Differential input high threshold	V_{IDTH}	-	-	70	mV	
Differential input low threshold	V_{IDTL}	70	-	-	mV	
MIPI Characteristics for Low Power Mode						
Pad signal voltage range	V_I	-50	-	1350	mV	
Ground shift	V_{GNDSH}	-50	-	50	mV	
Output low level	V_{OL}	-150	-	150	mV	
Output high level	V_{OH}	1.1	1.2	1.3	V	

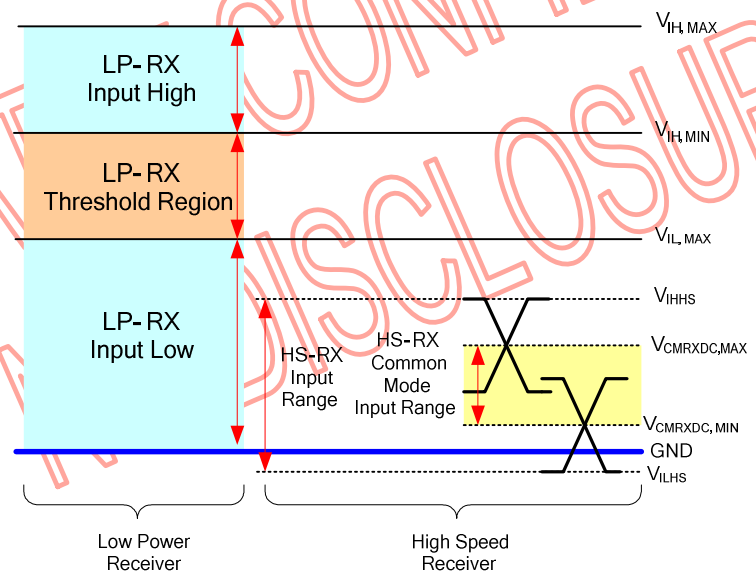


Figure 22. MIPI DC Diagram

14. AC Electrical Characteristics

14.1. Input AC Characteristic

Table 33. VDD/GRB AC characteristic

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD power source slew time	T_{POR}	-	-	20	ms	From 0V to 90% VDD
GRB active pulse width	T_{GRB}	1	-	-	ms	VDD = 3.3V
VDD resettle time	T_{RES}	1	-	-	s	

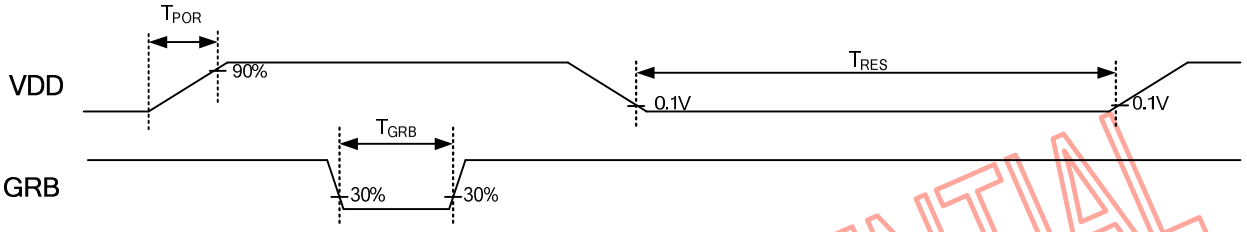


Figure 23. VDD/GRB timing

Table 34. I2C-Bus Timing

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Working Frequency	F_{CLK}	-	-	400	Khz	
I2C Clock Low	T_{CKL}	1200	-	-	ns	
I2C Clock High	T_{CKH}	600	-	-	ns	
I2C Data ring time	T_R	-	-	300	ns	
I2C Data falling time	T_F	-	-	300	ns	
I2C Data hold time	T_{DATHD}	0	-	900	ns	
I2C Data setup time	T_{DATSU}	100	-		ns	
I2C Start Condition hold time	T_{STAHD}	600	-	-	ns	
I2C Start Condition setup time	T_{STASU}	600	-	-	ns	
I2C Stop Condition setup time	T_{STPSU}	600	-	-	ns	
I2C Bus free time	$T_{BUSFREE}$	1200	-	-	ns	

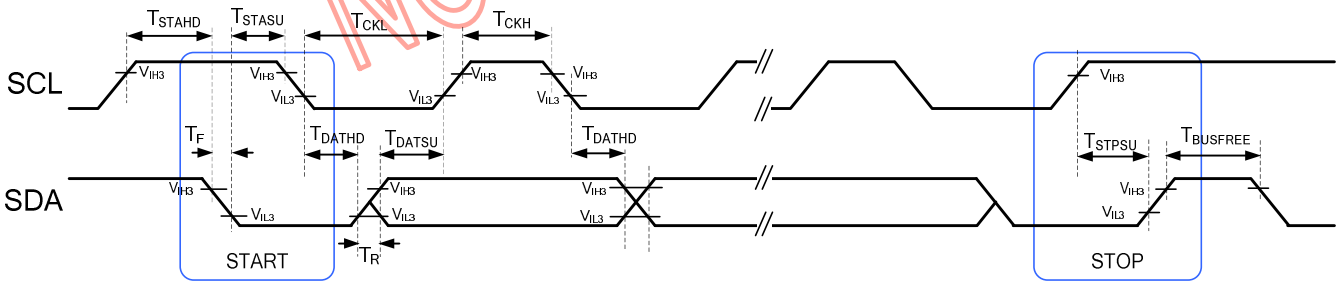


Figure 24. I2C-Bus timing

14.2. MIPI AC Characteristic

14.2.1. LP Transmission

Table 35. LP Transmitter AC Specifications

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min	Typ	Max	Units
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	25	ns
Pulse width of the LP exclusive-OR clock	$T_{LP-PULSE-TX}$	50	-	-	ns
Period of the LP exclusive-OR clock	$T_{LP-PER-TX}$	100	-	-	ns

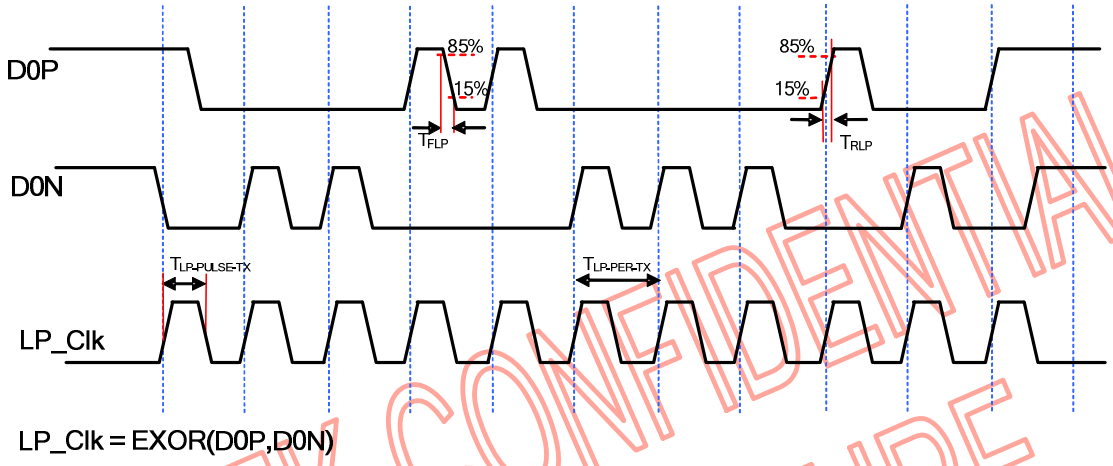


Figure 25. LP Transmitter Timing Definitions

14.2.2. High Speed Transmission

Table 36. Data-Clock Timing Specifications

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	1.0	-	12.5	ns
Data to Clock Setup Time	T_{SETUP}	0.3	-	-	UI_{INST}
Data to Clock Hold Time	T_{HOLD}	0.3	-	-	UI_{INST}

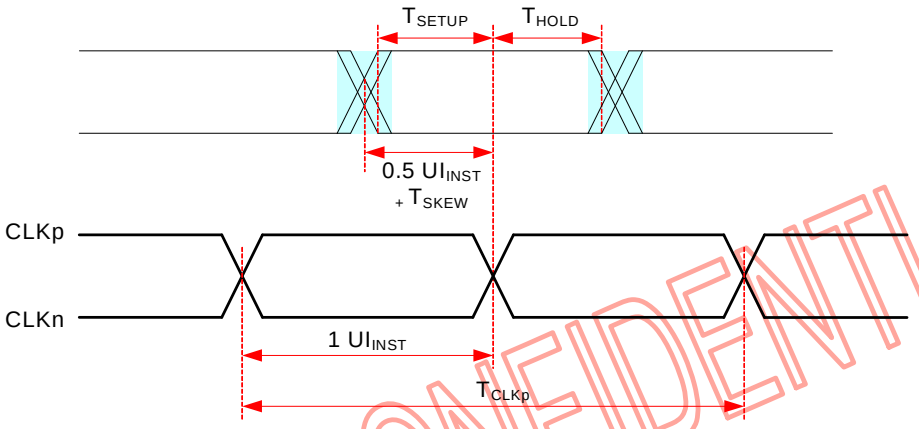


Figure 26. Data to Clock Timing Definitions

14.2.3. High-Speed Data Transmission in Bursts

Table 37. High-Speed Data Transmission Operation Timing Parameters

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40	-	55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns

Note:
1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. UI means Unit Interval, equal to one half HS clock period on the Clock Lane.
3. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

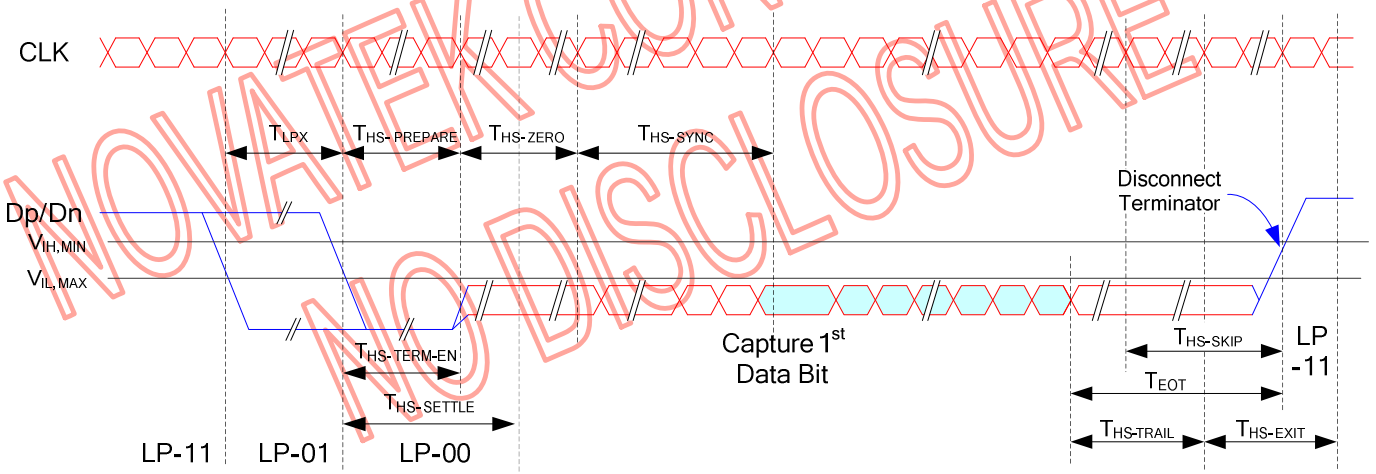


Figure 27. High-Speed Data Transmission in Bursts

14.2.4. High-Speed Clock Transmission

Table 38. Switching the Clock Lane Operation Timing Parameters

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

Note:
The DSI host processor shall support continuous clock on the Clock Lane for NT chip that require it, so the host processor needs to keep the HS serial clock running.

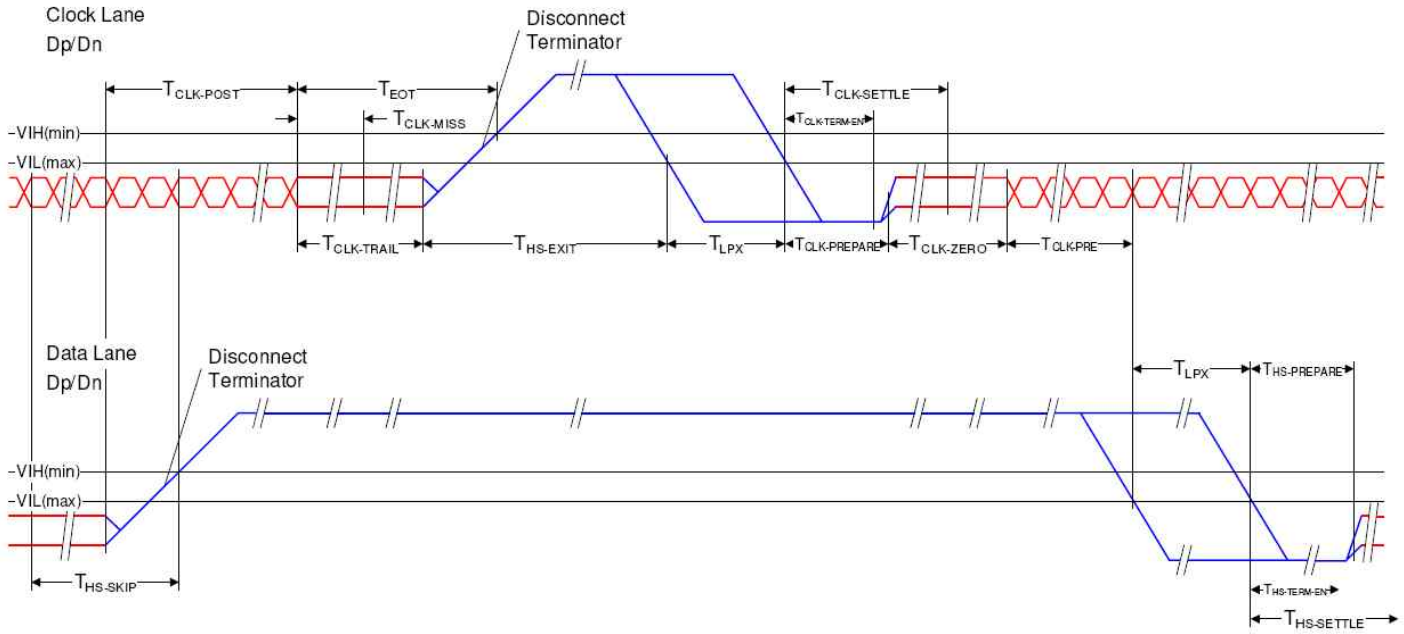
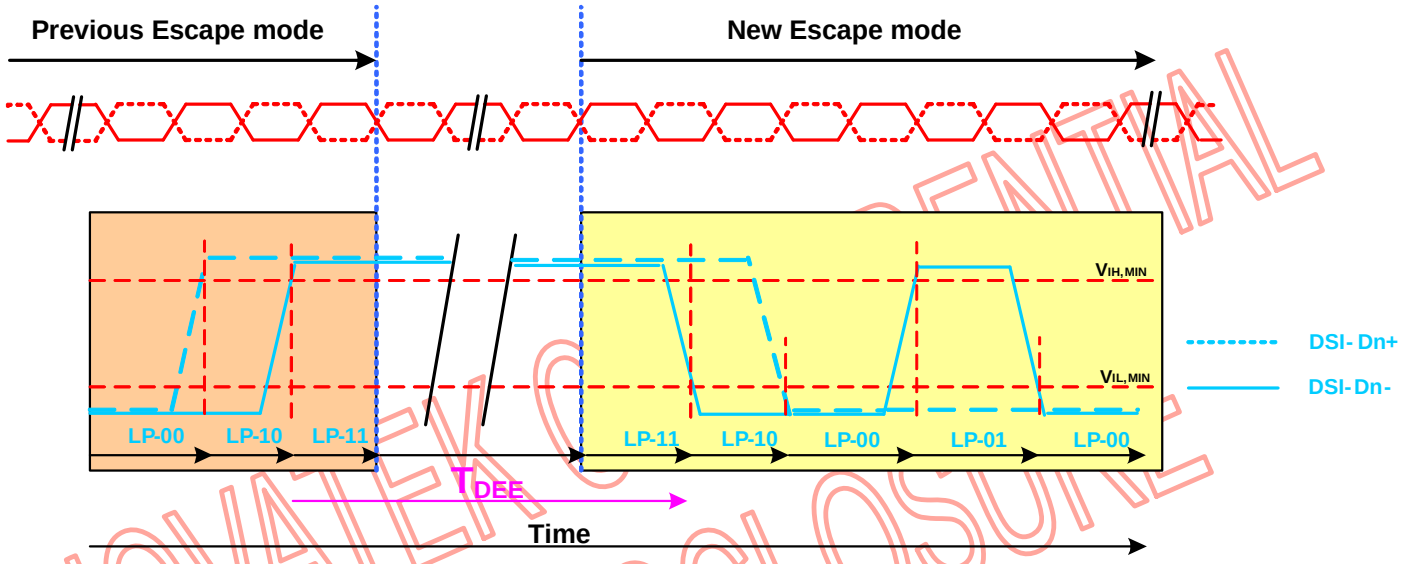


Figure 28. Switching the Clock Lane between Clock Transmission and Low-Power Mode

14.2.5. LP11 timing request between data transformation

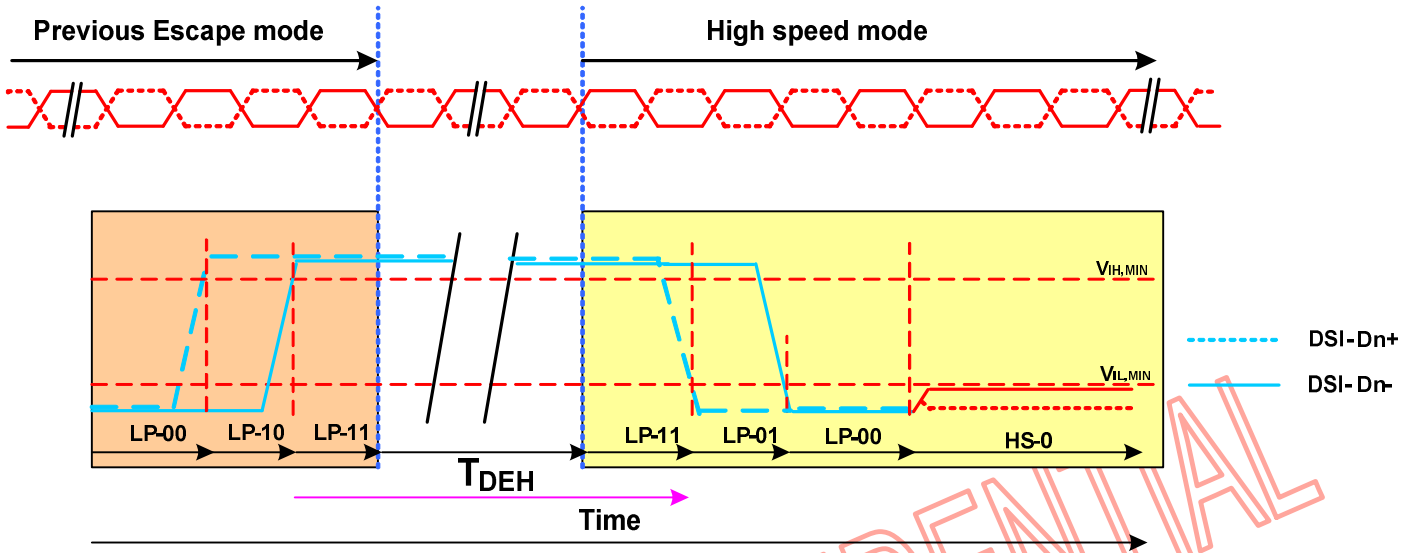
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP - LP, LP - HS, HS - LP, and HS – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP - LP command



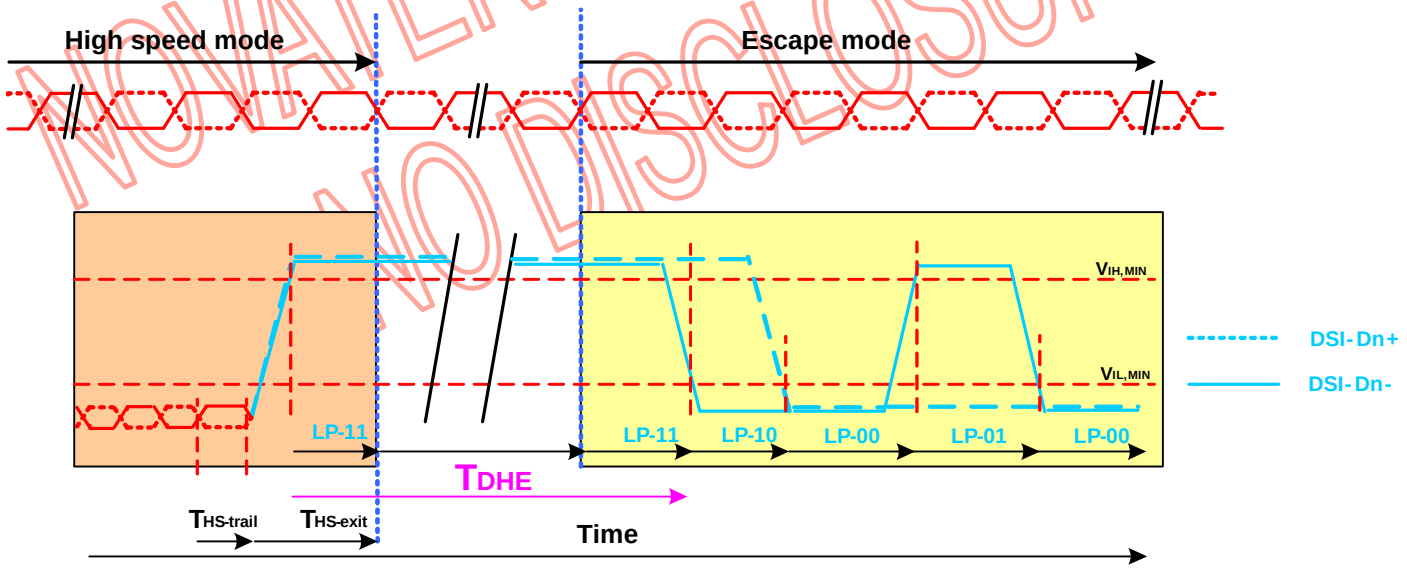
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the new Escape Mode Entry	T_{DEE}	150	-	-	ns

(2)Timing between LP - HS command



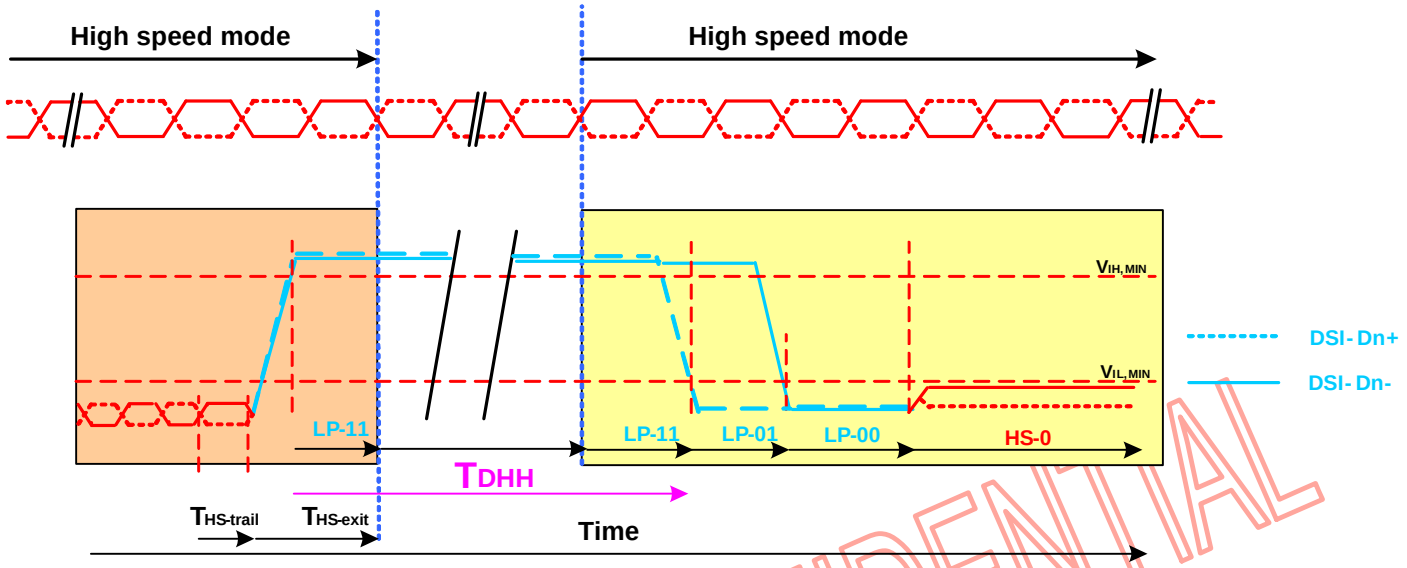
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Entering High Speed Mode	T_{DEH}	Max(150,32UI)	-	-	ns

(3)Timing between HS - LP command



Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Escape Mode Entry	T_{DHE}	Max(150,32UI)	-	-	ns

(4)Timing between HS - HS command



Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Entering High Speed Mode	T_{DHH}	Max(150,32UI)	-	-	ns

14.3. Output Timing Table

14.3.1. Digital output AC Timing

Table 39. Digital output AC Characteristic

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Time from Hsync to LD	T_{HLD}	-	252	-	UI	
LD Pulse Width	T_{WLD}	-	96	-	UI	
Time from STV rising to LD rising	T_{STVLD}	-	0.5	-	H	
Time from LD rising to STV falling	T_{LDSTV}	-	0.5	-	H	
Time from CKV rising to LD rising	T_{CKVLD}	-	36	-	UI	
Time from CKV rising to OEV falling	T_{WOEV1}	-	192	-	UI	1 port interface
Time from OEV rising to CKV rising	T_{WOEV2}	-	2016	-	UI	1 port interface
GPMOE pulse width	T_{GPMOE}	-	1344	-	UI	1 port interface

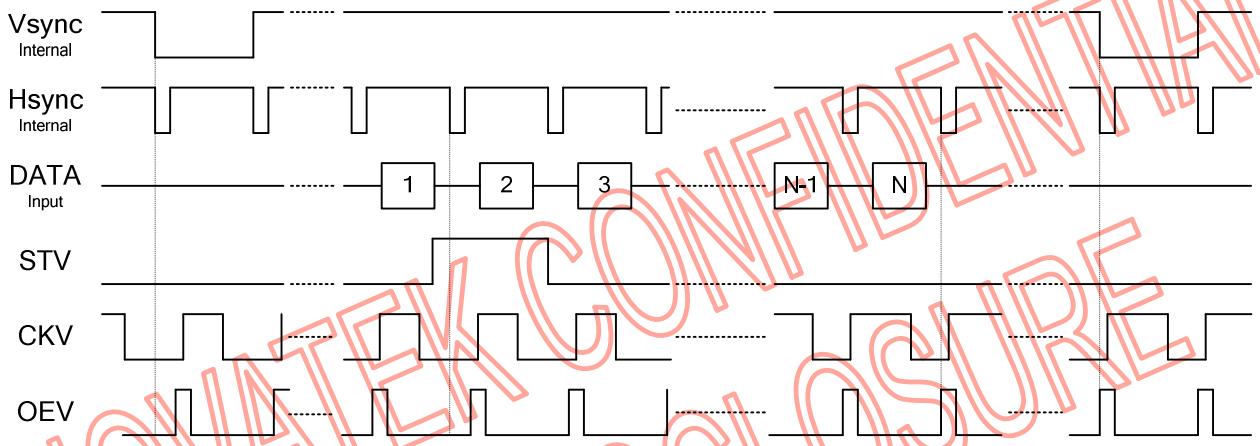


Figure 29. Vertical Output Timing

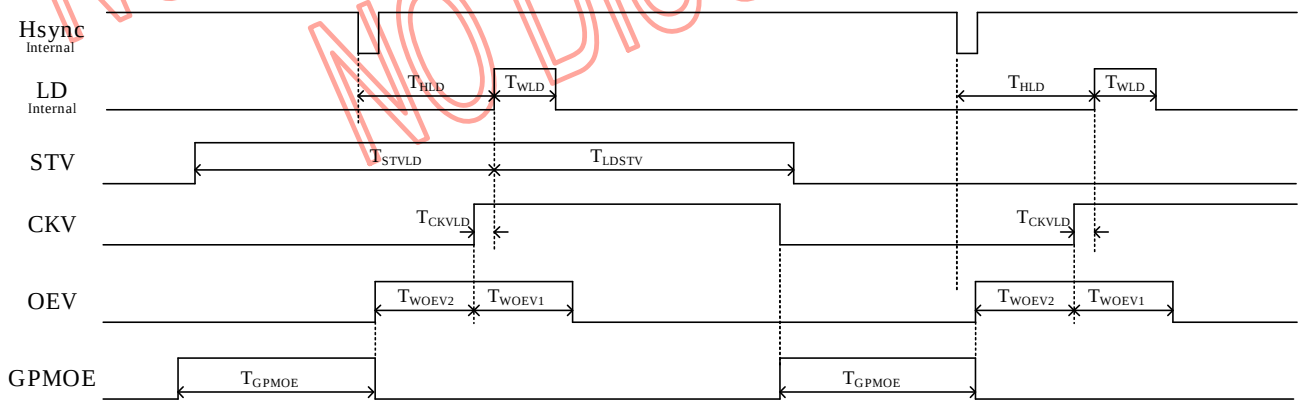


Figure 30. Gate output timing diagram

14.3.2. Analog output AC Timing

Table 40. Analog Output AC Characteristic

(VDD= 2.7V to 3.6V, AVDD= 7V to 10V, GND=AGND= 0V, TA= -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Source Driver output stable time	T_{SST}	-	-	4	us	
Repair OP output stable time	T_{RST}	-	-	6	us	

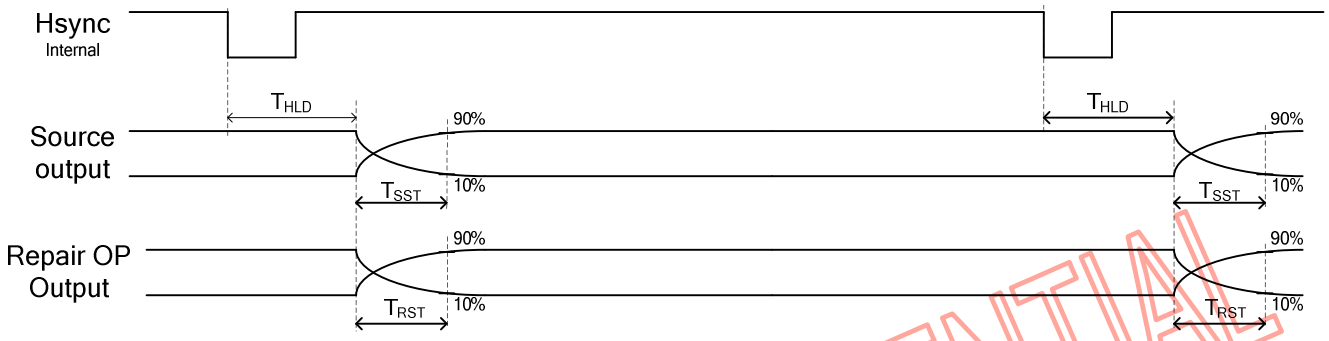


Figure 31. Source output timing chart

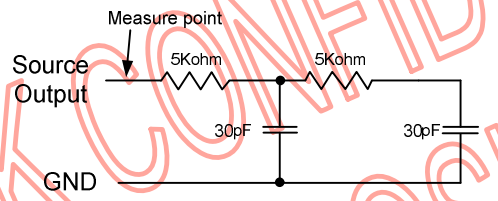


Figure 32. Source output loading condition

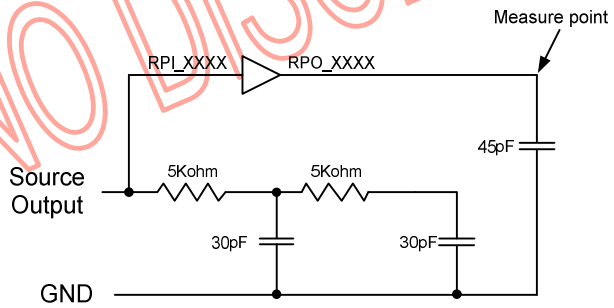


Figure 33. Repair OP output loading condition

15. Chip Outline Dimensions

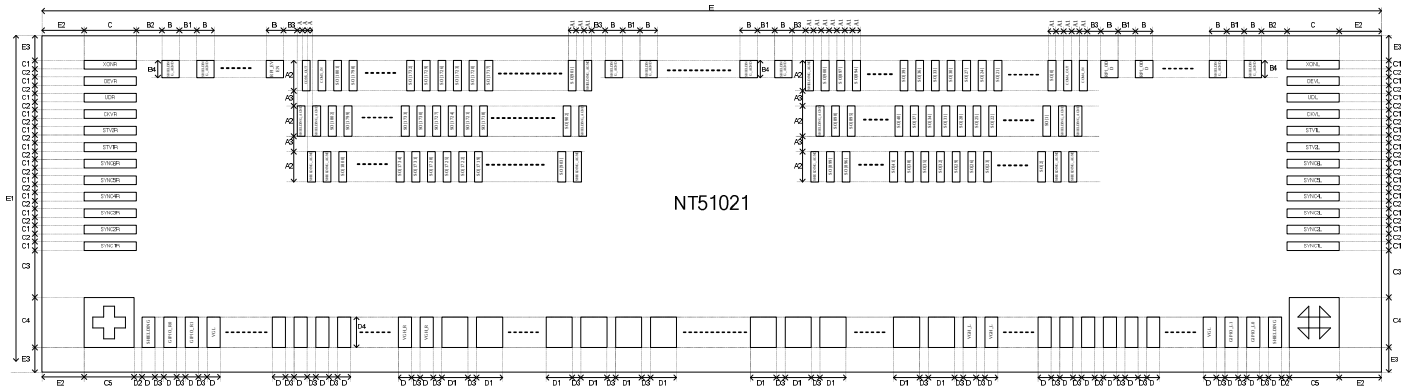


Figure 34. Chip Outline Dimensions

15.1. Alignment Mark

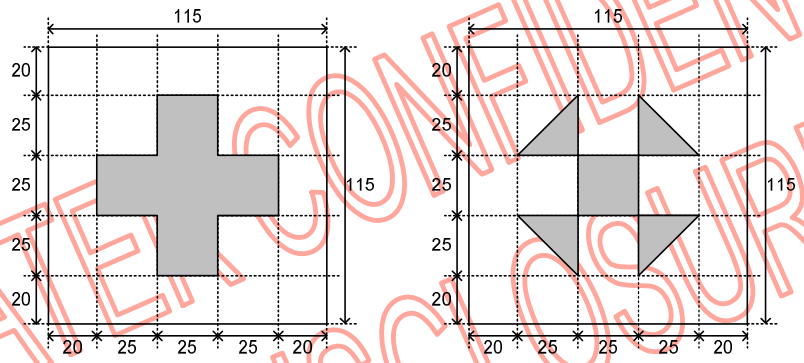


Figure 35. Alignment Mark

15.2. Pad Information

Table 41. Pad Dimension

Symbol	Dimension (um)	Symbol	Dimension (um)	Symbol	Dimension (um)
A	12	C	120	D	30
A1	18	C1	20	D1	60
A2	70	C2	18	D2	18
A3	35	C3	108	D3	20
		C4	115	D4	70
B	40	C5	115		
B1	40			E	28500(max)
B2	59			E1	775(max)
B3	31			E2	97(max)
B4	40			E3	57(max)

*Note: 1. Chip dimension includes scribe line.
2. Total bump area : 3910060um^2.

16. Pad Coordinate

Table 42. Pad Coordinate

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1	SHIELDING	-14005	-295.5	30	70
2	GIPIO_R0	-13955	-295.5	30	70
3	GIPIO_R1	-13905	-295.5	30	70
4	VGL	-13855	-295.5	30	70
5	VGL	-13805	-295.5	30	70
6	GIPIO_R2	-13755	-295.5	30	70
7	GIPIO_R3	-13705	-295.5	30	70
8	GIPIO_R4	-13655	-295.5	30	70
9	GIPIO_R5	-13605	-295.5	30	70
10	GIPIO_R6	-13555	-295.5	30	70
11	GIPIO_R7	-13505	-295.5	30	70
12	GIPIO_R8	-13455	-295.5	30	70
13	GIPIO_R9	-13405	-295.5	30	70
14	GIPIO_R10	-13355	-295.5	30	70
15	GIPIO_R11	-13305	-295.5	30	70
16	GIPIO_R12	-13255	-295.5	30	70
17	GIPIO_R13	-13205	-295.5	30	70
18	GIPIO_R14	-13155	-295.5	30	70
19	GIPIO_R15	-13105	-295.5	30	70
20	GIPIO_R16	-13055	-295.5	30	70
21	GIPIO_R17	-13005	-295.5	30	70
22	GIPIO_R18	-12955	-295.5	30	70
23	GIPIO_R19	-12905	-295.5	30	70
24	VGL	-12855	-295.5	30	70
25	VGL	-12805	-295.5	30	70
26	VGL	-12755	-295.5	30	70
27	VGL	-12705	-295.5	30	70
28	VGL	-12655	-295.5	30	70
29	VGL	-12605	-295.5	30	70
30	VGL	-12555	-295.5	30	70
31	VGL	-12505	-295.5	30	70
32	VGL	-12455	-295.5	30	70
33	VGH_R	-12405	-295.5	30	70
34	VGH_R	-12355	-295.5	30	70
35	VGH_R	-12305	-295.5	30	70
36	COMR2_IN	-12240	-295.5	60	70
37	COMR2_IN	-12160	-295.5	60	70
38	COMR1_IN	-12080	-295.5	60	70
39	COMR1_IN	-12000	-295.5	60	70
40	SHIELDING_GND	-11920	-295.5	60	70
41	TP8	-11840	-295.5	60	70
42	TP9	-11760	-295.5	60	70
43	TP10	-11680	-295.5	60	70
44	SHIELDING_GND	-11600	-295.5	60	70
45	RPO_EVEN	-11520	-295.5	60	70
46	RPO_EVEN	-11440	-295.5	60	70
47	RPO_EVEN	-11360	-295.5	60	70
48	TP11	-11280	-295.5	60	70
49	SCL	-11200	-295.5	60	70
50	SDA	-11120	-295.5	60	70
51	SHIELDING_GND	-11040	-295.5	60	70
52	I2C_SCL	-10960	-295.5	60	70
53	I2C_SDA	-10880	-295.5	60	70
54	PMU_EN	-10800	-295.5	60	70
55	STATE	-10720	-295.5	60	70
56	GRB	-10640	-295.5	60	70
57	STBYB	-10560	-295.5	60	70
58	SHIELDING_GND	-10480	-295.5	60	70
59	GPMOE	-10400	-295.5	60	70
60	LEDON	-10320	-295.5	60	70
61	LEDPWM	-10240	-295.5	60	70
62	TP_SYNC	-10160	-295.5	60	70
63	XON_IN	-10080	-295.5	60	70
64	ALSIN	-10000	-295.5	60	70
65	SHIELDING_GND	-9920	-295.5	60	70
66	RPEN_EVEN	-9840	-295.5	60	70
67	LED_EN	-9760	-295.5	60	70
68	TP12	-9680	-295.5	60	70
69	CMD_SEL	-9600	-295.5	60	70
70	SDLOC0	-9520	-295.5	60	70
71	SDLOC1	-9440	-295.5	60	70
72	SA2	-9360	-295.5	60	70
73	SA3	-9280	-295.5	60	70
74	RES0	-9200	-295.5	60	70
75	RES1	-9120	-295.5	60	70
76	TP35	-9040	-295.5	60	70
77	TP36	-8960	-295.5	60	70
78	PORT2B	-8880	-295.5	60	70
79	VCC	-8800	-295.5	60	70
80	VCC	-8720	-295.5	60	70
81	VCC	-8640	-295.5	60	70
82	VDD	-8560	-295.5	60	70
83	VDD	-8480	-295.5	60	70
84	VDD	-8400	-295.5	60	70
85	GND	-8320	-295.5	60	70
86	GND	-8240	-295.5	60	70
87	GND	-8160	-295.5	60	70
88	AVDD	-8080	-295.5	60	70
89	AVDD	-8000	-295.5	60	70
90	AVDD	-7920	-295.5	60	70
91	AVDD	-7840	-295.5	60	70
92	AVDD	-7760	-295.5	60	70
93	AVDD	-7680	-295.5	60	70
94	AGND	-7600	-295.5	60	70
95	AGND	-7520	-295.5	60	70
96	AGND	-7440	-295.5	60	70
97	AGND	-7360	-295.5	60	70
98	AGND1	-7280	-295.5	60	70
99	AGND1	-7200	-295.5	60	70
100	HAVDD	-7120	-295.5	60	70
101	HAVDD	-7040	-295.5	60	70
102	HAVDD	-6960	-295.5	60	70
103	HAVDD	-6880	-295.5	60	70
104	HAVDD	-6800	-295.5	60	70
105	HAVDD	-6720	-295.5	60	70
106	TP17	-6640	-295.5	60	70
107	TP18	-6560	-295.5	60	70
108	TP19	-6480	-295.5	60	70
109	TP20	-6400	-295.5	60	70
110	SHIELDING_AGND	-6320	-295.5	60	70
111	SHIELDING_AGND	-6240	-295.5	60	70
112	SHIELDING_AGND	-6160	-295.5	60	70
113	SHIELDING_AGND	-6080	-295.5	60	70
114	SHIELDING_AGND	-6000	-295.5	60	70
115	VCOMPI	-5920	-295.5	60	70
116	VCOMPI	-5840	-295.5	60	70
117	VCOMNI	-5760	-295.5	60	70
118	VCOMNI	-5680	-295.5	60	70
119	VCOMO	-5600	-295.5	60	70
120	VCOMO	-5520	-295.5	60	70
121	VCOMO	-5440	-295.5	60	70
122	VCOMO	-5360	-295.5	60	70
123	VCOMO	-5280	-295.5	60	70
124	VCOMO	-5200	-295.5	60	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
125	VCOM_EN	-5120	-295.5	60	70
126	VCOM_UGB	-5040	-295.5	60	70
127	HAOP_EN	-4960	-295.5	60	70
128	SHIELDING_AGND	-4880	-295.5	60	70
129	HAOP	-4800	-295.5	60	70
130	HAOP	-4720	-295.5	60	70
131	HAOP	-4640	-295.5	60	70
132	HAOP	-4560	-295.5	60	70
133	HAOP	-4480	-295.5	60	70
134	HAOP	-4400	-295.5	60	70
135	SHIELDING_AGND	-4320	-295.5	60	70
136	VQH	-4240	-295.5	60	70
137	VQH	-4160	-295.5	60	70
138	VQL	-4080	-295.5	60	70
139	VQL	-4000	-295.5	60	70
140	VCC	-3920	-295.5	60	70
141	VCC	-3840	-295.5	60	70
142	VCC	-3760	-295.5	60	70
143	VCC_IF	-3680	-295.5	60	70
144	VCC_IF	-3600	-295.5	60	70
145	VCC_IF	-3520	-295.5	60	70
146	GND	-3440	-295.5	60	70
147	GND	-3360	-295.5	60	70
148	GND	-3280	-295.5	60	70
149	GND_IF	-3200	-295.5	60	70
150	GND_IF	-3120	-295.5	60	70
151	GND_IF	-3040	-295.5	60	70
152	D3N	-2960	-295.5	60	70
153	D3N	-2880	-295.5	60	70
154	D3P	-2800	-295.5	60	70
155	D3P	-2720	-295.5	60	70
156	DASH	-2640	-295.5	60	70
157	D2N	-2560	-295.5	60	70
158	D2N	-2480	-295.5	60	70
159	D2P	-2400	-295.5	60	70
160	D2P	-2320	-295.5	60	70
161	DASH	-2240	-295.5	60	70
162	CLKN	-2160	-295.5	60	70
163	CLKN	-2080	-295.5	60	70
164	CLKP	-2000	-295.5	60	70
165	CLKP	-1920	-295.5	60	70
166	DASH	-1840	-295.5	60	70
167	D1N	-1760	-295.5	60	70
168	D1N	-1680	-295.5	60	70
169	D1P	-1600	-295.5	60	70
170	D1P	-1520	-295.5	60	70
171	DASH	-1440	-295.5	60	70
172	D0N	-1360	-295.5	60	70
173	D0N	-1280	-295.5	60	70
174	D0P	-1200	-295.5	60	70
175	D0P	-1120	-295.5	60	70
176	GND_IF	-1040	-295.5	60	70
177	GND_IF	-960	-295.5	60	70
178	GND_IF	-880	-295.5	60	70
179	GND	-800	-295.5	60	70
180	GND	-720	-295.5	60	70
181	GND	-640	-295.5	60	70
182	VCC_IF	-560	-295.5	60	70
183	VCC_IF	-480	-295.5	60	70
184	VCC_IF	-400	-295.5	60	70
185	VCC	-320	-295.5	60	70
186	VCC	-240	-295.5	60	70
187	VCC	-160	-295.5	60	70
188	SHIELDING_GND	-80	-295.5	60	70
189	SHIELDING_GND	0	-295.5	60	70
190	SHIELDING_GND	80	-295.5	60	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
191	SHIELDING_GND	160	-295.5	60	70
192	SHIELDING_GND	240	-295.5	60	70
193	SHIELDING_GND	320	-295.5	60	70
194	SHIELDING_GND	400	-295.5	60	70
195	SHIELDING_GND	480	-295.5	60	70
196	SHIELDING_GND	560	-295.5	60	70
197	SHIELDING_GND	640	-295.5	60	70
198	SHIELDING_GND	720	-295.5	60	70
199	SHIELDING_GND	800	-295.5	60	70
200	SHIELDING_GND	880	-295.5	60	70
201	SHIELDING_GND	960	-295.5	60	70
202	SHIELDING_GND	1040	-295.5	60	70
203	SHIELDING_GND	1120	-295.5	60	70
204	SHIELDING_GND	1200	-295.5	60	70
205	SHIELDING_GND	1280	-295.5	60	70
206	SHIELDING_GND	1360	-295.5	60	70
207	SHIELDING_GND	1440	-295.5	60	70
208	SHIELDING_GND	1520	-295.5	60	70
209	SHIELDING_GND	1600	-295.5	60	70
210	SHIELDING_GND	1680	-295.5	60	70
211	SHIELDING_GND	1760	-295.5	60	70
212	SHIELDING_GND	1840	-295.5	60	70
213	SHIELDING_GND	1920	-295.5	60	70
214	SHIELDING_GND	2000	-295.5	60	70
215	SHIELDING_GND	2080	-295.5	60	70
216	SHIELDING_GND	2160	-295.5	60	70
217	SHIELDING_GND	2240	-295.5	60	70
218	SHIELDING_GND	2320	-295.5	60	70
219	SHIELDING_GND	2400	-295.5	60	70
220	SHIELDING_GND	2480	-295.5	60	70
221	SHIELDING_GND	2560	-295.5	60	70
222	SHIELDING_GND	2640	-295.5	60	70
223	SHIELDING_GND	2720	-295.5	60	70
224	SHIELDING_GND	2800	-295.5	60	70
225	SHIELDING_GND	2880	-295.5	60	70
226	VLPH	2960	-295.5	60	70
227	VLPH	3040	-295.5	60	70
228	VLPH	3120	-295.5	60	70
229	VDD	3200	-295.5	60	70
230	VDD	3280	-295.5	60	70
231	VDD	3360	-295.5	60	70
232	VCC_EN	3440	-295.5	60	70
233	VCC	3520	-295.5	60	70
234	VCC	3600	-295.5	60	70
235	VCC	3680	-295.5	60	70
236	GND	3760	-295.5	60	70
237	GND	3840	-295.5	60	70
238	GND	3920	-295.5	60	70
239	SHIELDING_AGND	4000	-295.5	60	70
240	SHIELDING_AGND	4080	-295.5	60	70
241	TP21	4160	-295.5	60	70
242	V1	4240	-295.5	60	70
243	V4	4320	-295.5	60	70
244	V7	4400	-295.5	60	70
245	V8	4480	-295.5	60	70
246	V11	4560	-295.5	60	70
247	V14	4640	-295.5	60	70
248	SHIELDING_AGND	4720	-295.5	60	70
249	SHIELDING_AGND	4800	-295.5	60	70
250	AVDD	4880	-295.5	60	70
251	AVDD	4960	-295.5	60	70
252	AVDD	5040	-295.5	60	70
253	AVDD	5120	-295.5	60	70
254	AVDD	5200	-295.5	60	70
255	AVDD	5280	-295.5	60	70
256	AGND1	5360	-295.5	60	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
257	AGND1	5440	-295.5	60	70
258	AGND	5520	-295.5	60	70
259	AGND	5600	-295.5	60	70
260	AGND	5680	-295.5	60	70
261	AGND	5760	-295.5	60	70
262	HAVDD	5840	-295.5	60	70
263	HAVDD	5920	-295.5	60	70
264	HAVDD	6000	-295.5	60	70
265	HAVDD	6080	-295.5	60	70
266	HAVDD	6160	-295.5	60	70
267	HAVDD	6240	-295.5	60	70
268	TM0	6320	-295.5	60	70
269	TM1	6400	-295.5	60	70
270	TM2	6480	-295.5	60	70
271	TM3	6560	-295.5	60	70
272	TM4	6640	-295.5	60	70
273	TM5	6720	-295.5	60	70
274	TM6	6800	-295.5	60	70
275	TM7	6880	-295.5	60	70
276	SHIELDING_GND	6960	-295.5	60	70
277	TP0	7040	-295.5	60	70
278	TP1	7120	-295.5	60	70
279	SHIELDING_GND	7200	-295.5	60	70
280	TP2	7280	-295.5	60	70
281	TP3	7360	-295.5	60	70
282	SHIELDING_GND	7440	-295.5	60	70
283	TP4	7520	-295.5	60	70
284	TP5	7600	-295.5	60	70
285	SHIELDING_GND	7680	-295.5	60	70
286	TP6	7760	-295.5	60	70
287	TP7	7840	-295.5	60	70
288	SHIELDING_GND	7920	-295.5	60	70
289	RTERM_EN	8000	-295.5	60	70
290	RTERM[0]	8080	-295.5	60	70
291	RTERM[1]	8160	-295.5	60	70
292	BISTAUTO	8240	-295.5	60	70
293	BISTB	8320	-295.5	60	70
294	BIST_CKSL	8400	-295.5	60	70
295	SHIELDING_GND	8480	-295.5	60	70
296	BIST_CLK	8560	-295.5	60	70
297	SHLR	8640	-295.5	60	70
298	UPDNB	8720	-295.5	60	70
299	CABC_ENB[0]	8800	-295.5	60	70
300	CABC_ENB[1]	8880	-295.5	60	70
301	TP30	8960	-295.5	60	70
302	CE_ENB	9040	-295.5	60	70
303	TP31	9120	-295.5	60	70
304	LSTVB	9200	-295.5	60	70
305	INVSEL[0]	9280	-295.5	60	70
306	INVSEL[1]	9360	-295.5	60	70
307	OPDRV0	9440	-295.5	60	70
308	OPDRV1	9520	-295.5	60	70
309	BLKINSER	9600	-295.5	60	70
310	ZTYPE	9680	-295.5	60	70
311	ZIGZAG	9760	-295.5	60	70
312	TP34	9840	-295.5	60	70
313	NBW	9920	-295.5	60	70
314	TP13	10000	-295.5	60	70
315	TP14	10080	-295.5	60	70
316	TP15	10160	-295.5	60	70
317	TP16	10240	-295.5	60	70
318	TP37	10320	-295.5	60	70
319	TP38	10400	-295.5	60	70
320	GIP_EN	10480	-295.5	60	70
321	GIP_SEL[0]	10560	-295.5	60	70
322	GIP_SEL[1]	10640	-295.5	60	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
323	GIP_SEL[2]	10720	-295.5	60	70
324	GIP_SEL[3]	10800	-295.5	60	70
325	RPEN_ODD	10880	-295.5	60	70
326	COM3_IN	10960	-295.5	60	70
327	COM3_OUT	11040	-295.5	60	70
328	RPO_ODD	11120	-295.5	60	70
329	RPO_ODD	11200	-295.5	60	70
330	RPO_ODD	11280	-295.5	60	70
331	SHIELDING_GND	11360	-295.5	60	70
332	TP39	11440	-295.5	60	70
333	TP40	11520	-295.5	60	70
334	TP41	11600	-295.5	60	70
335	SHIELDING_GND	11680	-295.5	60	70
336	COML2_IN	11760	-295.5	60	70
337	COML2_IN	11840	-295.5	60	70
338	COML1_IN	11920	-295.5	60	70
339	COML1_IN	12000	-295.5	60	70
340	VPP_MTP	12080	-295.5	60	70
341	VPP_MTP	12160	-295.5	60	70
342	VPP_MTP	12240	-295.5	60	70
343	VGH_L	12305	-295.5	30	70
344	VGH_L	12355	-295.5	30	70
345	VGH_L	12405	-295.5	30	70
346	VGL	12455	-295.5	30	70
347	VGL	12505	-295.5	30	70
348	VGL	12555	-295.5	30	70
349	VGL	12605	-295.5	30	70
350	VGL	12655	-295.5	30	70
351	VGL	12705	-295.5	30	70
352	VGL	12755	-295.5	30	70
353	VGL	12805	-295.5	30	70
354	VGL	12855	-295.5	30	70
355	GIPIO_L19	12905	-295.5	30	70
356	GIPIO_L18	12955	-295.5	30	70
357	GIPIO_L17	13005	-295.5	30	70
358	GIPIO_L16	13055	-295.5	30	70
359	GIPIO_L15	13105	-295.5	30	70
360	GIPIO_L14	13155	-295.5	30	70
361	GIPIO_L13	13205	-295.5	30	70
362	GIPIO_L12	13255	-295.5	30	70
363	GIPIO_L11	13305	-295.5	30	70
364	GIPIO_L10	13355	-295.5	30	70
365	GIPIO_L9	13405	-295.5	30	70
366	GIPIO_L8	13455	-295.5	30	70
367	GIPIO_L7	13505	-295.5	30	70
368	GIPIO_L6	13555	-295.5	30	70
369	GIPIO_L5	13605	-295.5	30	70
370	GIPIO_L4	13655	-295.5	30	70
371	GIPIO_L3	13705	-295.5	30	70
372	GIPIO_L2	13755	-295.5	30	70
373	VGL	13805	-295.5	30	70
374	VGL	13855	-295.5	30	70
375	GIPIO_L1	13905	-295.5	30	70
376	GIPIO_L0	13955	-295.5	30	70
377	SHIELDING	14005	-295.5	30	70
378	SYNC1L	14093	-97.5	120	20
379	SYNC2L	14093	-59.5	120	20
380	SYNC3L	14093	-21.5	120	20
381	SYNC4L	14093	16.5	120	20
382	SYNC5L	14093	54.5	120	20
383	SYNC6L	14093	92.5	120	20
384	STV2L	14093	130.5	120	20
385	STV1L	14093	168.5	120	20
386	CKVL	14093	206.5	120	20
387	UDL	14093	244.5	120	20
388	OEVL	14093	282.5	120	20

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
389	XONL	14093	320.5	120	20
390	SHIELDING_AGND	13954	310.5	40	40
391	SHIELDING_AGND	13874	310.5	40	40
392	SHIELDING_AGND	13794	310.5	40	40
393	SHIELDING_AGND	13714	310.5	40	40
394	SHIELDING_AGND	13634	310.5	40	40
395	SHIELDING_AGND	13554	310.5	40	40
396	SHIELDING_AGND	13474	310.5	40	40
397	SHIELDING_AGND	13394	310.5	40	40
398	SHIELDING_AGND	13314	310.5	40	40
399	SHIELDING_AGND	13234	310.5	40	40
400	COML1_OUT	13154	310.5	40	40
401	COML1_OUT	13074	310.5	40	40
402	COML2_OUT	12994	310.5	40	40
403	COML2_OUT	12914	310.5	40	40
404	RPI_ODD	12834	310.5	40	40
405	RPI_ODD	12754	310.5	40	40
406	COM4_IN	12694	295.5	18	70
407	SHIELDING_AGND	12682	190.5	18	70
408	SHIELDING_AGND	12670	85.5	18	70
409	COM4_OUT	12658	295.5	18	70
410	SHIELDING_AGND	12646	190.5	18	70
411	SHIELDING_AGND	12634	85.5	18	70
412	SO[0]	12622	295.5	18	70
413	SO[1]	12610	190.5	18	70
414	SO[2]	12598	85.5	18	70
415	SO[3]	12586	295.5	18	70
416	SO[4]	12574	190.5	18	70
417	SO[5]	12562	85.5	18	70
418	SO[6]	12550	295.5	18	70
419	SO[7]	12538	190.5	18	70
420	SO[8]	12526	85.5	18	70
421	SO[9]	12514	295.5	18	70
422	SO[10]	12502	190.5	18	70
423	SO[11]	12490	85.5	18	70
424	SO[12]	12478	295.5	18	70
425	SO[13]	12466	190.5	18	70
426	SO[14]	12454	85.5	18	70
427	SO[15]	12442	295.5	18	70
428	SO[16]	12430	190.5	18	70
429	SO[17]	12418	85.5	18	70
430	SO[18]	12406	295.5	18	70
431	SO[19]	12394	190.5	18	70
432	SO[20]	12382	85.5	18	70
433	SO[21]	12370	295.5	18	70
434	SO[22]	12358	190.5	18	70
435	SO[23]	12346	85.5	18	70
436	SO[24]	12334	295.5	18	70
437	SO[25]	12322	190.5	18	70
438	SO[26]	12310	85.5	18	70
439	SO[27]	12298	295.5	18	70
440	SO[28]	12286	190.5	18	70
441	SO[29]	12274	85.5	18	70
442	SO[30]	12262	295.5	18	70
443	SO[31]	12250	190.5	18	70
444	SO[32]	12238	85.5	18	70
445	SO[33]	12226	295.5	18	70
446	SO[34]	12214	190.5	18	70
447	SO[35]	12202	85.5	18	70
448	SO[36]	12190	295.5	18	70
449	SO[37]	12178	190.5	18	70
450	SO[38]	12166	85.5	18	70
451	SO[39]	12154	295.5	18	70
452	SO[40]	12142	190.5	18	70
453	SO[41]	12130	85.5	18	70
454	SO[42]	12118	295.5	18	70
455	SO[43]	12106	190.5	18	70
456	SO[44]	12094	85.5	18	70
457	SO[45]	12082	295.5	18	70
458	SO[46]	12070	190.5	18	70
459	SO[47]	12058	85.5	18	70
460	SO[48]	12046	295.5	18	70
461	SO[49]	12034	190.5	18	70
462	SO[50]	12022	85.5	18	70
463	SO[51]	12010	295.5	18	70
464	SO[52]	11998	190.5	18	70
465	SO[53]	11986	85.5	18	70
466	SO[54]	11974	295.5	18	70
467	SO[55]	11962	190.5	18	70
468	SO[56]	11950	85.5	18	70
469	SO[57]	11938	295.5	18	70
470	SO[58]	11926	190.5	18	70
471	SO[59]	11914	85.5	18	70
472	SO[60]	11902	295.5	18	70
473	SO[61]	11890	190.5	18	70
474	SO[62]	11878	85.5	18	70
475	SO[63]	11866	295.5	18	70
476	SO[64]	11854	190.5	18	70
477	SO[65]	11842	85.5	18	70
478	SO[66]	11830	295.5	18	70
479	SO[67]	11818	190.5	18	70
480	SO[68]	11806	85.5	18	70
481	SO[69]	11794	295.5	18	70
482	SO[70]	11782	190.5	18	70
483	SO[71]	11770	85.5	18	70
484	SO[72]	11758	295.5	18	70
485	SO[73]	11746	190.5	18	70
486	SO[74]	11734	85.5	18	70
487	SO[75]	11722	295.5	18	70
488	SO[76]	11710	190.5	18	70
489	SO[77]	11698	85.5	18	70
490	SO[78]	11686	295.5	18	70
491	SO[79]	11674	190.5	18	70
492	SO[80]	11662	85.5	18	70
493	SO[81]	11650	295.5	18	70
494	SO[82]	11638	190.5	18	70
495	SO[83]	11626	85.5	18	70
496	SO[84]	11614	295.5	18	70
497	SO[85]	11602	190.5	18	70
498	SO[86]	11590	85.5	18	70
499	SO[87]	11578	295.5	18	70
500	SO[88]	11566	190.5	18	70
501	SO[89]	11554	85.5	18	70
502	SO[90]	11542	295.5	18	70
503	SO[91]	11530	190.5	18	70
504	SO[92]	11518	85.5	18	70
505	SO[93]	11506	295.5	18	70
506	SO[94]	11494	190.5	18	70
507	SO[95]	11482	85.5	18	70
508	SO[96]	11470	295.5	18	70
509	SO[97]	11458	190.5	18	70
510	SO[98]	11446	85.5	18	70
511	SO[99]	11434	295.5	18	70
512	SO[100]	11422	190.5	18	70
513	SO[101]	11410	85.5	18	70
514	SO[102]	11398	295.5	18	70
515	SO[103]	11386	190.5	18	70
516	SO[104]	11374	85.5	18	70
517	SO[105]	11362	295.5	18	70
518	SO[106]	11350	190.5	18	70
519	SO[107]	11338	85.5	18	70
520	SO[108]	11326	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
521	SO[109]	11314	190.5	18	70
522	SO[110]	11302	85.5	18	70
523	SO[111]	11290	295.5	18	70
524	SO[112]	11278	190.5	18	70
525	SO[113]	11266	85.5	18	70
526	SO[114]	11254	295.5	18	70
527	SO[115]	11242	190.5	18	70
528	SO[116]	11230	85.5	18	70
529	SO[117]	11218	295.5	18	70
530	SO[118]	11206	190.5	18	70
531	SO[119]	11194	85.5	18	70
532	SO[120]	11182	295.5	18	70
533	SO[121]	11170	190.5	18	70
534	SO[122]	11158	85.5	18	70
535	SO[123]	11146	295.5	18	70
536	SO[124]	11134	190.5	18	70
537	SO[125]	11122	85.5	18	70
538	SO[126]	11110	295.5	18	70
539	SO[127]	11098	190.5	18	70
540	SO[128]	11086	85.5	18	70
541	SO[129]	11074	295.5	18	70
542	SO[130]	11062	190.5	18	70
543	SO[131]	11050	85.5	18	70
544	SO[132]	11038	295.5	18	70
545	SO[133]	11026	190.5	18	70
546	SO[134]	11014	85.5	18	70
547	SO[135]	11002	295.5	18	70
548	SO[136]	10990	190.5	18	70
549	SO[137]	10978	85.5	18	70
550	SO[138]	10966	295.5	18	70
551	SO[139]	10954	190.5	18	70
552	SO[140]	10942	85.5	18	70
553	SO[141]	10930	295.5	18	70
554	SO[142]	10918	190.5	18	70
555	SO[143]	10906	85.5	18	70
556	SO[144]	10894	295.5	18	70
557	SO[145]	10882	190.5	18	70
558	SO[146]	10870	85.5	18	70
559	SO[147]	10858	295.5	18	70
560	SO[148]	10846	190.5	18	70
561	SO[149]	10834	85.5	18	70
562	SO[150]	10822	295.5	18	70
563	SO[151]	10810	190.5	18	70
564	SO[152]	10798	85.5	18	70
565	SO[153]	10786	295.5	18	70
566	SO[154]	10774	190.5	18	70
567	SO[155]	10762	85.5	18	70
568	SO[156]	10750	295.5	18	70
569	SO[157]	10738	190.5	18	70
570	SO[158]	10726	85.5	18	70
571	SO[159]	10714	295.5	18	70
572	SO[160]	10702	190.5	18	70
573	SO[161]	10690	85.5	18	70
574	SO[162]	10678	295.5	18	70
575	SO[163]	10666	190.5	18	70
576	SO[164]	10654	85.5	18	70
577	SO[165]	10642	295.5	18	70
578	SO[166]	10630	190.5	18	70
579	SO[167]	10618	85.5	18	70
580	SO[168]	10606	295.5	18	70
581	SO[169]	10594	190.5	18	70
582	SO[170]	10582	85.5	18	70
583	SO[171]	10570	295.5	18	70
584	SO[172]	10558	190.5	18	70
585	SO[173]	10546	85.5	18	70
586	SO[174]	10534	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
587	SO[175]	10522	190.5	18	70
588	SO[176]	10510	85.5	18	70
589	SO[177]	10498	295.5	18	70
590	SO[178]	10486	190.5	18	70
591	SO[179]	10474	85.5	18	70
592	SO[180]	10462	295.5	18	70
593	SO[181]	10450	190.5	18	70
594	SO[182]	10438	85.5	18	70
595	SO[183]	10426	295.5	18	70
596	SO[184]	10414	190.5	18	70
597	SO[185]	10402	85.5	18	70
598	SO[186]	10390	295.5	18	70
599	SO[187]	10378	190.5	18	70
600	SO[188]	10366	85.5	18	70
601	SO[189]	10354	295.5	18	70
602	SO[190]	10342	190.5	18	70
603	SO[191]	10330	85.5	18	70
604	SO[192]	10318	295.5	18	70
605	SO[193]	10306	190.5	18	70
606	SO[194]	10294	85.5	18	70
607	SO[195]	10282	295.5	18	70
608	SO[196]	10270	190.5	18	70
609	SO[197]	10258	85.5	18	70
610	SO[198]	10246	295.5	18	70
611	SO[199]	10234	190.5	18	70
612	SO[200]	10222	85.5	18	70
613	SO[201]	10210	295.5	18	70
614	SO[202]	10198	190.5	18	70
615	SO[203]	10186	85.5	18	70
616	SO[204]	10174	295.5	18	70
617	SO[205]	10162	190.5	18	70
618	SO[206]	10150	85.5	18	70
619	SO[207]	10138	295.5	18	70
620	SO[208]	10126	190.5	18	70
621	SO[209]	10114	85.5	18	70
622	SO[210]	10102	295.5	18	70
623	SO[211]	10090	190.5	18	70
624	SO[212]	10078	85.5	18	70
625	SO[213]	10066	295.5	18	70
626	SO[214]	10054	190.5	18	70
627	SO[215]	10042	85.5	18	70
628	SO[216]	10030	295.5	18	70
629	SO[217]	10018	190.5	18	70
630	SO[218]	10006	85.5	18	70
631	SO[219]	9994	295.5	18	70
632	SO[220]	9982	190.5	18	70
633	SO[221]	9970	85.5	18	70
634	SO[222]	9958	295.5	18	70
635	SO[223]	9946	190.5	18	70
636	SO[224]	9934	85.5	18	70
637	SO[225]	9922	295.5	18	70
638	SO[226]	9910	190.5	18	70
639	SO[227]	9898	85.5	18	70
640	SO[228]	9886	295.5	18	70
641	SO[229]	9874	190.5	18	70
642	SO[230]	9862	85.5	18	70
643	SO[231]	9850	295.5	18	70
644	SO[232]	9838	190.5	18	70
645	SO[233]	9826	85.5	18	70
646	SO[234]	9814	295.5	18	70
647	SO[235]	9802	190.5	18	70
648	SO[236]	9790	85.5	18	70
649	SO[237]	9778	295.5	18	70
650	SO[238]	9766	190.5	18	70
651	SO[239]	9754	85.5	18	70
652	SO[240]	9742	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
653	SO[241]	9730	190.5	18	70
654	SO[242]	9718	85.5	18	70
655	SO[243]	9706	295.5	18	70
656	SO[244]	9694	190.5	18	70
657	SO[245]	9682	85.5	18	70
658	SO[246]	9670	295.5	18	70
659	SO[247]	9658	190.5	18	70
660	SO[248]	9646	85.5	18	70
661	SO[249]	9634	295.5	18	70
662	SO[250]	9622	190.5	18	70
663	SO[251]	9610	85.5	18	70
664	SO[252]	9598	295.5	18	70
665	SO[253]	9586	190.5	18	70
666	SO[254]	9574	85.5	18	70
667	SO[255]	9562	295.5	18	70
668	SO[256]	9550	190.5	18	70
669	SO[257]	9538	85.5	18	70
670	SO[258]	9526	295.5	18	70
671	SO[259]	9514	190.5	18	70
672	SO[260]	9502	85.5	18	70
673	SO[261]	9490	295.5	18	70
674	SO[262]	9478	190.5	18	70
675	SO[263]	9466	85.5	18	70
676	SO[264]	9454	295.5	18	70
677	SO[265]	9442	190.5	18	70
678	SO[266]	9430	85.5	18	70
679	SO[267]	9418	295.5	18	70
680	SO[268]	9406	190.5	18	70
681	SO[269]	9394	85.5	18	70
682	SO[270]	9382	295.5	18	70
683	SO[271]	9370	190.5	18	70
684	SO[272]	9358	85.5	18	70
685	SO[273]	9346	295.5	18	70
686	SO[274]	9334	190.5	18	70
687	SO[275]	9322	85.5	18	70
688	SO[276]	9310	295.5	18	70
689	SO[277]	9298	190.5	18	70
690	SO[278]	9286	85.5	18	70
691	SO[279]	9274	295.5	18	70
692	SO[280]	9262	190.5	18	70
693	SO[281]	9250	85.5	18	70
694	SO[282]	9238	295.5	18	70
695	SO[283]	9226	190.5	18	70
696	SO[284]	9214	85.5	18	70
697	SO[285]	9202	295.5	18	70
698	SO[286]	9190	190.5	18	70
699	SO[287]	9178	85.5	18	70
700	SO[288]	9166	295.5	18	70
701	SO[289]	9154	190.5	18	70
702	SO[290]	9142	85.5	18	70
703	SO[291]	9130	295.5	18	70
704	SO[292]	9118	190.5	18	70
705	SO[293]	9106	85.5	18	70
706	SO[294]	9094	295.5	18	70
707	SO[295]	9082	190.5	18	70
708	SO[296]	9070	85.5	18	70
709	SO[297]	9058	295.5	18	70
710	SO[298]	9046	190.5	18	70
711	SO[299]	9034	85.5	18	70
712	SO[300]	9022	295.5	18	70
713	SO[301]	9010	190.5	18	70
714	SO[302]	8998	85.5	18	70
715	SO[303]	8986	295.5	18	70
716	SO[304]	8974	190.5	18	70
717	SO[305]	8962	85.5	18	70
718	SO[306]	8950	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
719	SO[307]	8938	190.5	18	70
720	SO[308]	8926	85.5	18	70
721	SO[309]	8914	295.5	18	70
722	SO[310]	8902	190.5	18	70
723	SO[311]	8890	85.5	18	70
724	SO[312]	8878	295.5	18	70
725	SO[313]	8866	190.5	18	70
726	SO[314]	8854	85.5	18	70
727	SO[315]	8842	295.5	18	70
728	SO[316]	8830	190.5	18	70
729	SO[317]	8818	85.5	18	70
730	SO[318]	8806	295.5	18	70
731	SO[319]	8794	190.5	18	70
732	SO[320]	8782	85.5	18	70
733	SO[321]	8770	295.5	18	70
734	SO[322]	8758	190.5	18	70
735	SO[323]	8746	85.5	18	70
736	SO[324]	8734	295.5	18	70
737	SO[325]	8722	190.5	18	70
738	SO[326]	8710	85.5	18	70
739	SO[327]	8698	295.5	18	70
740	SO[328]	8686	190.5	18	70
741	SO[329]	8674	85.5	18	70
742	SO[330]	8662	295.5	18	70
743	SO[331]	8650	190.5	18	70
744	SO[332]	8638	85.5	18	70
745	SO[333]	8626	295.5	18	70
746	SO[334]	8614	190.5	18	70
747	SO[335]	8602	85.5	18	70
748	SO[336]	8590	295.5	18	70
749	SO[337]	8578	190.5	18	70
750	SO[338]	8566	85.5	18	70
751	SO[339]	8554	295.5	18	70
752	SO[340]	8542	190.5	18	70
753	SO[341]	8530	85.5	18	70
754	SO[342]	8518	295.5	18	70
755	SO[343]	8506	190.5	18	70
756	SO[344]	8494	85.5	18	70
757	SO[345]	8482	295.5	18	70
758	SO[346]	8470	190.5	18	70
759	SO[347]	8458	85.5	18	70
760	SO[348]	8446	295.5	18	70
761	SO[349]	8434	190.5	18	70
762	SO[350]	8422	85.5	18	70
763	SO[351]	8410	295.5	18	70
764	SO[352]	8398	190.5	18	70
765	SO[353]	8386	85.5	18	70
766	SO[354]	8374	295.5	18	70
767	SO[355]	8362	190.5	18	70
768	SO[356]	8350	85.5	18	70
769	SO[357]	8338	295.5	18	70
770	SO[358]	8326	190.5	18	70
771	SO[359]	8314	85.5	18	70
772	SO[360]	8302	295.5	18	70
773	SO[361]	8290	190.5	18	70
774	SO[362]	8278	85.5	18	70
775	SO[363]	8266	295.5	18	70
776	SO[364]	8254	190.5	18	70
777	SO[365]	8242	85.5	18	70
778	SO[366]	8230	295.5	18	70
779	SO[367]	8218	190.5	18	70
780	SO[368]	8206	85.5	18	70
781	SO[369]	8194	295.5	18	70
782	SO[370]	8182	190.5	18	70
783	SO[371]	8170	85.5	18	70
784	SO[372]	8158	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
785	SO[373]	8146	190.5	18	70
786	SO[374]	8134	85.5	18	70
787	SO[375]	8122	295.5	18	70
788	SO[376]	8110	190.5	18	70
789	SO[377]	8098	85.5	18	70
790	SO[378]	8086	295.5	18	70
791	SO[379]	8074	190.5	18	70
792	SO[380]	8062	85.5	18	70
793	SO[381]	8050	295.5	18	70
794	SO[382]	8038	190.5	18	70
795	SO[383]	8026	85.5	18	70
796	SO[384]	8014	295.5	18	70
797	SO[385]	8002	190.5	18	70
798	SO[386]	7990	85.5	18	70
799	SO[387]	7978	295.5	18	70
800	SO[388]	7966	190.5	18	70
801	SO[389]	7954	85.5	18	70
802	SO[390]	7942	295.5	18	70
803	SO[391]	7930	190.5	18	70
804	SO[392]	7918	85.5	18	70
805	SO[393]	7906	295.5	18	70
806	SO[394]	7894	190.5	18	70
807	SO[395]	7882	85.5	18	70
808	SO[396]	7870	295.5	18	70
809	SO[397]	7858	190.5	18	70
810	SO[398]	7846	85.5	18	70
811	SO[399]	7834	295.5	18	70
812	SO[400]	7822	190.5	18	70
813	SO[401]	7810	85.5	18	70
814	SO[402]	7798	295.5	18	70
815	SO[403]	7786	190.5	18	70
816	SO[404]	7774	85.5	18	70
817	SO[405]	7762	295.5	18	70
818	SO[406]	7750	190.5	18	70
819	SO[407]	7738	85.5	18	70
820	SO[408]	7726	295.5	18	70
821	SO[409]	7714	190.5	18	70
822	SO[410]	7702	85.5	18	70
823	SO[411]	7690	295.5	18	70
824	SO[412]	7678	190.5	18	70
825	SO[413]	7666	85.5	18	70
826	SO[414]	7654	295.5	18	70
827	SO[415]	7642	190.5	18	70
828	SO[416]	7630	85.5	18	70
829	SO[417]	7618	295.5	18	70
830	SO[418]	7606	190.5	18	70
831	SO[419]	7594	85.5	18	70
832	SO[420]	7582	295.5	18	70
833	SO[421]	7570	190.5	18	70
834	SO[422]	7558	85.5	18	70
835	SO[423]	7546	295.5	18	70
836	SO[424]	7534	190.5	18	70
837	SO[425]	7522	85.5	18	70
838	SO[426]	7510	295.5	18	70
839	SO[427]	7498	190.5	18	70
840	SO[428]	7486	85.5	18	70
841	SO[429]	7474	295.5	18	70
842	SO[430]	7462	190.5	18	70
843	SO[431]	7450	85.5	18	70
844	SO[432]	7438	295.5	18	70
845	SO[433]	7426	190.5	18	70
846	SO[434]	7414	85.5	18	70
847	SO[435]	7402	295.5	18	70
848	SO[436]	7390	190.5	18	70
849	SO[437]	7378	85.5	18	70
850	SO[438]	7366	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
851	SO[439]	7354	190.5	18	70
852	SO[440]	7342	85.5	18	70
853	SO[441]	7330	295.5	18	70
854	SO[442]	7318	190.5	18	70
855	SO[443]	7306	85.5	18	70
856	SO[444]	7294	295.5	18	70
857	SO[445]	7282	190.5	18	70
858	SO[446]	7270	85.5	18	70
859	SO[447]	7258	295.5	18	70
860	SO[448]	7246	190.5	18	70
861	SO[449]	7234	85.5	18	70
862	SO[450]	7222	295.5	18	70
863	SO[451]	7210	190.5	18	70
864	SO[452]	7198	85.5	18	70
865	SO[453]	7186	295.5	18	70
866	SO[454]	7174	190.5	18	70
867	SO[455]	7162	85.5	18	70
868	SO[456]	7150	295.5	18	70
869	SO[457]	7138	190.5	18	70
870	SO[458]	7126	85.5	18	70
871	SO[459]	7114	295.5	18	70
872	SO[460]	7102	190.5	18	70
873	SO[461]	7090	85.5	18	70
874	SO[462]	7078	295.5	18	70
875	SO[463]	7066	190.5	18	70
876	SO[464]	7054	85.5	18	70
877	SO[465]	7042	295.5	18	70
878	SO[466]	7030	190.5	18	70
879	SO[467]	7018	85.5	18	70
880	SO[468]	7006	295.5	18	70
881	SO[469]	6994	190.5	18	70
882	SO[470]	6982	85.5	18	70
883	SO[471]	6970	295.5	18	70
884	SO[472]	6958	190.5	18	70
885	SO[473]	6946	85.5	18	70
886	SO[474]	6934	295.5	18	70
887	SO[475]	6922	190.5	18	70
888	SO[476]	6910	85.5	18	70
889	SO[477]	6898	295.5	18	70
890	SO[478]	6886	190.5	18	70
891	SO[479]	6874	85.5	18	70
892	SO[480]	6862	295.5	18	70
893	SO[481]	6850	190.5	18	70
894	SO[482]	6838	85.5	18	70
895	SO[483]	6826	295.5	18	70
896	SO[484]	6814	190.5	18	70
897	SO[485]	6802	85.5	18	70
898	SO[486]	6790	295.5	18	70
899	SO[487]	6778	190.5	18	70
900	SO[488]	6766	85.5	18	70
901	SO[489]	6754	295.5	18	70
902	SO[490]	6742	190.5	18	70
903	SO[491]	6730	85.5	18	70
904	SO[492]	6718	295.5	18	70
905	SO[493]	6706	190.5	18	70
906	SO[494]	6694	85.5	18	70
907	SO[495]	6682	295.5	18	70
908	SO[496]	6670	190.5	18	70
909	SO[497]	6658	85.5	18	70
910	SO[498]	6646	295.5	18	70
911	SO[499]	6634	190.5	18	70
912	SO[500]	6622	85.5	18	70
913	SO[501]	6610	295.5	18	70
914	SO[502]	6598	190.5	18	70
915	SO[503]	6586	85.5	18	70
916	SO[504]	6574	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
917	SO[505]	6562	190.5	18	70
918	SO[506]	6550	85.5	18	70
919	SO[507]	6538	295.5	18	70
920	SO[508]	6526	190.5	18	70
921	SO[509]	6514	85.5	18	70
922	SO[510]	6502	295.5	18	70
923	SO[511]	6490	190.5	18	70
924	SO[512]	6478	85.5	18	70
925	SO[513]	6466	295.5	18	70
926	SO[514]	6454	190.5	18	70
927	SO[515]	6442	85.5	18	70
928	SO[516]	6430	295.5	18	70
929	SO[517]	6418	190.5	18	70
930	SO[518]	6406	85.5	18	70
931	SO[519]	6394	295.5	18	70
932	SO[520]	6382	190.5	18	70
933	SO[521]	6370	85.5	18	70
934	SO[522]	6358	295.5	18	70
935	SO[523]	6346	190.5	18	70
936	SO[524]	6334	85.5	18	70
937	SO[525]	6322	295.5	18	70
938	SO[526]	6310	190.5	18	70
939	SO[527]	6298	85.5	18	70
940	SO[528]	6286	295.5	18	70
941	SO[529]	6274	190.5	18	70
942	SO[530]	6262	85.5	18	70
943	SO[531]	6250	295.5	18	70
944	SO[532]	6238	190.5	18	70
945	SO[533]	6226	85.5	18	70
946	SO[534]	6214	295.5	18	70
947	SO[535]	6202	190.5	18	70
948	SO[536]	6190	85.5	18	70
949	SO[537]	6178	295.5	18	70
950	SO[538]	6166	190.5	18	70
951	SO[539]	6154	85.5	18	70
952	SO[540]	6142	295.5	18	70
953	SO[541]	6130	190.5	18	70
954	SO[542]	6118	85.5	18	70
955	SO[543]	6106	295.5	18	70
956	SO[544]	6094	190.5	18	70
957	SO[545]	6082	85.5	18	70
958	SO[546]	6070	295.5	18	70
959	SO[547]	6058	190.5	18	70
960	SO[548]	6046	85.5	18	70
961	SO[549]	6034	295.5	18	70
962	SO[550]	6022	190.5	18	70
963	SO[551]	6010	85.5	18	70
964	SO[552]	5998	295.5	18	70
965	SO[553]	5986	190.5	18	70
966	SO[554]	5974	85.5	18	70
967	SO[555]	5962	295.5	18	70
968	SO[556]	5950	190.5	18	70
969	SO[557]	5938	85.5	18	70
970	SO[558]	5926	295.5	18	70
971	SO[559]	5914	190.5	18	70
972	SO[560]	5902	85.5	18	70
973	SO[561]	5890	295.5	18	70
974	SO[562]	5878	190.5	18	70
975	SO[563]	5866	85.5	18	70
976	SO[564]	5854	295.5	18	70
977	SO[565]	5842	190.5	18	70
978	SO[566]	5830	85.5	18	70
979	SO[567]	5818	295.5	18	70
980	SO[568]	5806	190.5	18	70
981	SO[569]	5794	85.5	18	70
982	SO[570]	5782	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
983	SO[571]	5770	190.5	18	70
984	SO[572]	5758	85.5	18	70
985	SO[573]	5746	295.5	18	70
986	SO[574]	5734	190.5	18	70
987	SO[575]	5722	85.5	18	70
988	SO[576]	5710	295.5	18	70
989	SO[577]	5698	190.5	18	70
990	SO[578]	5686	85.5	18	70
991	SO[579]	5674	295.5	18	70
992	SO[580]	5662	190.5	18	70
993	SO[581]	5650	85.5	18	70
994	SO[582]	5638	295.5	18	70
995	SO[583]	5626	190.5	18	70
996	SO[584]	5614	85.5	18	70
997	SO[585]	5602	295.5	18	70
998	SO[586]	5590	190.5	18	70
999	SO[587]	5578	85.5	18	70
1000	SO[588]	5566	295.5	18	70
1001	SO[589]	5554	190.5	18	70
1002	SO[590]	5542	85.5	18	70
1003	SO[591]	5530	295.5	18	70
1004	SO[592]	5518	190.5	18	70
1005	SO[593]	5506	85.5	18	70
1006	SO[594]	5494	295.5	18	70
1007	SO[595]	5482	190.5	18	70
1008	SO[596]	5470	85.5	18	70
1009	SO[597]	5458	295.5	18	70
1010	SO[598]	5446	190.5	18	70
1011	SO[599]	5434	85.5	18	70
1012	SO[600]	5422	295.5	18	70
1013	SO[601]	5410	190.5	18	70
1014	SO[602]	5398	85.5	18	70
1015	SO[603]	5386	295.5	18	70
1016	SO[604]	5374	190.5	18	70
1017	SO[605]	5362	85.5	18	70
1018	SO[606]	5350	295.5	18	70
1019	SO[607]	5338	190.5	18	70
1020	SO[608]	5326	85.5	18	70
1021	SO[609]	5314	295.5	18	70
1022	SO[610]	5302	190.5	18	70
1023	SO[611]	5290	85.5	18	70
1024	SO[612]	5278	295.5	18	70
1025	SO[613]	5266	190.5	18	70
1026	SO[614]	5254	85.5	18	70
1027	SO[615]	5242	295.5	18	70
1028	SO[616]	5230	190.5	18	70
1029	SO[617]	5218	85.5	18	70
1030	SO[618]	5206	295.5	18	70
1031	SO[619]	5194	190.5	18	70
1032	SO[620]	5182	85.5	18	70
1033	SO[621]	5170	295.5	18	70
1034	SO[622]	5158	190.5	18	70
1035	SO[623]	5146	85.5	18	70
1036	SO[624]	5134	295.5	18	70
1037	SO[625]	5122	190.5	18	70
1038	SO[626]	5110	85.5	18	70
1039	SO[627]	5098	295.5	18	70
1040	SO[628]	5086	190.5	18	70
1041	SO[629]	5074	85.5	18	70
1042	SO[630]	5062	295.5	18	70
1043	SO[631]	5050	190.5	18	70
1044	SO[632]	5038	85.5	18	70
1045	SO[633]	5026	295.5	18	70
1046	SO[634]	5014	190.5	18	70
1047	SO[635]	5002	85.5	18	70
1048	SO[636]	4990	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1049	SO[637]	4978	190.5	18	70
1050	SO[638]	4966	85.5	18	70
1051	SO[639]	4954	295.5	18	70
1052	SO[640]	4942	190.5	18	70
1053	SO[641]	4930	85.5	18	70
1054	SO[642]	4918	295.5	18	70
1055	SO[643]	4906	190.5	18	70
1056	SO[644]	4894	85.5	18	70
1057	SO[645]	4882	295.5	18	70
1058	SO[646]	4870	190.5	18	70
1059	SO[647]	4858	85.5	18	70
1060	SO[648]	4846	295.5	18	70
1061	SO[649]	4834	190.5	18	70
1062	SO[650]	4822	85.5	18	70
1063	SO[651]	4810	295.5	18	70
1064	SO[652]	4798	190.5	18	70
1065	SO[653]	4786	85.5	18	70
1066	SO[654]	4774	295.5	18	70
1067	SO[655]	4762	190.5	18	70
1068	SO[656]	4750	85.5	18	70
1069	SO[657]	4738	295.5	18	70
1070	SO[658]	4726	190.5	18	70
1071	SO[659]	4714	85.5	18	70
1072	SO[660]	4702	295.5	18	70
1073	SO[661]	4690	190.5	18	70
1074	SO[662]	4678	85.5	18	70
1075	SO[663]	4666	295.5	18	70
1076	SO[664]	4654	190.5	18	70
1077	SO[665]	4642	85.5	18	70
1078	SO[666]	4630	295.5	18	70
1079	SO[667]	4618	190.5	18	70
1080	SO[668]	4606	85.5	18	70
1081	SO[669]	4594	295.5	18	70
1082	SO[670]	4582	190.5	18	70
1083	SO[671]	4570	85.5	18	70
1084	SO[672]	4558	295.5	18	70
1085	SO[673]	4546	190.5	18	70
1086	SO[674]	4534	85.5	18	70
1087	SO[675]	4522	295.5	18	70
1088	SO[676]	4510	190.5	18	70
1089	SO[677]	4498	85.5	18	70
1090	SO[678]	4486	295.5	18	70
1091	SO[679]	4474	190.5	18	70
1092	SO[680]	4462	85.5	18	70
1093	SO[681]	4450	295.5	18	70
1094	SO[682]	4438	190.5	18	70
1095	SO[683]	4426	85.5	18	70
1096	SO[684]	4414	295.5	18	70
1097	SO[685]	4402	190.5	18	70
1098	SO[686]	4390	85.5	18	70
1099	SO[687]	4378	295.5	18	70
1100	SO[688]	4366	190.5	18	70
1101	SO[689]	4354	85.5	18	70
1102	SO[690]	4342	295.5	18	70
1103	SO[691]	4330	190.5	18	70
1104	SO[692]	4318	85.5	18	70
1105	SO[693]	4306	295.5	18	70
1106	SO[694]	4294	190.5	18	70
1107	SO[695]	4282	85.5	18	70
1108	SO[696]	4270	295.5	18	70
1109	SO[697]	4258	190.5	18	70
1110	SO[698]	4246	85.5	18	70
1111	SO[699]	4234	295.5	18	70
1112	SO[700]	4222	190.5	18	70
1113	SO[701]	4210	85.5	18	70
1114	SO[702]	4198	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1115	SO[703]	4186	190.5	18	70
1116	SO[704]	4174	85.5	18	70
1117	SO[705]	4162	295.5	18	70
1118	SO[706]	4150	190.5	18	70
1119	SO[707]	4138	85.5	18	70
1120	SO[708]	4126	295.5	18	70
1121	SO[709]	4114	190.5	18	70
1122	SO[710]	4102	85.5	18	70
1123	SO[711]	4090	295.5	18	70
1124	SO[712]	4078	190.5	18	70
1125	SO[713]	4066	85.5	18	70
1126	SO[714]	4054	295.5	18	70
1127	SO[715]	4042	190.5	18	70
1128	SO[716]	4030	85.5	18	70
1129	SO[717]	4018	295.5	18	70
1130	SO[718]	4006	190.5	18	70
1131	SO[719]	3994	85.5	18	70
1132	SO[720]	3982	295.5	18	70
1133	SO[721]	3970	190.5	18	70
1134	SO[722]	3958	85.5	18	70
1135	SO[723]	3946	295.5	18	70
1136	SO[724]	3934	190.5	18	70
1137	SO[725]	3922	85.5	18	70
1138	SO[726]	3910	295.5	18	70
1139	SO[727]	3898	190.5	18	70
1140	SO[728]	3886	85.5	18	70
1141	SO[729]	3874	295.5	18	70
1142	SO[730]	3862	190.5	18	70
1143	SO[731]	3850	85.5	18	70
1144	SO[732]	3838	295.5	18	70
1145	SO[733]	3826	190.5	18	70
1146	SO[734]	3814	85.5	18	70
1147	SO[735]	3802	295.5	18	70
1148	SO[736]	3790	190.5	18	70
1149	SO[737]	3778	85.5	18	70
1150	SO[738]	3766	295.5	18	70
1151	SO[739]	3754	190.5	18	70
1152	SO[740]	3742	85.5	18	70
1153	SO[741]	3730	295.5	18	70
1154	SO[742]	3718	190.5	18	70
1155	SO[743]	3706	85.5	18	70
1156	SO[744]	3694	295.5	18	70
1157	SO[745]	3682	190.5	18	70
1158	SO[746]	3670	85.5	18	70
1159	SO[747]	3658	295.5	18	70
1160	SO[748]	3646	190.5	18	70
1161	SO[749]	3634	85.5	18	70
1162	SO[750]	3622	295.5	18	70
1163	SO[751]	3610	190.5	18	70
1164	SO[752]	3598	85.5	18	70
1165	SO[753]	3586	295.5	18	70
1166	SO[754]	3574	190.5	18	70
1167	SO[755]	3562	85.5	18	70
1168	SO[756]	3550	295.5	18	70
1169	SO[757]	3538	190.5	18	70
1170	SO[758]	3526	85.5	18	70
1171	SO[759]	3514	295.5	18	70
1172	SO[760]	3502	190.5	18	70
1173	SO[761]	3490	85.5	18	70
1174	SO[762]	3478	295.5	18	70
1175	SO[763]	3466	190.5	18	70
1176	SO[764]	3454	85.5	18	70
1177	SO[765]	3442	295.5	18	70
1178	SO[766]	3430	190.5	18	70
1179	SO[767]	3418	85.5	18	70
1180	SO[768]	3406	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1181	SO[769]	3394	190.5	18	70
1182	SO[770]	3382	85.5	18	70
1183	SO[771]	3370	295.5	18	70
1184	SO[772]	3358	190.5	18	70
1185	SO[773]	3346	85.5	18	70
1186	SO[774]	3334	295.5	18	70
1187	SO[775]	3322	190.5	18	70
1188	SO[776]	3310	85.5	18	70
1189	SO[777]	3298	295.5	18	70
1190	SO[778]	3286	190.5	18	70
1191	SO[779]	3274	85.5	18	70
1192	SO[780]	3262	295.5	18	70
1193	SO[781]	3250	190.5	18	70
1194	SO[782]	3238	85.5	18	70
1195	SO[783]	3226	295.5	18	70
1196	SO[784]	3214	190.5	18	70
1197	SO[785]	3202	85.5	18	70
1198	SO[786]	3190	295.5	18	70
1199	SO[787]	3178	190.5	18	70
1200	SO[788]	3166	85.5	18	70
1201	SO[789]	3154	295.5	18	70
1202	SO[790]	3142	190.5	18	70
1203	SO[791]	3130	85.5	18	70
1204	SO[792]	3118	295.5	18	70
1205	SO[793]	3106	190.5	18	70
1206	SO[794]	3094	85.5	18	70
1207	SO[795]	3082	295.5	18	70
1208	SO[796]	3070	190.5	18	70
1209	SO[797]	3058	85.5	18	70
1210	SO[798]	3046	295.5	18	70
1211	SO[799]	3034	190.5	18	70
1212	SO[800]	3022	85.5	18	70
1213	SO[801]	3010	295.5	18	70
1214	SO[802]	2998	190.5	18	70
1215	SO[803]	2986	85.5	18	70
1216	SO[804]	2974	295.5	18	70
1217	SO[805]	2962	190.5	18	70
1218	SO[806]	2950	85.5	18	70
1219	SO[807]	2938	295.5	18	70
1220	SO[808]	2926	190.5	18	70
1221	SO[809]	2914	85.5	18	70
1222	SO[810]	2902	295.5	18	70
1223	SO[811]	2890	190.5	18	70
1224	SO[812]	2878	85.5	18	70
1225	SO[813]	2866	295.5	18	70
1226	SO[814]	2854	190.5	18	70
1227	SO[815]	2842	85.5	18	70
1228	SO[816]	2830	295.5	18	70
1229	SO[817]	2818	190.5	18	70
1230	SO[818]	2806	85.5	18	70
1231	SO[819]	2794	295.5	18	70
1232	SO[820]	2782	190.5	18	70
1233	SO[821]	2770	85.5	18	70
1234	SO[822]	2758	295.5	18	70
1235	SO[823]	2746	190.5	18	70
1236	SO[824]	2734	85.5	18	70
1237	SO[825]	2722	295.5	18	70
1238	SO[826]	2710	190.5	18	70
1239	SO[827]	2698	85.5	18	70
1240	SO[828]	2686	295.5	18	70
1241	SO[829]	2674	190.5	18	70
1242	SO[830]	2662	85.5	18	70
1243	SO[831]	2650	295.5	18	70
1244	SO[832]	2638	190.5	18	70
1245	SO[833]	2626	85.5	18	70
1246	SO[834]	2614	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1247	SO[835]	2602	190.5	18	70
1248	SO[836]	2590	85.5	18	70
1249	SO[837]	2578	295.5	18	70
1250	SO[838]	2566	190.5	18	70
1251	SO[839]	2554	85.5	18	70
1252	SO[840]	2542	295.5	18	70
1253	SO[841]	2530	190.5	18	70
1254	SO[842]	2518	85.5	18	70
1255	SO[843]	2506	295.5	18	70
1256	SO[844]	2494	190.5	18	70
1257	SO[845]	2482	85.5	18	70
1258	SO[846]	2470	295.5	18	70
1259	SO[847]	2458	190.5	18	70
1260	SO[848]	2446	85.5	18	70
1261	SO[849]	2434	295.5	18	70
1262	SO[850]	2422	190.5	18	70
1263	SO[851]	2410	85.5	18	70
1264	SO[852]	2398	295.5	18	70
1265	SO[853]	2386	190.5	18	70
1266	SO[854]	2374	85.5	18	70
1267	SO[855]	2362	295.5	18	70
1268	SO[856]	2350	190.5	18	70
1269	SO[857]	2338	85.5	18	70
1270	SO[858]	2326	295.5	18	70
1271	SO[859]	2314	190.5	18	70
1272	SO[860]	2302	85.5	18	70
1273	SO[861]	2290	295.5	18	70
1274	SO[862]	2278	190.5	18	70
1275	SO[863]	2266	85.5	18	70
1276	SO[864]	2254	295.5	18	70
1277	SO[865]	2242	190.5	18	70
1278	SO[866]	2230	85.5	18	70
1279	SO[867]	2218	295.5	18	70
1280	SO[868]	2206	190.5	18	70
1281	SO[869]	2194	85.5	18	70
1282	SO[870]	2182	295.5	18	70
1283	SO[871]	2170	190.5	18	70
1284	SO[872]	2158	85.5	18	70
1285	SO[873]	2146	295.5	18	70
1286	SO[874]	2134	190.5	18	70
1287	SO[875]	2122	85.5	18	70
1288	SO[876]	2110	295.5	18	70
1289	SO[877]	2098	190.5	18	70
1290	SO[878]	2086	85.5	18	70
1291	SO[879]	2074	295.5	18	70
1292	SO[880]	2062	190.5	18	70
1293	SO[881]	2050	85.5	18	70
1294	SO[882]	2038	295.5	18	70
1295	SO[883]	2026	190.5	18	70
1296	SO[884]	2014	85.5	18	70
1297	SO[885]	2002	295.5	18	70
1298	SO[886]	1990	190.5	18	70
1299	SO[887]	1978	85.5	18	70
1300	SO[888]	1966	295.5	18	70
1301	SO[889]	1954	190.5	18	70
1302	SO[890]	1942	85.5	18	70
1303	SO[891]	1930	295.5	18	70
1304	SO[892]	1918	190.5	18	70
1305	SO[893]	1906	85.5	18	70
1306	SO[894]	1894	295.5	18	70
1307	SO[895]	1882	190.5	18	70
1308	SO[896]	1870	85.5	18	70
1309	SO[897]	1858	295.5	18	70
1310	SO[898]	1846	190.5	18	70
1311	SO[899]	1834	85.5	18	70
1312	SO[900]	1822	295.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1313	SHIELDING_AGND	1810	190.5	18	70
1314	SHIELDING_AGND	1798	85.5	18	70
1315	SHIELDING_AGND	1786	295.5	18	70
1316	SHIELDING_AGND	1726	310.5	40	40
1317	SHIELDING_AGND	1646	310.5	40	40
1318	SHIELDING_AGND	1566	310.5	40	40
1319	SHIELDING_AGND	1486	310.5	40	40
1320	SHIELDING_AGND	1406	310.5	40	40
1321	SHIELDING_AGND	1326	310.5	40	40
1322	SHIELDING_AGND	1246	310.5	40	40
1323	SHIELDING_AGND	1166	310.5	40	40
1324	SHIELDING_AGND	1086	310.5	40	40
1325	SHIELDING_AGND	1006	310.5	40	40
1326	SHIELDING_AGND	926	310.5	40	40
1327	SHIELDING_AGND	846	310.5	40	40
1328	SHIELDING_AGND	766	310.5	40	40
1329	SHIELDING_AGND	686	310.5	40	40
1330	SHIELDING_AGND	606	310.5	40	40
1331	SHIELDING_AGND	526	310.5	40	40
1332	SHIELDING_AGND	446	310.5	40	40
1333	SHIELDING_AGND	366	310.5	40	40
1334	SHIELDING_AGND	286	310.5	40	40
1335	SHIELDING_AGND	206	310.5	40	40
1336	SHIELDING_AGND	126	310.5	40	40
1337	SHIELDING_AGND	46	310.5	40	40
1338	SHIELDING_AGND	-34	310.5	40	40
1339	SHIELDING_AGND	-114	310.5	40	40
1340	SHIELDING_AGND	-194	310.5	40	40
1341	SHIELDING_AGND	-274	310.5	40	40
1342	SHIELDING_AGND	-354	310.5	40	40
1343	SHIELDING_AGND	-434	310.5	40	40
1344	SHIELDING_AGND	-514	310.5	40	40
1345	SHIELDING_AGND	-594	310.5	40	40
1346	SHIELDING_AGND	-674	310.5	40	40
1347	SHIELDING_AGND	-754	310.5	40	40
1348	SHIELDING_AGND	-834	310.5	40	40
1349	SHIELDING_AGND	-914	310.5	40	40
1350	SHIELDING_AGND	-994	310.5	40	40
1351	SHIELDING_AGND	-1074	310.5	40	40
1352	SHIELDING_AGND	-1154	310.5	40	40
1353	SHIELDING_AGND	-1234	310.5	40	40
1354	SHIELDING_AGND	-1314	310.5	40	40
1355	SHIELDING_AGND	-1394	310.5	40	40
1356	SHIELDING_AGND	-1474	310.5	40	40
1357	SHIELDING_AGND	-1554	310.5	40	40
1358	SHIELDING_AGND	-1634	310.5	40	40
1359	SHIELDING_AGND	-1714	310.5	40	40
1360	SHIELDING_AGND	-1794	310.5	40	40
1361	SHIELDING_AGND	-1874	310.5	40	40
1362	SHIELDING_AGND	-1954	310.5	40	40
1363	SHIELDING_AGND	-2034	310.5	40	40
1364	SHIELDING_AGND	-2114	310.5	40	40
1365	SHIELDING_AGND	-2194	310.5	40	40
1366	SHIELDING_AGND	-2274	310.5	40	40
1367	SHIELDING_AGND	-2334	295.5	18	70
1368	SHIELDING_AGND	-2346	190.5	18	70
1369	SHIELDING_AGND	-2358	85.5	18	70
1370	SO[901]	-2370	295.5	18	70
1371	SO[902]	-2382	190.5	18	70
1372	SO[903]	-2394	85.5	18	70
1373	SO[904]	-2406	295.5	18	70
1374	SO[905]	-2418	190.5	18	70
1375	SO[906]	-2430	85.5	18	70
1376	SO[907]	-2442	295.5	18	70
1377	SO[908]	-2454	190.5	18	70
1378	SO[909]	-2466	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1379	SO[910]	-2478	295.5	18	70
1380	SO[911]	-2490	190.5	18	70
1381	SO[912]	-2502	85.5	18	70
1382	SO[913]	-2514	295.5	18	70
1383	SO[914]	-2526	190.5	18	70
1384	SO[915]	-2538	85.5	18	70
1385	SO[916]	-2550	295.5	18	70
1386	SO[917]	-2562	190.5	18	70
1387	SO[918]	-2574	85.5	18	70
1388	SO[919]	-2586	295.5	18	70
1389	SO[920]	-2598	190.5	18	70
1390	SO[921]	-2610	85.5	18	70
1391	SO[922]	-2622	295.5	18	70
1392	SO[923]	-2634	190.5	18	70
1393	SO[924]	-2646	85.5	18	70
1394	SO[925]	-2658	295.5	18	70
1395	SO[926]	-2670	190.5	18	70
1396	SO[927]	-2682	85.5	18	70
1397	SO[928]	-2694	295.5	18	70
1398	SO[929]	-2706	190.5	18	70
1399	SO[930]	-2718	85.5	18	70
1400	SO[931]	-2730	295.5	18	70
1401	SO[932]	-2742	190.5	18	70
1402	SO[933]	-2754	85.5	18	70
1403	SO[934]	-2766	295.5	18	70
1404	SO[935]	-2778	190.5	18	70
1405	SO[936]	-2790	85.5	18	70
1406	SO[937]	-2802	295.5	18	70
1407	SO[938]	-2814	190.5	18	70
1408	SO[939]	-2826	85.5	18	70
1409	SO[940]	-2838	295.5	18	70
1410	SO[941]	-2850	190.5	18	70
1411	SO[942]	-2862	85.5	18	70
1412	SO[943]	-2874	295.5	18	70
1413	SO[944]	-2886	190.5	18	70
1414	SO[945]	-2898	85.5	18	70
1415	SO[946]	-2910	295.5	18	70
1416	SO[947]	-2922	190.5	18	70
1417	SO[948]	-2934	85.5	18	70
1418	SO[949]	-2946	295.5	18	70
1419	SO[950]	-2958	190.5	18	70
1420	SO[951]	-2970	85.5	18	70
1421	SO[952]	-2982	295.5	18	70
1422	SO[953]	-2994	190.5	18	70
1423	SO[954]	-3006	85.5	18	70
1424	SO[955]	-3018	295.5	18	70
1425	SO[956]	-3030	190.5	18	70
1426	SO[957]	-3042	85.5	18	70
1427	SO[958]	-3054	295.5	18	70
1428	SO[959]	-3066	190.5	18	70
1429	SO[960]	-3078	85.5	18	70
1430	SO[961]	-3090	295.5	18	70
1431	SO[962]	-3102	190.5	18	70
1432	SO[963]	-3114	85.5	18	70
1433	SO[964]	-3126	295.5	18	70
1434	SO[965]	-3138	190.5	18	70
1435	SO[966]	-3150	85.5	18	70
1436	SO[967]	-3162	295.5	18	70
1437	SO[968]	-3174	190.5	18	70
1438	SO[969]	-3186	85.5	18	70
1439	SO[970]	-3198	295.5	18	70
1440	SO[971]	-3210	190.5	18	70
1441	SO[972]	-3222	85.5	18	70
1442	SO[973]	-3234	295.5	18	70
1443	SO[974]	-3246	190.5	18	70
1444	SO[975]	-3258	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1445	SO[976]	-3270	295.5	18	70
1446	SO[977]	-3282	190.5	18	70
1447	SO[978]	-3294	85.5	18	70
1448	SO[979]	-3306	295.5	18	70
1449	SO[980]	-3318	190.5	18	70
1450	SO[981]	-3330	85.5	18	70
1451	SO[982]	-3342	295.5	18	70
1452	SO[983]	-3354	190.5	18	70
1453	SO[984]	-3366	85.5	18	70
1454	SO[985]	-3378	295.5	18	70
1455	SO[986]	-3390	190.5	18	70
1456	SO[987]	-3402	85.5	18	70
1457	SO[988]	-3414	295.5	18	70
1458	SO[989]	-3426	190.5	18	70
1459	SO[990]	-3438	85.5	18	70
1460	SO[991]	-3450	295.5	18	70
1461	SO[992]	-3462	190.5	18	70
1462	SO[993]	-3474	85.5	18	70
1463	SO[994]	-3486	295.5	18	70
1464	SO[995]	-3498	190.5	18	70
1465	SO[996]	-3510	85.5	18	70
1466	SO[997]	-3522	295.5	18	70
1467	SO[998]	-3534	190.5	18	70
1468	SO[999]	-3546	85.5	18	70
1469	SO[1000]	-3558	295.5	18	70
1470	SO[1001]	-3570	190.5	18	70
1471	SO[1002]	-3582	85.5	18	70
1472	SO[1003]	-3594	295.5	18	70
1473	SO[1004]	-3606	190.5	18	70
1474	SO[1005]	-3618	85.5	18	70
1475	SO[1006]	-3630	295.5	18	70
1476	SO[1007]	-3642	190.5	18	70
1477	SO[1008]	-3654	85.5	18	70
1478	SO[1009]	-3666	295.5	18	70
1479	SO[1010]	-3678	190.5	18	70
1480	SO[1011]	-3690	85.5	18	70
1481	SO[1012]	-3702	295.5	18	70
1482	SO[1013]	-3714	190.5	18	70
1483	SO[1014]	-3726	85.5	18	70
1484	SO[1015]	-3738	295.5	18	70
1485	SO[1016]	-3750	190.5	18	70
1486	SO[1017]	-3762	85.5	18	70
1487	SO[1018]	-3774	295.5	18	70
1488	SO[1019]	-3786	190.5	18	70
1489	SO[1020]	-3798	85.5	18	70
1490	SO[1021]	-3810	295.5	18	70
1491	SO[1022]	-3822	190.5	18	70
1492	SO[1023]	-3834	85.5	18	70
1493	SO[1024]	-3846	295.5	18	70
1494	SO[1025]	-3858	190.5	18	70
1495	SO[1026]	-3870	85.5	18	70
1496	SO[1027]	-3882	295.5	18	70
1497	SO[1028]	-3894	190.5	18	70
1498	SO[1029]	-3906	85.5	18	70
1499	SO[1030]	-3918	295.5	18	70
1500	SO[1031]	-3930	190.5	18	70
1501	SO[1032]	-3942	85.5	18	70
1502	SO[1033]	-3954	295.5	18	70
1503	SO[1034]	-3966	190.5	18	70
1504	SO[1035]	-3978	85.5	18	70
1505	SO[1036]	-3990	295.5	18	70
1506	SO[1037]	-4002	190.5	18	70
1507	SO[1038]	-4014	85.5	18	70
1508	SO[1039]	-4026	295.5	18	70
1509	SO[1040]	-4038	190.5	18	70
1510	SO[1041]	-4050	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1511	SO[1042]	-4062	295.5	18	70
1512	SO[1043]	-4074	190.5	18	70
1513	SO[1044]	-4086	85.5	18	70
1514	SO[1045]	-4098	295.5	18	70
1515	SO[1046]	-4110	190.5	18	70
1516	SO[1047]	-4122	85.5	18	70
1517	SO[1048]	-4134	295.5	18	70
1518	SO[1049]	-4146	190.5	18	70
1519	SO[1050]	-4158	85.5	18	70
1520	SO[1051]	-4170	295.5	18	70
1521	SO[1052]	-4182	190.5	18	70
1522	SO[1053]	-4194	85.5	18	70
1523	SO[1054]	-4206	295.5	18	70
1524	SO[1055]	-4218	190.5	18	70
1525	SO[1056]	-4230	85.5	18	70
1526	SO[1057]	-4242	295.5	18	70
1527	SO[1058]	-4254	190.5	18	70
1528	SO[1059]	-4266	85.5	18	70
1529	SO[1060]	-4278	295.5	18	70
1530	SO[1061]	-4290	190.5	18	70
1531	SO[1062]	-4302	85.5	18	70
1532	SO[1063]	-4314	295.5	18	70
1533	SO[1064]	-4326	190.5	18	70
1534	SO[1065]	-4338	85.5	18	70
1535	SO[1066]	-4350	295.5	18	70
1536	SO[1067]	-4362	190.5	18	70
1537	SO[1068]	-4374	85.5	18	70
1538	SO[1069]	-4386	295.5	18	70
1539	SO[1070]	-4398	190.5	18	70
1540	SO[1071]	-4410	85.5	18	70
1541	SO[1072]	-4422	295.5	18	70
1542	SO[1073]	-4434	190.5	18	70
1543	SO[1074]	-4446	85.5	18	70
1544	SO[1075]	-4458	295.5	18	70
1545	SO[1076]	-4470	190.5	18	70
1546	SO[1077]	-4482	85.5	18	70
1547	SO[1078]	-4494	295.5	18	70
1548	SO[1079]	-4506	190.5	18	70
1549	SO[1080]	-4518	85.5	18	70
1550	SO[1081]	-4530	295.5	18	70
1551	SO[1082]	-4542	190.5	18	70
1552	SO[1083]	-4554	85.5	18	70
1553	SO[1084]	-4566	295.5	18	70
1554	SO[1085]	-4578	190.5	18	70
1555	SO[1086]	-4590	85.5	18	70
1556	SO[1087]	-4602	295.5	18	70
1557	SO[1088]	-4614	190.5	18	70
1558	SO[1089]	-4626	85.5	18	70
1559	SO[1090]	-4638	295.5	18	70
1560	SO[1091]	-4650	190.5	18	70
1561	SO[1092]	-4662	85.5	18	70
1562	SO[1093]	-4674	295.5	18	70
1563	SO[1094]	-4686	190.5	18	70
1564	SO[1095]	-4698	85.5	18	70
1565	SO[1096]	-4710	295.5	18	70
1566	SO[1097]	-4722	190.5	18	70
1567	SO[1098]	-4734	85.5	18	70
1568	SO[1099]	-4746	295.5	18	70
1569	SO[1100]	-4758	190.5	18	70
1570	SO[1101]	-4770	85.5	18	70
1571	SO[1102]	-4782	295.5	18	70
1572	SO[1103]	-4794	190.5	18	70
1573	SO[1104]	-4806	85.5	18	70
1574	SO[1105]	-4818	295.5	18	70
1575	SO[1106]	-4830	190.5	18	70
1576	SO[1107]	-4842	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1577	SO[1108]	-4854	295.5	18	70
1578	SO[1109]	-4866	190.5	18	70
1579	SO[1110]	-4878	85.5	18	70
1580	SO[1111]	-4890	295.5	18	70
1581	SO[1112]	-4902	190.5	18	70
1582	SO[1113]	-4914	85.5	18	70
1583	SO[1114]	-4926	295.5	18	70
1584	SO[1115]	-4938	190.5	18	70
1585	SO[1116]	-4950	85.5	18	70
1586	SO[1117]	-4962	295.5	18	70
1587	SO[1118]	-4974	190.5	18	70
1588	SO[1119]	-4986	85.5	18	70
1589	SO[1120]	-4998	295.5	18	70
1590	SO[1121]	-5010	190.5	18	70
1591	SO[1122]	-5022	85.5	18	70
1592	SO[1123]	-5034	295.5	18	70
1593	SO[1124]	-5046	190.5	18	70
1594	SO[1125]	-5058	85.5	18	70
1595	SO[1126]	-5070	295.5	18	70
1596	SO[1127]	-5082	190.5	18	70
1597	SO[1128]	-5094	85.5	18	70
1598	SO[1129]	-5106	295.5	18	70
1599	SO[1130]	-5118	190.5	18	70
1600	SO[1131]	-5130	85.5	18	70
1601	SO[1132]	-5142	295.5	18	70
1602	SO[1133]	-5154	190.5	18	70
1603	SO[1134]	-5166	85.5	18	70
1604	SO[1135]	-5178	295.5	18	70
1605	SO[1136]	-5190	190.5	18	70
1606	SO[1137]	-5202	85.5	18	70
1607	SO[1138]	-5214	295.5	18	70
1608	SO[1139]	-5226	190.5	18	70
1609	SO[1140]	-5238	85.5	18	70
1610	SO[1141]	-5250	295.5	18	70
1611	SO[1142]	-5262	190.5	18	70
1612	SO[1143]	-5274	85.5	18	70
1613	SO[1144]	-5286	295.5	18	70
1614	SO[1145]	-5298	190.5	18	70
1615	SO[1146]	-5310	85.5	18	70
1616	SO[1147]	-5322	295.5	18	70
1617	SO[1148]	-5334	190.5	18	70
1618	SO[1149]	-5346	85.5	18	70
1619	SO[1150]	-5358	295.5	18	70
1620	SO[1151]	-5370	190.5	18	70
1621	SO[1152]	-5382	85.5	18	70
1622	SO[1153]	-5394	295.5	18	70
1623	SO[1154]	-5406	190.5	18	70
1624	SO[1155]	-5418	85.5	18	70
1625	SO[1156]	-5430	295.5	18	70
1626	SO[1157]	-5442	190.5	18	70
1627	SO[1158]	-5454	85.5	18	70
1628	SO[1159]	-5466	295.5	18	70
1629	SO[1160]	-5478	190.5	18	70
1630	SO[1161]	-5490	85.5	18	70
1631	SO[1162]	-5502	295.5	18	70
1632	SO[1163]	-5514	190.5	18	70
1633	SO[1164]	-5526	85.5	18	70
1634	SO[1165]	-5538	295.5	18	70
1635	SO[1166]	-5550	190.5	18	70
1636	SO[1167]	-5562	85.5	18	70
1637	SO[1168]	-5574	295.5	18	70
1638	SO[1169]	-5586	190.5	18	70
1639	SO[1170]	-5598	85.5	18	70
1640	SO[1171]	-5610	295.5	18	70
1641	SO[1172]	-5622	190.5	18	70
1642	SO[1173]	-5634	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1643	SO[1174]	-5646	295.5	18	70
1644	SO[1175]	-5658	190.5	18	70
1645	SO[1176]	-5670	85.5	18	70
1646	SO[1177]	-5682	295.5	18	70
1647	SO[1178]	-5694	190.5	18	70
1648	SO[1179]	-5706	85.5	18	70
1649	SO[1180]	-5718	295.5	18	70
1650	SO[1181]	-5730	190.5	18	70
1651	SO[1182]	-5742	85.5	18	70
1652	SO[1183]	-5754	295.5	18	70
1653	SO[1184]	-5766	190.5	18	70
1654	SO[1185]	-5778	85.5	18	70
1655	SO[1186]	-5790	295.5	18	70
1656	SO[1187]	-5802	190.5	18	70
1657	SO[1188]	-5814	85.5	18	70
1658	SO[1189]	-5826	295.5	18	70
1659	SO[1190]	-5838	190.5	18	70
1660	SO[1191]	-5850	85.5	18	70
1661	SO[1192]	-5862	295.5	18	70
1662	SO[1193]	-5874	190.5	18	70
1663	SO[1194]	-5886	85.5	18	70
1664	SO[1195]	-5898	295.5	18	70
1665	SO[1196]	-5910	190.5	18	70
1666	SO[1197]	-5922	85.5	18	70
1667	SO[1198]	-5934	295.5	18	70
1668	SO[1199]	-5946	190.5	18	70
1669	SO[1200]	-5958	85.5	18	70
1670	SO[1201]	-5970	295.5	18	70
1671	SO[1202]	-5982	190.5	18	70
1672	SO[1203]	-5994	85.5	18	70
1673	SO[1204]	-6006	295.5	18	70
1674	SO[1205]	-6018	190.5	18	70
1675	SO[1206]	-6030	85.5	18	70
1676	SO[1207]	-6042	295.5	18	70
1677	SO[1208]	-6054	190.5	18	70
1678	SO[1209]	-6066	85.5	18	70
1679	SO[1210]	-6078	295.5	18	70
1680	SO[1211]	-6090	190.5	18	70
1681	SO[1212]	-6102	85.5	18	70
1682	SO[1213]	-6114	295.5	18	70
1683	SO[1214]	-6126	190.5	18	70
1684	SO[1215]	-6138	85.5	18	70
1685	SO[1216]	-6150	295.5	18	70
1686	SO[1217]	-6162	190.5	18	70
1687	SO[1218]	-6174	85.5	18	70
1688	SO[1219]	-6186	295.5	18	70
1689	SO[1220]	-6198	190.5	18	70
1690	SO[1221]	-6210	85.5	18	70
1691	SO[1222]	-6222	295.5	18	70
1692	SO[1223]	-6234	190.5	18	70
1693	SO[1224]	-6246	85.5	18	70
1694	SO[1225]	-6258	295.5	18	70
1695	SO[1226]	-6270	190.5	18	70
1696	SO[1227]	-6282	85.5	18	70
1697	SO[1228]	-6294	295.5	18	70
1698	SO[1229]	-6306	190.5	18	70
1699	SO[1230]	-6318	85.5	18	70
1700	SO[1231]	-6330	295.5	18	70
1701	SO[1232]	-6342	190.5	18	70
1702	SO[1233]	-6354	85.5	18	70
1703	SO[1234]	-6366	295.5	18	70
1704	SO[1235]	-6378	190.5	18	70
1705	SO[1236]	-6390	85.5	18	70
1706	SO[1237]	-6402	295.5	18	70
1707	SO[1238]	-6414	190.5	18	70
1708	SO[1239]	-6426	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1709	SO[1240]	-6438	295.5	18	70
1710	SO[1241]	-6450	190.5	18	70
1711	SO[1242]	-6462	85.5	18	70
1712	SO[1243]	-6474	295.5	18	70
1713	SO[1244]	-6486	190.5	18	70
1714	SO[1245]	-6498	85.5	18	70
1715	SO[1246]	-6510	295.5	18	70
1716	SO[1247]	-6522	190.5	18	70
1717	SO[1248]	-6534	85.5	18	70
1718	SO[1249]	-6546	295.5	18	70
1719	SO[1250]	-6558	190.5	18	70
1720	SO[1251]	-6570	85.5	18	70
1721	SO[1252]	-6582	295.5	18	70
1722	SO[1253]	-6594	190.5	18	70
1723	SO[1254]	-6606	85.5	18	70
1724	SO[1255]	-6618	295.5	18	70
1725	SO[1256]	-6630	190.5	18	70
1726	SO[1257]	-6642	85.5	18	70
1727	SO[1258]	-6654	295.5	18	70
1728	SO[1259]	-6666	190.5	18	70
1729	SO[1260]	-6678	85.5	18	70
1730	SO[1261]	-6690	295.5	18	70
1731	SO[1262]	-6702	190.5	18	70
1732	SO[1263]	-6714	85.5	18	70
1733	SO[1264]	-6726	295.5	18	70
1734	SO[1265]	-6738	190.5	18	70
1735	SO[1266]	-6750	85.5	18	70
1736	SO[1267]	-6762	295.5	18	70
1737	SO[1268]	-6774	190.5	18	70
1738	SO[1269]	-6786	85.5	18	70
1739	SO[1270]	-6798	295.5	18	70
1740	SO[1271]	-6810	190.5	18	70
1741	SO[1272]	-6822	85.5	18	70
1742	SO[1273]	-6834	295.5	18	70
1743	SO[1274]	-6846	190.5	18	70
1744	SO[1275]	-6858	85.5	18	70
1745	SO[1276]	-6870	295.5	18	70
1746	SO[1277]	-6882	190.5	18	70
1747	SO[1278]	-6894	85.5	18	70
1748	SO[1279]	-6906	295.5	18	70
1749	SO[1280]	-6918	190.5	18	70
1750	SO[1281]	-6930	85.5	18	70
1751	SO[1282]	-6942	295.5	18	70
1752	SO[1283]	-6954	190.5	18	70
1753	SO[1284]	-6966	85.5	18	70
1754	SO[1285]	-6978	295.5	18	70
1755	SO[1286]	-6990	190.5	18	70
1756	SO[1287]	-7002	85.5	18	70
1757	SO[1288]	-7014	295.5	18	70
1758	SO[1289]	-7026	190.5	18	70
1759	SO[1290]	-7038	85.5	18	70
1760	SO[1291]	-7050	295.5	18	70
1761	SO[1292]	-7062	190.5	18	70
1762	SO[1293]	-7074	85.5	18	70
1763	SO[1294]	-7086	295.5	18	70
1764	SO[1295]	-7098	190.5	18	70
1765	SO[1296]	-7110	85.5	18	70
1766	SO[1297]	-7122	295.5	18	70
1767	SO[1298]	-7134	190.5	18	70
1768	SO[1299]	-7146	85.5	18	70
1769	SO[1300]	-7158	295.5	18	70
1770	SO[1301]	-7170	190.5	18	70
1771	SO[1302]	-7182	85.5	18	70
1772	SO[1303]	-7194	295.5	18	70
1773	SO[1304]	-7206	190.5	18	70
1774	SO[1305]	-7218	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1775	SO[1306]	-7230	295.5	18	70
1776	SO[1307]	-7242	190.5	18	70
1777	SO[1308]	-7254	85.5	18	70
1778	SO[1309]	-7266	295.5	18	70
1779	SO[1310]	-7278	190.5	18	70
1780	SO[1311]	-7290	85.5	18	70
1781	SO[1312]	-7302	295.5	18	70
1782	SO[1313]	-7314	190.5	18	70
1783	SO[1314]	-7326	85.5	18	70
1784	SO[1315]	-7338	295.5	18	70
1785	SO[1316]	-7350	190.5	18	70
1786	SO[1317]	-7362	85.5	18	70
1787	SO[1318]	-7374	295.5	18	70
1788	SO[1319]	-7386	190.5	18	70
1789	SO[1320]	-7398	85.5	18	70
1790	SO[1321]	-7410	295.5	18	70
1791	SO[1322]	-7422	190.5	18	70
1792	SO[1323]	-7434	85.5	18	70
1793	SO[1324]	-7446	295.5	18	70
1794	SO[1325]	-7458	190.5	18	70
1795	SO[1326]	-7470	85.5	18	70
1796	SO[1327]	-7482	295.5	18	70
1797	SO[1328]	-7494	190.5	18	70
1798	SO[1329]	-7506	85.5	18	70
1799	SO[1330]	-7518	295.5	18	70
1800	SO[1331]	-7530	190.5	18	70
1801	SO[1332]	-7542	85.5	18	70
1802	SO[1333]	-7554	295.5	18	70
1803	SO[1334]	-7566	190.5	18	70
1804	SO[1335]	-7578	85.5	18	70
1805	SO[1336]	-7590	295.5	18	70
1806	SO[1337]	-7602	190.5	18	70
1807	SO[1338]	-7614	85.5	18	70
1808	SO[1339]	-7626	295.5	18	70
1809	SO[1340]	-7638	190.5	18	70
1810	SO[1341]	-7650	85.5	18	70
1811	SO[1342]	-7662	295.5	18	70
1812	SO[1343]	-7674	190.5	18	70
1813	SO[1344]	-7686	85.5	18	70
1814	SO[1345]	-7698	295.5	18	70
1815	SO[1346]	-7710	190.5	18	70
1816	SO[1347]	-7722	85.5	18	70
1817	SO[1348]	-7734	295.5	18	70
1818	SO[1349]	-7746	190.5	18	70
1819	SO[1350]	-7758	85.5	18	70
1820	SO[1351]	-7770	295.5	18	70
1821	SO[1352]	-7782	190.5	18	70
1822	SO[1353]	-7794	85.5	18	70
1823	SO[1354]	-7806	295.5	18	70
1824	SO[1355]	-7818	190.5	18	70
1825	SO[1356]	-7830	85.5	18	70
1826	SO[1357]	-7842	295.5	18	70
1827	SO[1358]	-7854	190.5	18	70
1828	SO[1359]	-7866	85.5	18	70
1829	SO[1360]	-7878	295.5	18	70
1830	SO[1361]	-7890	190.5	18	70
1831	SO[1362]	-7902	85.5	18	70
1832	SO[1363]	-7914	295.5	18	70
1833	SO[1364]	-7926	190.5	18	70
1834	SO[1365]	-7938	85.5	18	70
1835	SO[1366]	-7950	295.5	18	70
1836	SO[1367]	-7962	190.5	18	70
1837	SO[1368]	-7974	85.5	18	70
1838	SO[1369]	-7986	295.5	18	70
1839	SO[1370]	-7998	190.5	18	70
1840	SO[1371]	-8010	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1841	SO[1372]	-8022	295.5	18	70
1842	SO[1373]	-8034	190.5	18	70
1843	SO[1374]	-8046	85.5	18	70
1844	SO[1375]	-8058	295.5	18	70
1845	SO[1376]	-8070	190.5	18	70
1846	SO[1377]	-8082	85.5	18	70
1847	SO[1378]	-8094	295.5	18	70
1848	SO[1379]	-8106	190.5	18	70
1849	SO[1380]	-8118	85.5	18	70
1850	SO[1381]	-8130	295.5	18	70
1851	SO[1382]	-8142	190.5	18	70
1852	SO[1383]	-8154	85.5	18	70
1853	SO[1384]	-8166	295.5	18	70
1854	SO[1385]	-8178	190.5	18	70
1855	SO[1386]	-8190	85.5	18	70
1856	SO[1387]	-8202	295.5	18	70
1857	SO[1388]	-8214	190.5	18	70
1858	SO[1389]	-8226	85.5	18	70
1859	SO[1390]	-8238	295.5	18	70
1860	SO[1391]	-8250	190.5	18	70
1861	SO[1392]	-8262	85.5	18	70
1862	SO[1393]	-8274	295.5	18	70
1863	SO[1394]	-8286	190.5	18	70
1864	SO[1395]	-8298	85.5	18	70
1865	SO[1396]	-8310	295.5	18	70
1866	SO[1397]	-8322	190.5	18	70
1867	SO[1398]	-8334	85.5	18	70
1868	SO[1399]	-8346	295.5	18	70
1869	SO[1400]	-8358	190.5	18	70
1870	SO[1401]	-8370	85.5	18	70
1871	SO[1402]	-8382	295.5	18	70
1872	SO[1403]	-8394	190.5	18	70
1873	SO[1404]	-8406	85.5	18	70
1874	SO[1405]	-8418	295.5	18	70
1875	SO[1406]	-8430	190.5	18	70
1876	SO[1407]	-8442	85.5	18	70
1877	SO[1408]	-8454	295.5	18	70
1878	SO[1409]	-8466	190.5	18	70
1879	SO[1410]	-8478	85.5	18	70
1880	SO[1411]	-8490	295.5	18	70
1881	SO[1412]	-8502	190.5	18	70
1882	SO[1413]	-8514	85.5	18	70
1883	SO[1414]	-8526	295.5	18	70
1884	SO[1415]	-8538	190.5	18	70
1885	SO[1416]	-8550	85.5	18	70
1886	SO[1417]	-8562	295.5	18	70
1887	SO[1418]	-8574	190.5	18	70
1888	SO[1419]	-8586	85.5	18	70
1889	SO[1420]	-8598	295.5	18	70
1890	SO[1421]	-8610	190.5	18	70
1891	SO[1422]	-8622	85.5	18	70
1892	SO[1423]	-8634	295.5	18	70
1893	SO[1424]	-8646	190.5	18	70
1894	SO[1425]	-8658	85.5	18	70
1895	SO[1426]	-8670	295.5	18	70
1896	SO[1427]	-8682	190.5	18	70
1897	SO[1428]	-8694	85.5	18	70
1898	SO[1429]	-8706	295.5	18	70
1899	SO[1430]	-8718	190.5	18	70
1900	SO[1431]	-8730	85.5	18	70
1901	SO[1432]	-8742	295.5	18	70
1902	SO[1433]	-8754	190.5	18	70
1903	SO[1434]	-8766	85.5	18	70
1904	SO[1435]	-8778	295.5	18	70
1905	SO[1436]	-8790	190.5	18	70
1906	SO[1437]	-8802	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1907	SO[1438]	-8814	295.5	18	70
1908	SO[1439]	-8826	190.5	18	70
1909	SO[1440]	-8838	85.5	18	70
1910	SO[1441]	-8850	295.5	18	70
1911	SO[1442]	-8862	190.5	18	70
1912	SO[1443]	-8874	85.5	18	70
1913	SO[1444]	-8886	295.5	18	70
1914	SO[1445]	-8898	190.5	18	70
1915	SO[1446]	-8910	85.5	18	70
1916	SO[1447]	-8922	295.5	18	70
1917	SO[1448]	-8934	190.5	18	70
1918	SO[1449]	-8946	85.5	18	70
1919	SO[1450]	-8958	295.5	18	70
1920	SO[1451]	-8970	190.5	18	70
1921	SO[1452]	-8982	85.5	18	70
1922	SO[1453]	-8994	295.5	18	70
1923	SO[1454]	-9006	190.5	18	70
1924	SO[1455]	-9018	85.5	18	70
1925	SO[1456]	-9030	295.5	18	70
1926	SO[1457]	-9042	190.5	18	70
1927	SO[1458]	-9054	85.5	18	70
1928	SO[1459]	-9066	295.5	18	70
1929	SO[1460]	-9078	190.5	18	70
1930	SO[1461]	-9090	85.5	18	70
1931	SO[1462]	-9102	295.5	18	70
1932	SO[1463]	-9114	190.5	18	70
1933	SO[1464]	-9126	85.5	18	70
1934	SO[1465]	-9138	295.5	18	70
1935	SO[1466]	-9150	190.5	18	70
1936	SO[1467]	-9162	85.5	18	70
1937	SO[1468]	-9174	295.5	18	70
1938	SO[1469]	-9186	190.5	18	70
1939	SO[1470]	-9198	85.5	18	70
1940	SO[1471]	-9210	295.5	18	70
1941	SO[1472]	-9222	190.5	18	70
1942	SO[1473]	-9234	85.5	18	70
1943	SO[1474]	-9246	295.5	18	70
1944	SO[1475]	-9258	190.5	18	70
1945	SO[1476]	-9270	85.5	18	70
1946	SO[1477]	-9282	295.5	18	70
1947	SO[1478]	-9294	190.5	18	70
1948	SO[1479]	-9306	85.5	18	70
1949	SO[1480]	-9318	295.5	18	70
1950	SO[1481]	-9330	190.5	18	70
1951	SO[1482]	-9342	85.5	18	70
1952	SO[1483]	-9354	295.5	18	70
1953	SO[1484]	-9366	190.5	18	70
1954	SO[1485]	-9378	85.5	18	70
1955	SO[1486]	-9390	295.5	18	70
1956	SO[1487]	-9402	190.5	18	70
1957	SO[1488]	-9414	85.5	18	70
1958	SO[1489]	-9426	295.5	18	70
1959	SO[1490]	-9438	190.5	18	70
1960	SO[1491]	-9450	85.5	18	70
1961	SO[1492]	-9462	295.5	18	70
1962	SO[1493]	-9474	190.5	18	70
1963	SO[1494]	-9486	85.5	18	70
1964	SO[1495]	-9498	295.5	18	70
1965	SO[1496]	-9510	190.5	18	70
1966	SO[1497]	-9522	85.5	18	70
1967	SO[1498]	-9534	295.5	18	70
1968	SO[1499]	-9546	190.5	18	70
1969	SO[1500]	-9558	85.5	18	70
1970	SO[1501]	-9570	295.5	18	70
1971	SO[1502]	-9582	190.5	18	70
1972	SO[1503]	-9594	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
1973	SO[1504]	-9606	295.5	18	70
1974	SO[1505]	-9618	190.5	18	70
1975	SO[1506]	-9630	85.5	18	70
1976	SO[1507]	-9642	295.5	18	70
1977	SO[1508]	-9654	190.5	18	70
1978	SO[1509]	-9666	85.5	18	70
1979	SO[1510]	-9678	295.5	18	70
1980	SO[1511]	-9690	190.5	18	70
1981	SO[1512]	-9702	85.5	18	70
1982	SO[1513]	-9714	295.5	18	70
1983	SO[1514]	-9726	190.5	18	70
1984	SO[1515]	-9738	85.5	18	70
1985	SO[1516]	-9750	295.5	18	70
1986	SO[1517]	-9762	190.5	18	70
1987	SO[1518]	-9774	85.5	18	70
1988	SO[1519]	-9786	295.5	18	70
1989	SO[1520]	-9798	190.5	18	70
1990	SO[1521]	-9810	85.5	18	70
1991	SO[1522]	-9822	295.5	18	70
1992	SO[1523]	-9834	190.5	18	70
1993	SO[1524]	-9846	85.5	18	70
1994	SO[1525]	-9858	295.5	18	70
1995	SO[1526]	-9870	190.5	18	70
1996	SO[1527]	-9882	85.5	18	70
1997	SO[1528]	-9894	295.5	18	70
1998	SO[1529]	-9906	190.5	18	70
1999	SO[1530]	-9918	85.5	18	70
2000	SO[1531]	-9930	295.5	18	70
2001	SO[1532]	-9942	190.5	18	70
2002	SO[1533]	-9954	85.5	18	70
2003	SO[1534]	-9966	295.5	18	70
2004	SO[1535]	-9978	190.5	18	70
2005	SO[1536]	-9990	85.5	18	70
2006	SO[1537]	-10002	295.5	18	70
2007	SO[1538]	-10014	190.5	18	70
2008	SO[1539]	-10026	85.5	18	70
2009	SO[1540]	-10038	295.5	18	70
2010	SO[1541]	-10050	190.5	18	70
2011	SO[1542]	-10062	85.5	18	70
2012	SO[1543]	-10074	295.5	18	70
2013	SO[1544]	-10086	190.5	18	70
2014	SO[1545]	-10098	85.5	18	70
2015	SO[1546]	-10110	295.5	18	70
2016	SO[1547]	-10122	190.5	18	70
2017	SO[1548]	-10134	85.5	18	70
2018	SO[1549]	-10146	295.5	18	70
2019	SO[1550]	-10158	190.5	18	70
2020	SO[1551]	-10170	85.5	18	70
2021	SO[1552]	-10182	295.5	18	70
2022	SO[1553]	-10194	190.5	18	70
2023	SO[1554]	-10206	85.5	18	70
2024	SO[1555]	-10218	295.5	18	70
2025	SO[1556]	-10230	190.5	18	70
2026	SO[1557]	-10242	85.5	18	70
2027	SO[1558]	-10254	295.5	18	70
2028	SO[1559]	-10266	190.5	18	70
2029	SO[1560]	-10278	85.5	18	70
2030	SO[1561]	-10290	295.5	18	70
2031	SO[1562]	-10302	190.5	18	70
2032	SO[1563]	-10314	85.5	18	70
2033	SO[1564]	-10326	295.5	18	70
2034	SO[1565]	-10338	190.5	18	70
2035	SO[1566]	-10350	85.5	18	70
2036	SO[1567]	-10362	295.5	18	70
2037	SO[1568]	-10374	190.5	18	70
2038	SO[1569]	-10386	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
2039	SO[1570]	-10398	295.5	18	70
2040	SO[1571]	-10410	190.5	18	70
2041	SO[1572]	-10422	85.5	18	70
2042	SO[1573]	-10434	295.5	18	70
2043	SO[1574]	-10446	190.5	18	70
2044	SO[1575]	-10458	85.5	18	70
2045	SO[1576]	-10470	295.5	18	70
2046	SO[1577]	-10482	190.5	18	70
2047	SO[1578]	-10494	85.5	18	70
2048	SO[1579]	-10506	295.5	18	70
2049	SO[1580]	-10518	190.5	18	70
2050	SO[1581]	-10530	85.5	18	70
2051	SO[1582]	-10542	295.5	18	70
2052	SO[1583]	-10554	190.5	18	70
2053	SO[1584]	-10566	85.5	18	70
2054	SO[1585]	-10578	295.5	18	70
2055	SO[1586]	-10590	190.5	18	70
2056	SO[1587]	-10602	85.5	18	70
2057	SO[1588]	-10614	295.5	18	70
2058	SO[1589]	-10626	190.5	18	70
2059	SO[1590]	-10638	85.5	18	70
2060	SO[1591]	-10650	295.5	18	70
2061	SO[1592]	-10662	190.5	18	70
2062	SO[1593]	-10674	85.5	18	70
2063	SO[1594]	-10686	295.5	18	70
2064	SO[1595]	-10698	190.5	18	70
2065	SO[1596]	-10710	85.5	18	70
2066	SO[1597]	-10722	295.5	18	70
2067	SO[1598]	-10734	190.5	18	70
2068	SO[1599]	-10746	85.5	18	70
2069	SO[1600]	-10758	295.5	18	70
2070	SO[1601]	-10770	190.5	18	70
2071	SO[1602]	-10782	85.5	18	70
2072	SO[1603]	-10794	295.5	18	70
2073	SO[1604]	-10806	190.5	18	70
2074	SO[1605]	-10818	85.5	18	70
2075	SO[1606]	-10830	295.5	18	70
2076	SO[1607]	-10842	190.5	18	70
2077	SO[1608]	-10854	85.5	18	70
2078	SO[1609]	-10866	295.5	18	70
2079	SO[1610]	-10878	190.5	18	70
2080	SO[1611]	-10890	85.5	18	70
2081	SO[1612]	-10902	295.5	18	70
2082	SO[1613]	-10914	190.5	18	70
2083	SO[1614]	-10926	85.5	18	70
2084	SO[1615]	-10938	295.5	18	70
2085	SO[1616]	-10950	190.5	18	70
2086	SO[1617]	-10962	85.5	18	70
2087	SO[1618]	-10974	295.5	18	70
2088	SO[1619]	-10986	190.5	18	70
2089	SO[1620]	-10998	85.5	18	70
2090	SO[1621]	-11010	295.5	18	70
2091	SO[1622]	-11022	190.5	18	70
2092	SO[1623]	-11034	85.5	18	70
2093	SO[1624]	-11046	295.5	18	70
2094	SO[1625]	-11058	190.5	18	70
2095	SO[1626]	-11070	85.5	18	70
2096	SO[1627]	-11082	295.5	18	70
2097	SO[1628]	-11094	190.5	18	70
2098	SO[1629]	-11106	85.5	18	70
2099	SO[1630]	-11118	295.5	18	70
2100	SO[1631]	-11130	190.5	18	70
2101	SO[1632]	-11142	85.5	18	70
2102	SO[1633]	-11154	295.5	18	70
2103	SO[1634]	-11166	190.5	18	70
2104	SO[1635]	-11178	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
2105	SO[1636]	-11190	295.5	18	70
2106	SO[1637]	-11202	190.5	18	70
2107	SO[1638]	-11214	85.5	18	70
2108	SO[1639]	-11226	295.5	18	70
2109	SO[1640]	-11238	190.5	18	70
2110	SO[1641]	-11250	85.5	18	70
2111	SO[1642]	-11262	295.5	18	70
2112	SO[1643]	-11274	190.5	18	70
2113	SO[1644]	-11286	85.5	18	70
2114	SO[1645]	-11298	295.5	18	70
2115	SO[1646]	-11310	190.5	18	70
2116	SO[1647]	-11322	85.5	18	70
2117	SO[1648]	-11334	295.5	18	70
2118	SO[1649]	-11346	190.5	18	70
2119	SO[1650]	-11358	85.5	18	70
2120	SO[1651]	-11370	295.5	18	70
2121	SO[1652]	-11382	190.5	18	70
2122	SO[1653]	-11394	85.5	18	70
2123	SO[1654]	-11406	295.5	18	70
2124	SO[1655]	-11418	190.5	18	70
2125	SO[1656]	-11430	85.5	18	70
2126	SO[1657]	-11442	295.5	18	70
2127	SO[1658]	-11454	190.5	18	70
2128	SO[1659]	-11466	85.5	18	70
2129	SO[1660]	-11478	295.5	18	70
2130	SO[1661]	-11490	190.5	18	70
2131	SO[1662]	-11502	85.5	18	70
2132	SO[1663]	-11514	295.5	18	70
2133	SO[1664]	-11526	190.5	18	70
2134	SO[1665]	-11538	85.5	18	70
2135	SO[1666]	-11550	295.5	18	70
2136	SO[1667]	-11562	190.5	18	70
2137	SO[1668]	-11574	85.5	18	70
2138	SO[1669]	-11586	295.5	18	70
2139	SO[1670]	-11598	190.5	18	70
2140	SO[1671]	-11610	85.5	18	70
2141	SO[1672]	-11622	295.5	18	70
2142	SO[1673]	-11634	190.5	18	70
2143	SO[1674]	-11646	85.5	18	70
2144	SO[1675]	-11658	295.5	18	70
2145	SO[1676]	-11670	190.5	18	70
2146	SO[1677]	-11682	85.5	18	70
2147	SO[1678]	-11694	295.5	18	70
2148	SO[1679]	-11706	190.5	18	70
2149	SO[1680]	-11718	85.5	18	70
2150	SO[1681]	-11730	295.5	18	70
2151	SO[1682]	-11742	190.5	18	70
2152	SO[1683]	-11754	85.5	18	70
2153	SO[1684]	-11766	295.5	18	70
2154	SO[1685]	-11778	190.5	18	70
2155	SO[1686]	-11790	85.5	18	70
2156	SO[1687]	-11802	295.5	18	70
2157	SO[1688]	-11814	190.5	18	70
2158	SO[1689]	-11826	85.5	18	70
2159	SO[1690]	-11838	295.5	18	70
2160	SO[1691]	-11850	190.5	18	70
2161	SO[1692]	-11862	85.5	18	70
2162	SO[1693]	-11874	295.5	18	70
2163	SO[1694]	-11886	190.5	18	70
2164	SO[1695]	-11898	85.5	18	70
2165	SO[1696]	-11910	295.5	18	70
2166	SO[1697]	-11922	190.5	18	70
2167	SO[1698]	-11934	85.5	18	70
2168	SO[1699]	-11946	295.5	18	70
2169	SO[1700]	-11958	190.5	18	70
2170	SO[1701]	-11970	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
2171	SO[1702]	-11982	295.5	18	70
2172	SO[1703]	-11994	190.5	18	70
2173	SO[1704]	-12006	85.5	18	70
2174	SO[1705]	-12018	295.5	18	70
2175	SO[1706]	-12030	190.5	18	70
2176	SO[1707]	-12042	85.5	18	70
2177	SO[1708]	-12054	295.5	18	70
2178	SO[1709]	-12066	190.5	18	70
2179	SO[1710]	-12078	85.5	18	70
2180	SO[1711]	-12090	295.5	18	70
2181	SO[1712]	-12102	190.5	18	70
2182	SO[1713]	-12114	85.5	18	70
2183	SO[1714]	-12126	295.5	18	70
2184	SO[1715]	-12138	190.5	18	70
2185	SO[1716]	-12150	85.5	18	70
2186	SO[1717]	-12162	295.5	18	70
2187	SO[1718]	-12174	190.5	18	70
2188	SO[1719]	-12186	85.5	18	70
2189	SO[1720]	-12198	295.5	18	70
2190	SO[1721]	-12210	190.5	18	70
2191	SO[1722]	-12222	85.5	18	70
2192	SO[1723]	-12234	295.5	18	70
2193	SO[1724]	-12246	190.5	18	70
2194	SO[1725]	-12258	85.5	18	70
2195	SO[1726]	-12270	295.5	18	70
2196	SO[1727]	-12282	190.5	18	70
2197	SO[1728]	-12294	85.5	18	70
2198	SO[1729]	-12306	295.5	18	70
2199	SO[1730]	-12318	190.5	18	70
2200	SO[1731]	-12330	85.5	18	70
2201	SO[1732]	-12342	295.5	18	70
2202	SO[1733]	-12354	190.5	18	70
2203	SO[1734]	-12366	85.5	18	70
2204	SO[1735]	-12378	295.5	18	70
2205	SO[1736]	-12390	190.5	18	70
2206	SO[1737]	-12402	85.5	18	70
2207	SO[1738]	-12414	295.5	18	70
2208	SO[1739]	-12426	190.5	18	70
2209	SO[1740]	-12438	85.5	18	70
2210	SO[1741]	-12450	295.5	18	70
2211	SO[1742]	-12462	190.5	18	70
2212	SO[1743]	-12474	85.5	18	70
2213	SO[1744]	-12486	295.5	18	70
2214	SO[1745]	-12498	190.5	18	70
2215	SO[1746]	-12510	85.5	18	70
2216	SO[1747]	-12522	295.5	18	70
2217	SO[1748]	-12534	190.5	18	70
2218	SO[1749]	-12546	85.5	18	70
2219	SO[1750]	-12558	295.5	18	70
2220	SO[1751]	-12570	190.5	18	70
2221	SO[1752]	-12582	85.5	18	70
2222	SO[1753]	-12594	295.5	18	70
2223	SO[1754]	-12606	190.5	18	70
2224	SO[1755]	-12618	85.5	18	70
2225	SO[1756]	-12630	295.5	18	70
2226	SO[1757]	-12642	190.5	18	70
2227	SO[1758]	-12654	85.5	18	70
2228	SO[1759]	-12666	295.5	18	70
2229	SO[1760]	-12678	190.5	18	70
2230	SO[1761]	-12690	85.5	18	70
2231	SO[1762]	-12702	295.5	18	70
2232	SO[1763]	-12714	190.5	18	70
2233	SO[1764]	-12726	85.5	18	70
2234	SO[1765]	-12738	295.5	18	70
2235	SO[1766]	-12750	190.5	18	70
2236	SO[1767]	-12762	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
2237	SO[1768]	-12774	295.5	18	70
2238	SO[1769]	-12786	190.5	18	70
2239	SO[1770]	-12798	85.5	18	70
2240	SO[1771]	-12810	295.5	18	70
2241	SO[1772]	-12822	190.5	18	70
2242	SO[1773]	-12834	85.5	18	70
2243	SO[1774]	-12846	295.5	18	70
2244	SO[1775]	-12858	190.5	18	70
2245	SO[1776]	-12870	85.5	18	70
2246	SO[1777]	-12882	295.5	18	70
2247	SO[1778]	-12894	190.5	18	70
2248	SO[1779]	-12906	85.5	18	70
2249	SO[1780]	-12918	295.5	18	70
2250	SO[1781]	-12930	190.5	18	70
2251	SO[1782]	-12942	85.5	18	70
2252	SO[1783]	-12954	295.5	18	70
2253	SO[1784]	-12966	190.5	18	70
2254	SO[1785]	-12978	85.5	18	70
2255	SO[1786]	-12990	295.5	18	70
2256	SO[1787]	-13002	190.5	18	70
2257	SO[1788]	-13014	85.5	18	70
2258	SO[1789]	-13026	295.5	18	70
2259	SO[1790]	-13038	190.5	18	70
2260	SO[1791]	-13050	85.5	18	70
2261	SO[1792]	-13062	295.5	18	70
2262	SO[1793]	-13074	190.5	18	70
2263	SO[1794]	-13086	85.5	18	70
2264	SO[1795]	-13098	295.5	18	70
2265	SO[1796]	-13110	190.5	18	70
2266	SO[1797]	-13122	85.5	18	70
2267	SO[1798]	-13134	295.5	18	70
2268	SO[1799]	-13146	190.5	18	70
2269	SO[1800]	-13158	85.5	18	70

Pad No	Pin Name	X-pos	Y-pos	X-size	Y-size
2270	SO[1801]	-13170	295.5	18	70
2271	SO[1802]	-13182	190.5	18	70
2272	SHIELDING_AGND	-13194	85.5	18	70
2273	COM5_IN	-13206	295.5	18	70
2274	SHIELDING_AGND	-13218	190.5	18	70
2275	SHIELDING_AGND	-13230	85.5	18	70
2276	COM5_OUT	-13242	295.5	18	70
2277	SHIELDING_AGND	-13254	190.5	18	70
2278	RPI_EVEN	-13314	310.5	40	40
2279	RPI_EVEN	-13394	310.5	40	40
2280	COMR1_OUT	-13474	310.5	40	40
2281	COMR1_OUT	-13554	310.5	40	40
2282	COMR2_OUT	-13634	310.5	40	40
2283	COMR2_OUT	-13714	310.5	40	40
2284	SHIELDING_AGND	-13794	310.5	40	40
2285	SHIELDING_AGND	-13874	310.5	40	40
2286	SHIELDING_AGND	-13954	310.5	40	40
2287	XONR	-14093	320.5	120	20
2288	OEVR	-14093	282.5	120	20
2289	UDR	-14093	244.5	120	20
2290	CKVR	-14093	206.5	120	20
2291	STV2R	-14093	168.5	120	20
2292	STV1R	-14093	130.5	120	20
2293	SYNC6R	-14093	92.5	120	20
2294	SYNC5R	-14093	54.5	120	20
2295	SYNC4R	-14093	16.5	120	20
2296	SYNC3R	-14093	-21.5	120	20
2297	SYNC2R	-14093	-59.5	120	20
2298	SYNC1R	-14093	-97.5	120	20
	Left Alignment Mark	-14095.5	-273	115	115
	Right Alignment Mark	14095.5	-273	115	115

17. Appendix A : BIST pattern

R→ G → B → Black → White → Color Bar → Horizontal 256 gray scale → Vertical 256 gray scale → Crosstalk pattern → Chess board (L255/L0) → Flicker pattern → White border → L32 gray →L64 gray →L128 gray → RGBW → Pixel chess board
Note: 18,19 and 20 are not in the automation sequence.

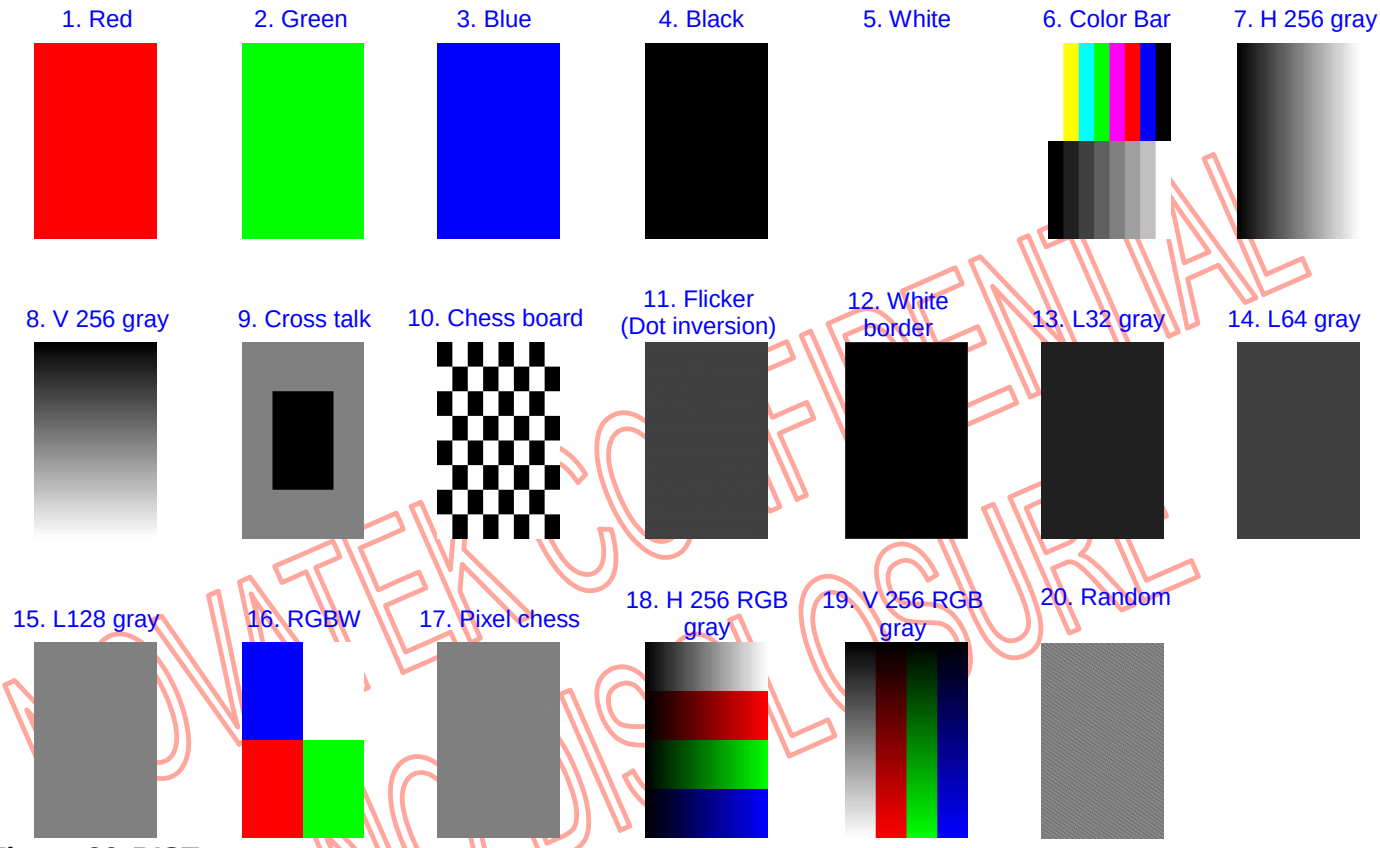


Figure 36. BIST pattern

18. Important Notice

The Company shall make use of the Confidential Information solely for the Purpose. The Company is prohibited from using the Confidential Information other than the Purpose, including but not limited to the human life safety related to, such as Aviation navigation systems, Surgical instruments, Military equipments, Automotive Driver Safety Assistant System etc.