Smart USB Charging Port Controller

General Description

The NT6008 is a smart USB interface IC specifically designed for high voltage dedicated charging port applications (HVDCP) that complies with Qualcomm™ QC 2.0/3.0 class A specification. The NT6008 accurately adjusts HVDCP output voltage according to request of the handheld devices so that the chaging time can be 75% faster.

The NT6008 automatically identifies the handheld devices attached to the USB port. Then it emulates the original chargers accordingly so that the attached device can draw maximum current from the charging port.

The NT6008 supports Apple iPad, Apple iPhone, Samsung Galaxy Note, BC1.2 or YD/T 1591 compliant devices, and majority of modern portable devices.

The NT6008 is available in TSOT23-8L and MSOP-10L packages.

Note: QC2.0, QC3.0, Apple, iPad, iPhone, Samsung and Galaxy Note are trademarks belonging to their respective owners.

Applications

- **CLA Car Chargers**
- **Computer Peripherals**
- **Wall Adaptors**
- **USB Power Plugs**
- **Portable Power Banks**

Features

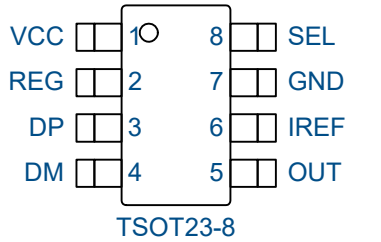
- **3.3V ~ 12.6V Single Supply Operation**
- **Smart USB Charger Identification Circuit**
  - **Compliant with QC 2.0/3.0 Class A**
  - **Support Apple 2.1A/2.4A Applications**
  - **Support Samsung Galaxy Note 2.0A Applications**
  - **Support BC1.2 & YD/T 1591 Battery Charging Specifications**
- **Output Voltage Discharge Function**
- **Output Over Voltage Protection**
- **8kV High ESD**
- **-40°C ~ +125°C Operating Ambient Temperature**
- **TSOT23-8L or MSOP-10L Package**
- **RoHS Compliant and Halogen-Free**

Ordering Information

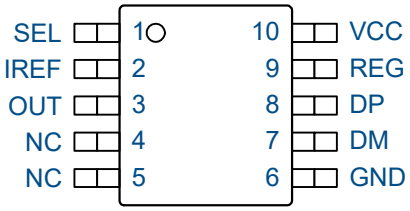
Order Number	Package	Top Marking
NT6008AMT8	TSOT23-8L	N03
NT6008ARAA	MSOP-10L	NT6008A

Note: NT products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

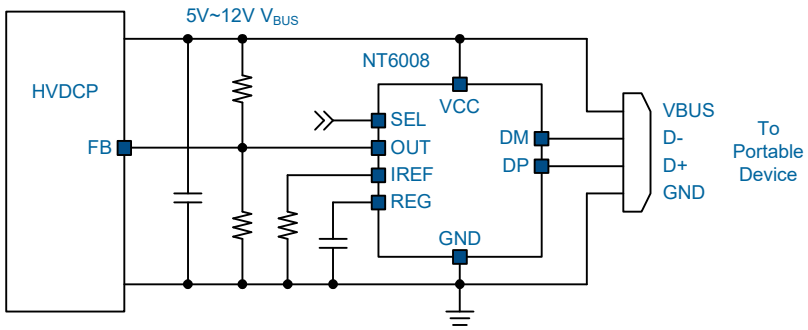
Pin Configuration & Typical Application Circuit



TSOT23-8



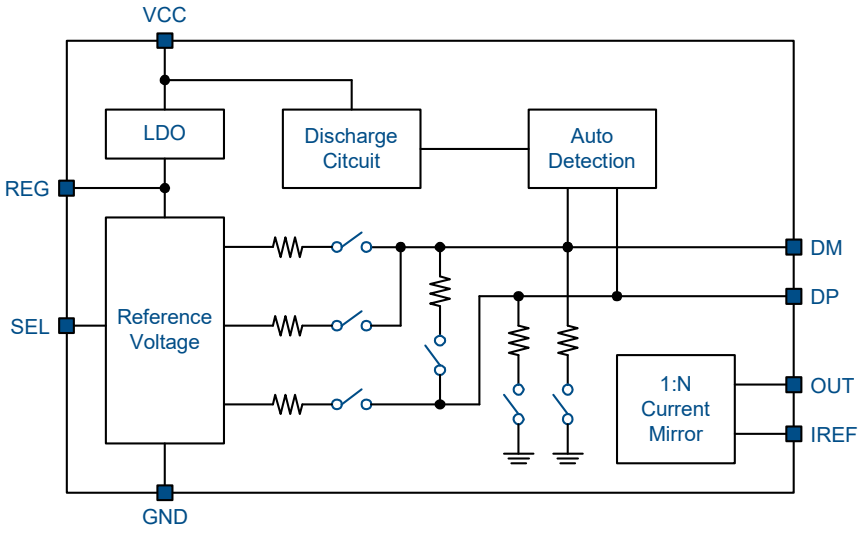
MSOP-10L



Functional Pin Description

Pin No.		Pin Name	Pin Function
MSOP-10L	SOT23-8L		
1	8	SEL	Mode Selection.Logic low selects Apple 2.4A mode, logic high selects Apple 2.1A mode. Do not let this pin floating.
2	6	IREF	Reference Current Setting
3	5	OUT	Current Sink/Source Output
4, 5	NA	NC	Not Internally Connected
6	7	GND	Ground
7	4	DM	Negative Data Line
8	3	DP	Positive Data Line
9	2	REG	Bypass for Internal LDO Output.
10	1	VCC	Supply Input

Functional Block Diagram



Functional Description

The NT6008 is a smart USB interface IC specifically designed for high-voltage dedicated charging port applications. The NT6008 automatically identifies the handheld devices attached to the USB port. Then it emulates the genuine chargers accordingly so that the attached device can draw maximum current from the charging port with demanded output voltage.

DM/DP Configuration

The DM/DP have four configurations, mode 1 ~ mode 4, as shown in Figure 1 ~ Figure 4. The NT6008 automatically selects configurations according to the DP/DM status and pre-defined timing so that the attached portable device can be quickly charged.

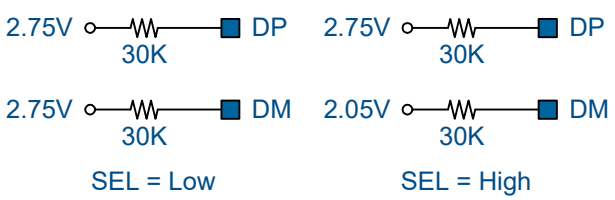


Figure 1. Mode 1 Configuration.

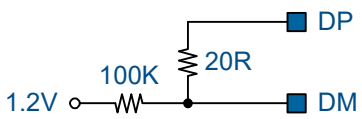


Figure 2. Mode 2 Configuration.

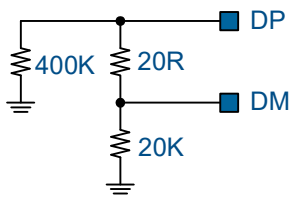


Figure 3. Mode 3 Configuration.

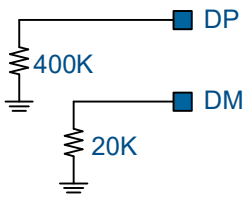


Figure 4. Mode 4 Configuration.

Mode 1 Configuration

Mode 1 is the default configuration when supply input is above the power on reset (POR) level. The NT6008 leaves mode 1 and enters mode 2 if one of the three conditions is true: 1.) $V_{DP} > V_{DP-0}$ for 2ms; 2.) $V_{DM} < V_{DM-1}$ for 10ms or 3.) $V_{DP} < V_{DP-1}$ for 10ms.

When entering mode 2, the NT6008 resets the internal 3-second counter.

Mode 2 Configuration

The NT6008 leaves mode 2 under two conditions:

1.) enters mode 3 if $V_{DP-3} < V_{DP} < V_{DP-2}$ for one second.

2.) otherwise enters mode 1 when the 3-second counter expires.

Mode 3 Configuration

The NT6008 leaves mode 3 under two conditions:

1.) enters mode 4 if $V_{DP-3} < V_{DP} < V_{DP-2}$ for 0.2s.

2.) otherwise enters mode 1 when the 3-second counter expires.

Mode 4 Configuration

The NT6008 leaves mode 4 and enter mode 1 if $V_{DP-3} > V_{DP}$ for 2ms or VCC overvoltage protection is triggered.

At mode 4, the NT6008 keeps monitoring V_{DM} voltage. Once $V_{DM} < V_{DM-5}$ for longer than 2ms, the OUT pin will sink or source a current I_{OUT} according to DP/DM voltages and the reference current I_{REF} set by the resistor connected to IREF pin. Table 1 illustrates the relationship between I_{OUT} and DP/DM voltages.

Table 1. I_{OUT} vs. DP/DM voltages relationship

V_{DP}	V_{DM}	I_{OUT}
$V_{DP} < V_{DP-5}$	X	Enter mode 1
$V_{DP-5} < V_{DP}$	$V_{DM} < V_{DM-5}$	0A
$V_{DP-4} < V_{DP} < V_{DP-4}$	$V_{DM-5} < V_{DM} < V_{DM-4}$	7 * I_{REF}
$V_{DP-5} < V_{DP} < V_{DP-4}$	$V_{DM} > V_{DP-4}$	Continuous mode
$V_{DP} > V_{DP-4}$	$V_{DM-5} < V_{DM} < V_{DM-4}$	4 * I_{REF}
$V_{DP} > V_{DP-4}$	$V_{DM} > V_{DM-4}$	Keep last state

Functional Description

Reference Current & Current Sink

Use a resistor R_{IREF} connected to IREF pin to set the reference current as:

$$I_{REF} = \frac{1.0V}{R_{REF}}$$

When selected by V_{DM}/V_{DM}, the OUT pin will ramp up/ down the sinking current to its target level with steps of $1/10*I_{REF}$ incremental, 50us per step.

Incremental I_{OUT}

When $V_{DP-5} < V_{DP} < V_{DP-4}$ and $V_{DM} > V_{DM-4}$, the NT6008 enters continuous mode. Upon each DP positive pulse with 150us delay time, the NT6008 increases output sinking current by 0.2 x I_{REF} as shown in Figure 5. Pulsewidth shorter than 150us will be skipped. The maximum output sinking current is limited at 7.0 x I_{REF} that will set the HVDCP output voltage 7V higher than nominal level.

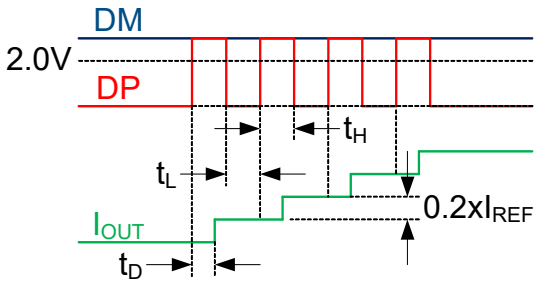


Figure 5. Incremental I_{OUT}.

Decremental I_{OUT}

Upon each DM negative pulse with 150us delay time, the NT6008 decreases output sinking current (increases output sourcing current) by 0.2 x I_{REF} as shown in Figure 6. Pulsewidth shorter than 150us will be skipped. The minimum output sinking current is limited at -1.4 x I_{REF} (1.4 x I_{REF} sourcing) that will set the HVDCP output voltage 1.4V lower than nominal level.

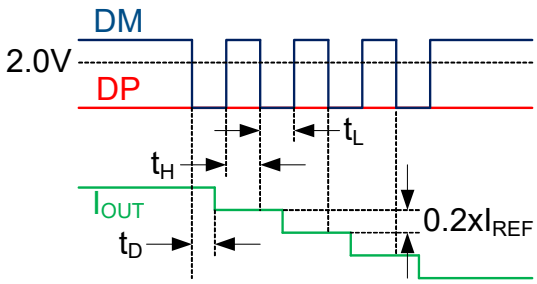


Figure 6. Decremental I_{OUT}.

Over Voltage Protection

If VCC is higher than 13.0V for 100us, over voltage protection (OVP) is triggered. OVP turns off the current sink and resets the DP/DM to mode 1 configuration.

Output Voltage Discharge

When the current sink decreases, the NT6008 sinks a 10mA current from the VCC pin for 500ms to discharge the output voltage of HVDCP to a safe level.

Absolute Maximum Rating

(Note1)

Supply Input Voltage, V_{CC} ---------- -0.3V to +13.2V
Other Pins ---------- +0.3V to 7V
Storage Temperature Range ---------- -55°C to +150°C
Operation Temperature Range ---------- -40°C to +125°C
Lead Temperature Range (Soldering 10sec) ---------- 260°C

ESD Rating (Note2)

MM (Machine Mode), DP and DM ---------- 800V
MM (Machine Mode), other pins ---------- 200V
HBM (Human Body Mode), DP and DM ---------- 8kV
HBM (Human Body Mode), other pins ---------- 2kV

Thermal Information

Package Thermal Resistance (Note3)

TSOT23-8L θ_{JA} ---------- 250°C/W
MSOP-10L θ_{JA} ---------- TBD
TSOT23-8L θ_{JC} ---------- 100°C/W
MSOP-10L θ_{JC} ---------- TBD

Power Dissipation, P_D @ T_A = 25°C

TSOT23-8L ---------- 0.4W
MSOP-10L ---------- TBD

Recommended Operating Conditions

Operating Junction Temperature Range (Note4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +125°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{CC} = 5V, T_A = +25°C unless otherwise specified.)

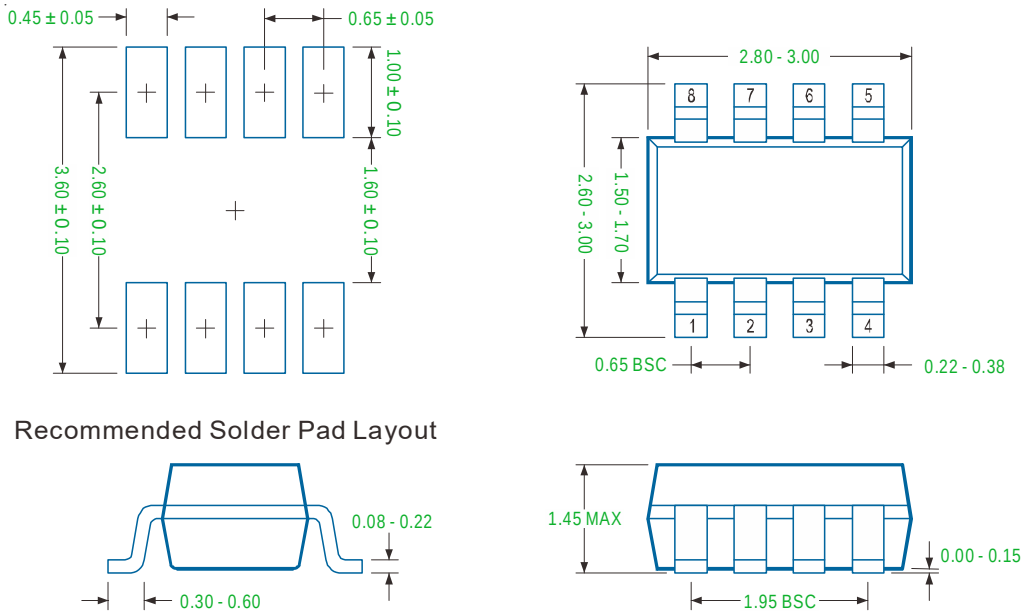
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage Range	V_{CC}		3.3	--	12.6	V
Input Over Voltage Protection	V_{OVP}		--	13	--	V
Quiescent Current	I_{CC}		--	0.4	0.5	mA
DP/DM at Mode 1						
DP Floating Voltage	V_{DP}		2.70	2.75	2.80	V
DM Floating Voltage	V_{DM}	SEL = Low	2.70	2.75	2.80	V
		SEL = High	2.00	2.05	2.10	
DP Pin Output Impedance	Z_{DP}		25	30	35	kΩ
DM Pin Output Impedance	Z_{DM}		25	30	35	kΩ
DP Rising Threshold for Exiting Mode 1	V_{DP-0}	Delta from initial V_{DP}	100	125	150	mV
DM Falling Threshold for Exiting Mode 1	V_{DP-1}		1.0	2.1	2.1	V
DM Falling Threshold for Exiting Mode 1	V_{DM-1}	SEL = Low	1.9	2.0	2.1	V
		SEL = High	1.4	1.5	1.6	V
Debounce Time for Exiting Mode 1		$V_{DP} > V_{DP-0}$	2.0	2.5	3.0	ms
		$V_{DM} < V_{DM-1}$ or $V_{DP} < V_{DP-1}$	9	10	11	ms
DP/DM at Mode 2						
DP and DM Short Circuit Switch			15	20	25	Ω
DP/DM Terminal Voltage			1.1	1.2	1.3	V
DM Pin Output Impedance	Z_{DM}	V_{DM} = 1.2V	70	100	130	kΩ
Recycle Time for Entering Mode 1			2.7	3.0	3.3	s
DP Upper Threshold Level for Entering Mode 3	V_{DP-2}		0.75	0.80	0.85	V
DP Lower Threshold Level for Entering Mode 3	V_{DP-3}		0.35	0.40	0.45	V
Debounce Time for Entering Mode 3			--	1	--	s
DP/DM at Mode 3						
DM Pull Low Resistance			16	20	24	kΩ
DM Pull Low Resistance			320	400	480	kΩ
DP Upper Threshold Level for Entering Mode 4	V_{DP-2}		0.75	0.80	0.85	V
DP Lower Threshold Level for Entering Mode 4	V_{DP-3}		0.35	0.40	0.45	V
Debounce Time for Entering Mode 4			0.18	0.20	0.22	s

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DP/DM at Mode 4						
DP Pull Low Resistance			320	400	480	kΩ
DM Pull Low Resistance			16	20	24	kΩ
DM/DP Forth Threshold Level	V_{DM-4}/V_{DP-4}	V_{DM}, V_{DP} rising	1.95	2.05	2.15	V
DM/DP Forth Level Hysteresis			--	100	--	mV
DM/DP Fifth Threshold Level	V_{DM-5}/V_{DP-5}	V_{DM}, V_{DP} rising	0.325	0.350	0.375	V
DM/DP Fifth Level Hysteresis			--	50	--	mV
Debounce Time for DM Low			1.6	2	2.4	ms
Debounce Time for DP Low			1.6	2	2.4	ms
Current Sink						
IREF Pin Voltage		R_{IREF} = 100kΩ	--	1.00	--	V
Output Current Accuracy (R_{IREF} = 100kΩ)		$V_{DP-5} < V_{DP} < V_{DP-4}$ $V_{DM-5} < V_{DM} < V_{DM-4}$	69.3	70	70.7	uA
		$V_{DP} > V_{DP-4}$; $V_{DM-5} < V_{DM} < V_{DM-4}$	39	40	41	uA
Glitch Time for V_{DP}/V_{DM} Change			36	40	44	ms
Duration for Current Step			40	50	60	us
Output Voltage Discharge						
Discharge Current			--	10	--	mA
Discharge Duration			--	500	--	ms

Package Information

TSOT23-8L

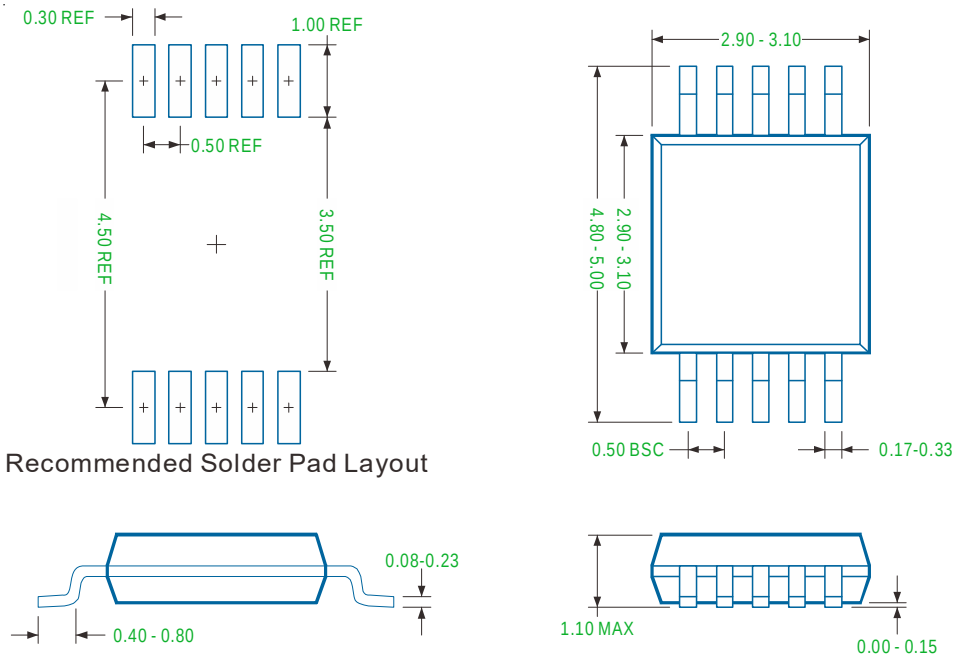


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

MSOP-10L



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