NOVATEK
聯 詠 科 技

Data Sheet

# *For **NT68563XF/NT68563EF***

## Flat Panel Monitor Controller

**Preliminary**
**Draft. 0.95**

2005-01-20

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# 1. Revision History

| NT68563 Specification Revision History | | |
|---|---|---|
| **Version** | **Content** | **Data** |
| 0.95 | To supplement with instruction of XF/EF | Jan.2005 |
| 0.94 | Update Pin name of Pin Assignment | Nov.2004 |
| 0.93 | Remove TCON and RSDS interface | Sep.2004 |
| 0.92 | Added DVI control Spec. | Aug.2004 |
| 0.91 | Added the Schmitt Trigger DC Spec. | Jul.2004 |
| 0.9 | Correction update | Jun.2004 |
| 0.1 | Original | Oct. 2003 |

# 2. FEATURES

**Analog Graphic Input**

- Integrated triple high speed ADC/PLL
- 0.55V to 0.9V Analog input range
- Supports both non-interlaced and interlaced input signals.
- Supports Analog YPbPr input signals clamping, the signals are slightly different from RGB signal in that the dc reference level
- 64 steps of phase adjust for each RGB channel
- Sampling rate up to 110MHz for X type, 165MHz for E type.
- 500 MHz programmable analog bandwidth
- Alternate sampling technology for higher input resolution up to UXGA

**Digital Graphic Input**

- Integrated single link DVI receiver
- Direct connect to all DVI compliant TMDS transmitters
- Operating up to up to 110MHz for X type (XGA), 165MHz for E type (SXGA)

**Digital Video Input**

- Supports ITU-R BT.656 8-bit Input format
- Built-in YUV to RGB color space converter
- Spatial de-interlace

**Display Output**

- Supports single pixel or dual pixel output
- Spread spectrum clock (SSC) output, output signals drive current and slew rate control for low EMI
- Dithering function supports 24-bit quality for 18-bit panel
- Optional Frame Sync or Free Run display synchronization modes
- 10-bit programmable gamma correction
- 2 channel PWM output for LCD back-light control or volume control
- Display resolution up to SXGA
- Supports sRGB input

**Built-in Dual Pixel LVDS Transmitter**

- Integrate the Dual Port, 4 Data Channel and Clock-Out Low-Voltage differential LVDS transmitter to supports single or dual pixel 6/8-bit display data transmission.
- Suited for VGA, SVGA, XGA and dual pixel SXGA, UXGA display transmission from controller to display with very low EMI

**Video Processing**

- Independent horizontal and vertical zoom and shrink
- Auto-calibration function for quick video positioning, clock tracking and phase adjust
- Programmable H-sync pulse guard window prevent the position detecting error
- Enhancement Back-end brightness, contrast, Hue, Saturation and sharpness adjust
- Built-in adaptive Noise Reduction function
- Built-in Post Pattern generator
- Support Bright Frame function

**Sync Processor**

- Support TTL Sync-On-Green (SOG) (including Sync Slicer)
- Polarity detection
- Frequency measurement
- Fast mode change detection
- Interlace or non-interlace input detection
- Separate or composite sync auto switching (including Sync Separator)

**Internal OSD**

- Programmable multi-color RAM font as well as a bitmapped graphical OSD are supported
- Provide 184 programmable 1 bits/pixel RAM Fonts, 64 programmable 2 bits/pixel RAM Fonts, 8 programmable 4 bits/pixel RAM Fonts
- Optional 10x18, 12x18, 10x16, 12x16 dot matrix
- Internal SRAM allows up to 2048 characters, with programmable OSD frame size. Width is 64 column, and Height is 32 row
- Programmable shadow or border control for each character by each row
- Programmable blinking effects for each character
- Spacing control to avoid expansion distortion
- Supports simultaneous display of up to 4 OSD windows
- Maximum 4 times of global zoom for horizontal and vertical axis
- Separate row zoom control
- Support flexible FG or BG optional transparent, translucent, and opaque effects
- 256 palette with 64K color selectable
- Top-bottom flip, left-right mirror and 90 degree / 270 degree rotated
- Flexible Fade-in, Fade-out effect
- Splitting OSD frame supported

**MCU Interface**

- High speed serial 2-wire IIC bus
- High speed parallel 4-Bits bus

**Package**

- QFP 128 pin

## 3. General Description

The NT68563 is a highly integrated flat panel display controller that interfaces analog, digital, and video inputs. It combines a triple ADC, a DVI compliant TMDS receiver, a digital YUV receiver, a high quality zoom and shrink engine, a multi-color on screen display (OSD) controller and many other functions in a single chip. It provides user a simple, flexible and cost-effective solution for various flat panel display products.
The NT68563 operates at frequencies up to 165MHz, suitable for LCD monitor up to SXGA resolution. By using alternate sampling technology, the supported analog input resolution can be extended to UXGA mode.
The NT68563 also build-in noise reduction function to provide more stable video quality, spread spectrum to provide low EMI solution, sRGB for video color space convert, post pattern for manufacture test.

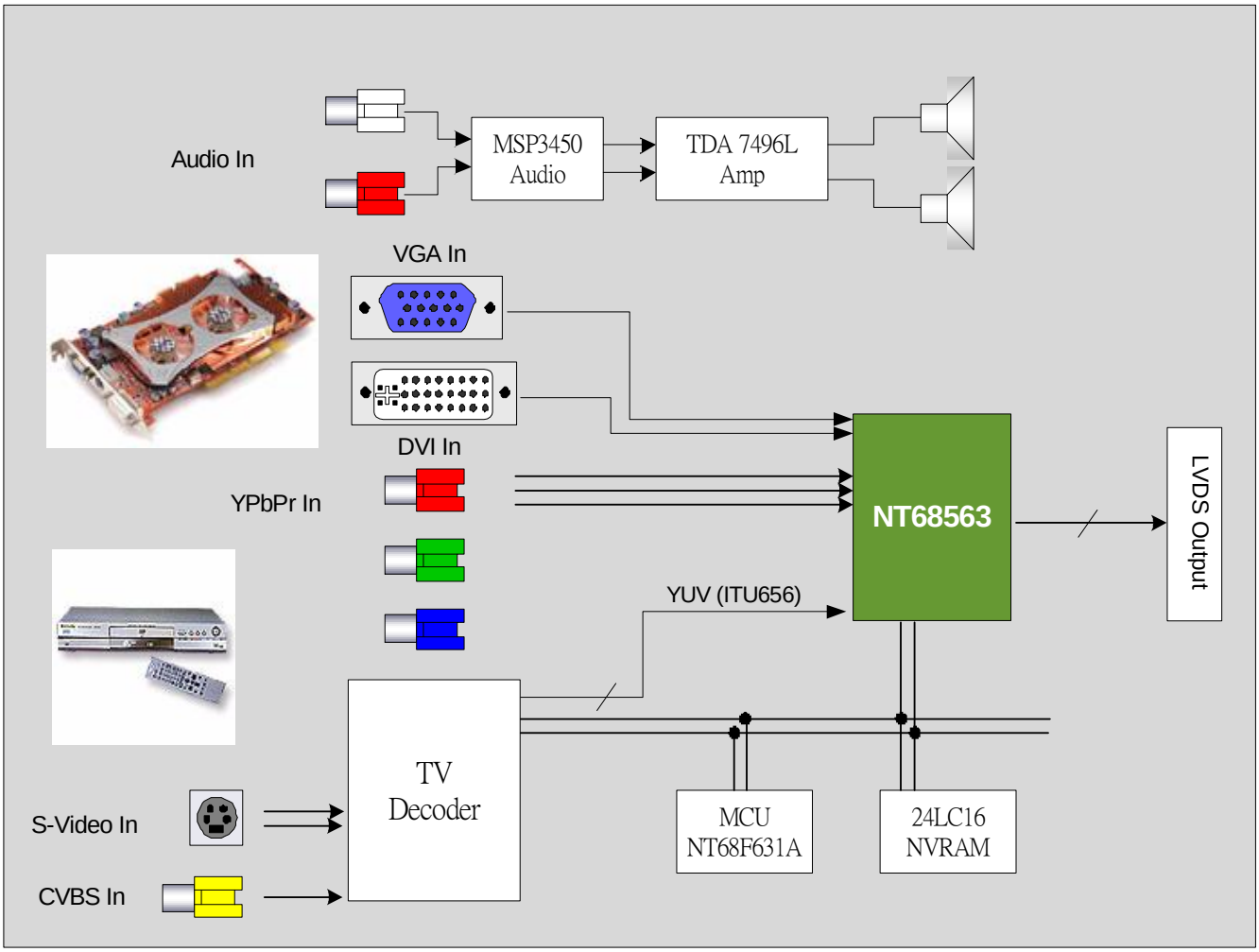



**Figure 3-1 NT68563 System Design Example**

# 4. Block Diagram

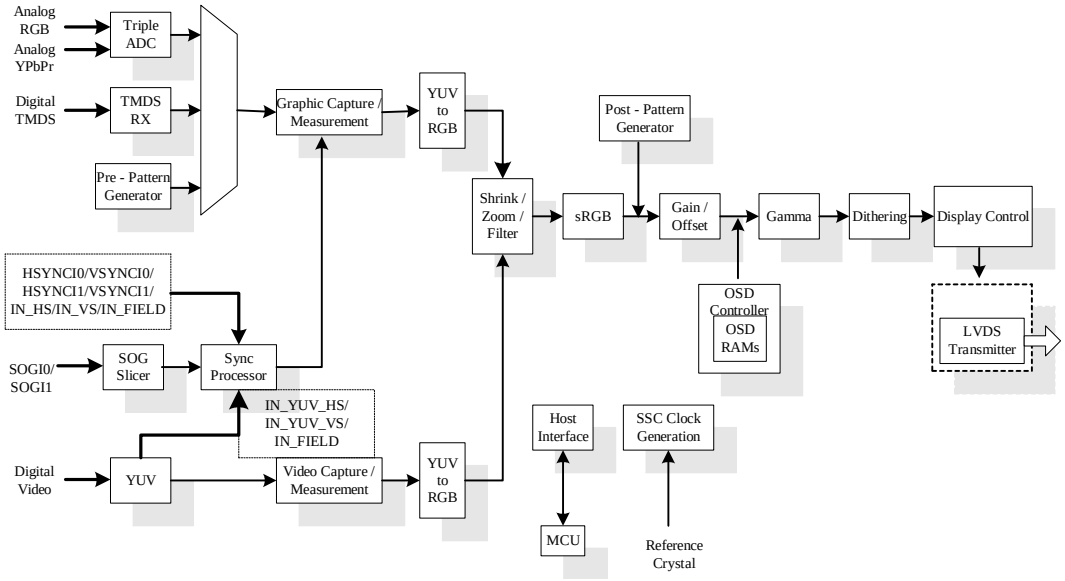



**Figure 4-1 Functional Block Diagram**

# 5. Pinout Information

## 5.1. Pin Diagram

- **Dual Analog, DVI and ITU-R BT656 input with Single/Dual port LVDS output**

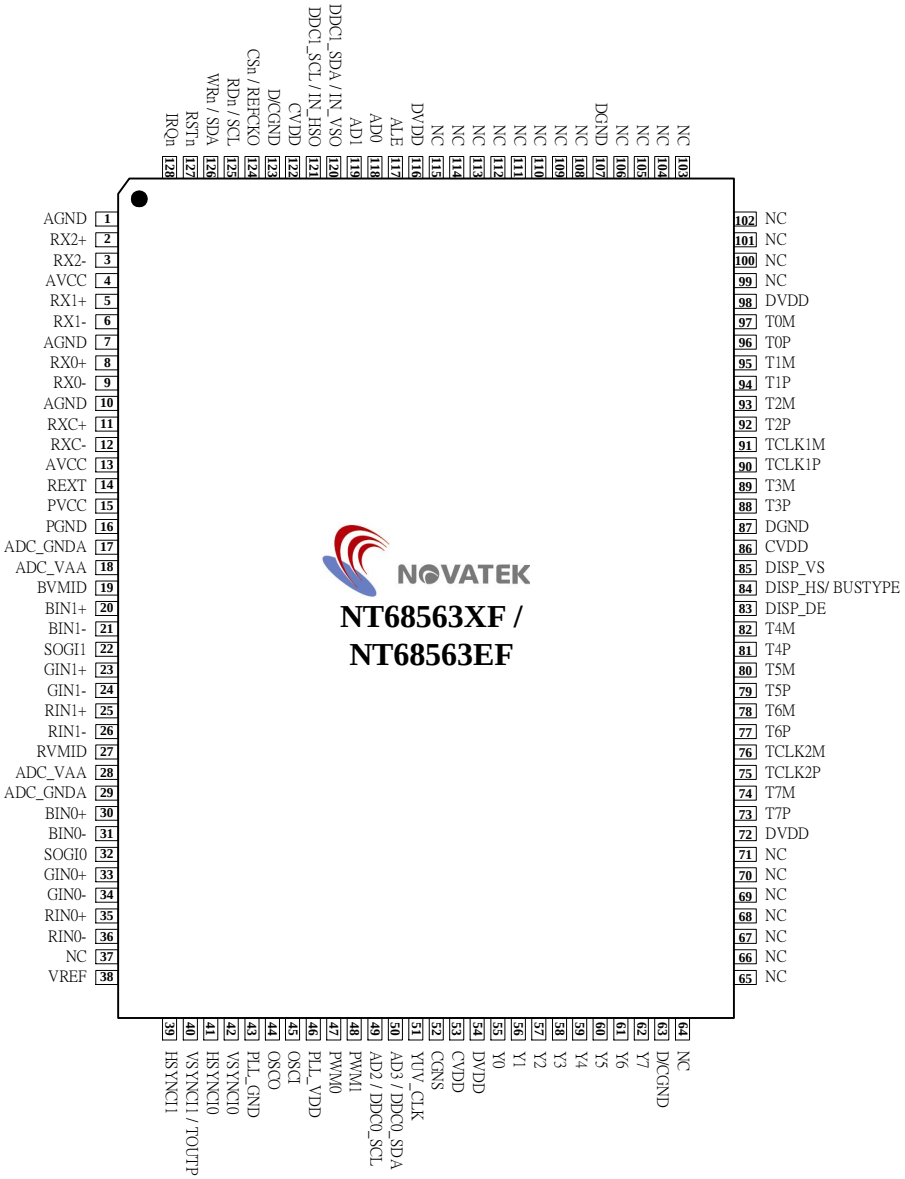



**Figure 5.1-1 NT68563XF, NT68563EF Pin Diagram**

## 5.2. Pin Assignment

| No. | Pin | Type | Definition |
|---|---|---|---|
| 1 | AGND | Power | TMDS Analog GND. |
| 2 | RX2+ | I | TMDS input channel 2+ |
| 3 | RX2- | I | TMDS input channel 2- |
| 4 | AVCC | Power | TMDS Analog VCC must be set to 3.3V. |
| 5 | RX1+ | I | TMDS input channel 1+ |
| 6 | RX1- | I | TMDS input channel 1- |
| 7 | AGND | Power | TMDS Analog GND. |
| 8 | RX0+ | I | TMDS input channel 0+ |
| 9 | RX0- | I | TMDS input channel 0- |
| 10 | AGND | Power | TMDS Analog GND. |
| 11 | RXC+ | I | TMDS input clock pair |
| 12 | RXC- | I | TMDS input clock pair |
| 13 | AVCC | Power | TMDS Analog VCC must be set to 3.3V. |
| 14 | REXT | I | External termination resistor. A 1% 470 Ω resistor must be connected from this pin to AVCC. |
| 15 | PVCC | Power | TMDS PLL Analog VCC must be set to 3.3V. |
| 16 | PGND | Power | TMDS PLL Analog GND. |
| 17 | ADC_GNDA | Power | ADC Analog ground |
| 18 | ADC_VAA | Power | ADC Analog power supply |
| 19 | BMIDSCV | | B Channel Midscale Clamp Voltage Bypass |
| 20 | BIN1+ | I | B channel positive analog video input |
| 21 | BIN1- | I | B channel negative analog video input |
| 22 | SOGI1 | I | VGA Port Sync On Green Input with Schmitt trigger |
| 23 | GIN1+ | I | G channel positive analog video input |
| 24 | GIN1- | I | G channel negative analog video input |
| 25 | RIN1+ | I | R channel positive analog video input |
| 26 | RIN1- | I | R channel negative analog video input |
| 27 | RMID_SCV | | R Channel Midscale Clamp Voltage Bypass |
| 28 | ADC_VAA | Power | ADC analog power supply |
| 29 | ADC_GNDA | Power | ADC analog ground |
| 30 | BIN0+ | I | B channel positive analog video input |
| 31 | BIN0- | I | B channel negative analog video input |
| 32 | SOGI0 | I | VGA Port Sync On Green Input with Schmitt trigger |
| 33 | GIN0+ | I | G channel positive analog video input |
| 34 | GIN0- | I | G channel negative analog video input |

| | | | |
|---|---|---|---|
| 35 | RIN0+ | I | R channel positive analog video input |
| 36 | RIN0- | I | R channel negative analog video input |
| 37 | NC/ADC_GNDA | Power | ADC analog ground |
| 38 | VREF | I | External reference voltage (2.5V) |
| 39 | HSYNCI1 | I | VGA Port Channel1Horizontal Sync Input with Schmitt trigger, when HPLL is enabling. |
| 40 | VSYNCI1 | I | VGA Port Channel 1Vertical Sync Input with Schmitt trigger |
| | TOUTP | O | Testing pin for ADC |
| 41 | HSYNCI0 | I | VGA Port Channel 0 Horizontal Sync Input with Schmitt trigger, when HPLL is enabling. |
| 42 | VSYNCI0 | I | VGA Port Channel 0Vertical Sync Input with Schmitt trigger |
| 43 | PLL_ GND | Power | Core Logic Ground pin for PLL. |
| 44 | OSCO | I/O | Crystal OSC Output |
| 45 | OSCI | I | Crystal OSC Input |
| 46 | PLL_ VDD | Power | Core logic power supply (1.8V) pin for PLL. External capacitor (0.1uF) connected is recommended. |
| 47 | PWM0/GPO10 | I/O | PWM0/ General purpose output |
| 48 | PWM1/GPO9 | I/O | PWM1/ General purpose output |
| 49~50 | GPO [8:7] / AD [2:3] | TTL O | General purpose output for panel driver / Parallel 4-Bits Bus address and data bus |
| 51 | YUV_CLK | I | Video Port Clock |
| 52 | DGND | Power | Digital Ground/ Core Logic Ground |
| 53 | CVDD | Power | Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended. |
| 54 | DVDD | Power | Display Digital Power Supply |
| 55~62 | Y [0:7] | I | Y Video Data [0:7] Input |
| 63 | DGND | Power | Digital Ground/ Core Logic Ground |
| 64~71 | NC | | |
| 72 | DVDD | Power | Display Digital Power Supply |
| 73 | T7P | LVDSO | Positive LVDS differential data output of channel 7 |
| 74 | T7M | LVDSO | Negative LVDS differential data output of channel 7 |
| 75 | TCLK2P | LVDSO | Positive LVDS differential clock 2 output |
| 76 | TCLK2M | LVDSO | Negative LVDS differential clock 2 output |
| 77 | T6P | LVDSO | Positive LVDS differential data output of channel 6 |
| 78 | T6M | LVDSO | Negative LVDS differential data output of channel 6 |
| 79 | T5P | LVDSO | Positive LVDS differential data output of channel 5 |
| 80 | T5M | LVDSO | Negative LVDS differential data output of channel 5 |
| 81 | T4P | LVDSO | Positive LVDS differential data output of channel 4 |
| 82 | T4M | LVDSO | Negative LVDS differential data output of channel 4 |

| | | | |
|---|---|---|---|
| 83 | DISP_DE | O | Display DE |
| 84 | DISP_HS | O | Display Horizontal Sync |
| | GPO0 | O | General purpose output for panel driver |
| 85 | DISP_VS | O | Display Vertical Sync |
| 86 | CVDD | Power | Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended. |
| 87 | DGND | Power | Digital Ground/ Core Logic Ground |
| 88 | T3P | LVDSO | Positive LVDS differential data output of channel 3 |
| 89 | T3M | LVDSO | Negative LVDS differential data output of channel 3 |
| 90 | TCLK1P | LVDSO | Positive LVDS differential clock 1 output |
| 91 | TCLK1M | LVDSO | Negative LVDS differential clock 1 output |
| 92 | T2P | LVDSO | Positive LVDS differential data output of channel 2 |
| 93 | T2M | LVDSO | Negative LVDS differential data output of channel 2 |
| 94 | T1P | LVDSO | Positive LVDS differential data output of channel 1 |
| 95 | T1M | LVDSO | Negative LVDS differential data output of channel 1 |
| 96 | T0P | LVDSO | Positive LVDS differential data output of channel 0 |
| 97 | T0M | LVDSO | Negative LVDS differential data output of channel 0 |
| 98 | DVDD | Power | Display Digital Power Supply |
| 99~106 | NC | | |
| 107 | DGND | Power | Digital Ground |
| 108~115 | NC | | |
| 116 | DVDD | Power | Display Digital Power Supply |
| 117 | GPO1/ ALE | TTL O | General purpose output for panel driver / Parallel 4-Bits Bus Address Latch Enable |
| 118 | GPO2 | TTL O | General purpose output |
| | AD0 | I | Parallel 4-Bits Bus address and data bus / I2C Bus address |
| 119 | GPO3 | TTL O | General purpose output |
| | AD1 | I | Parallel 4-Bits Bus address and data bus / I2C Bus address |
| 120 | IN_VSO/GPO4 | I/O | Internal Vertical Sync output, this signal is by-pass the Sync-processor/ General purpose output |
| 121 | IN_HSO/GPO5 | I/O | Internal Horizontal Sync output, this signal is by-pass the Sync-processor / General purpose output |
| 122 | CVDD | Power | Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended. |
| 123 | DGND | Power | Digital Ground/ Core Logic Ground |
| 124 | REFCKO | O | Reference clock Output |
| | GPO6 / CSn | O | General purpose output / Parallel 4-Bits Bus chip select |
| 125 | SCL / RDn | O | Host Interface Serial Clock. Incorporate Schmitt trigger buffer & spike filter / Parallel 4-Bits Bus read strobe |

| | | | |
|---|---|---|---|
| 126 | SDA / WRn | I/O | Host Interface Serial Data In/Out. Incorporate Schmitt trigger buffer & spike filter / Parallel 4-Bits Bus write strobe |
| 127 | RSTn | I | System Reset |
| 128 | IRQn | O | Interrupt Request |

**Table 5.2-1 Pin List**

## 5.3. Pin Description

**System Interface**

| Pin | Type | Pin No. | Drive | Definition |
|---|---|---|---|---|
| OSCO | I/O | 44 | | Crystal OSC Output |
| OSCI | I | 45 | | Crystal OSC Input |
| IRQn | O | 128 | 4 mA | Interrupt Request |
| RSTn | I | 127 | | System Reset |
| BUSTYPE | I | 84 | | Host interface configuring a '1' will configure chip for serial interface. A '0' will configure chip for parallel interface. |
| REFCKO / CSn | O | 124 | | Reference clock Output / Parallel 4-Bits Bus chip select |
| SDA / WRn | I | 126 | | Host Interface Serial Data In/Out. Incorporate Schmitt trigger buffer & spike filter / Parallel 4-Bits Bus write strobe |
| SCL / RDn | I/O | 125 | | Host Interface Serial Clock. Incorporate Schmitt trigger buffer & spike filter / Parallel 4-Bits Bus read strobe |
| ALE | O | 117 | | Parallel 4-Bits Bus Address Latch Enable |
| AD 0 | I/O | 118 | | Parallel 4-Bits Bus address and data bus / I2C Bus address |
| AD 1 | I/O | 119 | | Four Bit Parallel Bus address and data bus / I2C Bus address |
| AD 2 | I/O | 49 | | Parallel 4-Bits Bus address and data bus |
| AD 3 | I/O | 50 | | Parallel 4-Bits Bus address and data bus |

**Video Interface**

| Pin | Type | Pin No. | Drive | Definition |
|---|---|---|---|---|
| YUV_CLK | I | 51 | | Video Port Clock |
| Y [0:7] | I | 55~62 | | Y Video Data [0:7] Input |

**Graphic Analog Interface**

| Pin | Type | Pin No. | Drive | Definition |
|---|---|---|---|---|
| ADC_GNDA | Power | 17 | | B channel ADC analog ground |
| ADC_VAA | Power | 18 | | B channel ADC analog power supply |
| BMIDSCV | I | 19 | | B Channel Midscale Clamp Voltage Bypass |
| BIN0+ | I | 20 | | B channel positive analog video input |
| BIN0- | I | 21 | | B channel negative analog video input |
| SOGI0 | I | 22 | | VGA Port Sync On Green Input with Schmitt trigger |
| GIN0+ | I | 23 | | G channel positive analog video input |
| GIN0- | I | 24 | | G channel negative analog video input |
| RIN0+ | I | 25 | | R channel positive analog video input |
| RIN0- | I | 26 | | R channel negative analog video input |
| RMIDSCV | I | 27 | | R Channel Midscale Clamp Voltage Bypass |

| | | | | |
|---|---|---|---|---|
| ADC_VAA | Power | 28 | | R channel ADC analog power supply |
| ADC_GNDA | Power | 29 | | R channel ADC analog ground |
| BIN0+ | I | 30 | | B channel positive analog video input |
| BIN0- | I | 31 | | B channel negative analog video input |
| SOGI0 | I | 32 | | VGA Port Sync On Green Input with Schmitt trigger |
| GIN0+ | I | 33 | | G channel positive analog video input |
| GIN0- | I | 34 | | G channel negative analog video input |
| RIN0+ | I | 35 | | R channel positive analog video input |
| RIN0- | I | 36 | | R channel negative analog video input |
| ADC_GNDA | Power | 37 | | R channel ADC analog ground |
| VREF | I | 38 | | External reference voltage (2.5V) |
| HSYNCI1 | I | 39 | | VGA Port Horizontal Sync Input with Schmitt trigger |
| VSYNCI1 | I | 40 | | VGA Port Vertical Sync Input with Schmitt trigger |
| TOUTP | O | 40 | | Testing pin |
| HSYNCI0 | I | 41 | | VGA Port Horizontal Sync Input with Schmitt trigger |
| VSYNCI0 | I | 42 | | VGA Port Vertical Sync Input with Schmitt trigger |

**Graphic TMDS Interface**

| Pin | Type | Pin No. | Drive | Definition |
|---|---|---|---|---|
| RX2+ | I | 2 | | TMDS input channel 2+ |
| RX2- | I | 3 | | TMDS input channel 2- |
| RX1+ | I | 5 | | TMDS input channel 1+ |
| RX1- | I | 6 | | TMDS input channel 1- |
| RX0+ | I | 8 | | TMDS input channel 0+ |
| RX0- | I | 9 | | TMDS input channel 0- |
| RXC+ | I | 11 | | TMDS input clock pair |
| RXC- | I | 12 | | TMDS input clock pair |
| REXT | I | 14 | | External termination resistor. A 1% 470 ohm resistor must be connected from this pin to AVCC. |
| AVCC | Power | 4, 13 | | TMDS Analog VCC must be set to 3.3V. |
| AGND | Power | 1, 7, 10 | | TMDS Analog GND. |
| PVCC | Power | 15 | | TMDS PLL Analog VCC must be set to 3.3V. |
| PGND | Power | 16 | | TMDS PLL Analog GND. |

**Scaler TTL Panel Interface (For test)**

| Pin | Type | Pin No. | Drive | Definition |
|---|---|---|---|---|
| DISP_VS | O | 85 | 2-16 mA | Display Vertical Sync |
| DISP_HS | O | 84 | 2-16 mA | Display Horizontal Sync |
| DISP_DE | O | 83 | 2-16 mA | Display Enable |

**LVDS Panel Interface**

| Pin Name | Pin Type | Pin No. | Pin Count | Pin Function |
|---|---|---|---|---|
| TCLK1P | LVDSO | 90 | 1 | Positive LVDS differential clock 1 output |
| TCLK1M | LVDSO | 91 | 1 | Negative LVDS differential clock 1 output |
| T0P | LVDSO | 96 | 1 | Positive LVDS differential data output of channel 0 |
| T0M | LVDSO | 97 | 1 | Negative LVDS differential data output of channel 0 |

| | | | | |
|---|---|---|---|---|
| T1P | LVDSO | 94 | 1 | Positive LVDS differential data output of channel 1 |
| T1M | LVDSO | 95 | 1 | Negative LVDS differential data output of channel 1 |
| T2P | LVDSO | 92 | 1 | Positive LVDS differential data output of channel 2 |
| T2M | LVDSO | 93 | 1 | Negative LVDS differential data output of channel 2 |
| T3P | LVDSO | 88 | 1 | Positive LVDS differential data output of channel 3 |
| T3M | LVDSO | 89 | 1 | Negative LVDS differential data output of channel 3 |
| | | | | |
| TCLK2P | LVDSO | 75 | 1 | Positive LVDS differential clock 2 output |
| TCLK2M | LVDSO | 76 | 1 | Negative LVDS differential clock 2 output |
| T4P | LVDSO | 81 | 1 | Positive LVDS differential data output of channel 4 |
| T4M | LVDSO | 82 | 1 | Negative LVDS differential data output of channel 4 |
| T5P | LVDSO | 79 | 1 | Positive LVDS differential data output of channel 5 |
| T5M | LVDSO | 80 | 1 | Negative LVDS differential data output of channel 5 |
| T6P | LVDSO | 77 | 1 | Positive LVDS differential data output of channel 6 |
| T6M | LVDSO | 78 | 1 | Negative LVDS differential data output of channel 6 |
| T7P | LVDSO | 73 | 1 | Positive LVDS differential data output of channel 7 |
| T7M | LVDSO | 74 | 1 | Negative LVDS differential data output of channel 7 |

**GPIO Interface**

| Pin | Type | Pin No. | Drive | Definition |
|---|---|---|---|---|
| GPO0 / DISP_HS | O | 84 | | General purpose output / Display Horizontal Sync |
| GPO[1:3] | O | 117-119 | | General-purpose output signal |
| GPO4/ VSO / IN_VSO / DDC1_SDA | I/O | 120 | | General-purpose output signal / Sync-processor Vertical Sync output / Internal Vertical Sync output, this signal is by-pass the Sync-processor / Serial Data I/O for the DDC Port1 |
| GPO5/ HSO/ IN_HSO / DDC1_SCL | I/O | 121 | | General-purpose output signal / Sync-processor Horizontal Sync output / Internal Horizontal Sync output, this signal is by-pass the Sync-processor / Serial Clock I/O for the DDC Port1 |
| GPO6 | O | 124 | | General-purpose output signal |
| GPO7/DDC0_SDA | I/O | 50 | | General-purpose output signal.<br>Serial Data I/O for the DDC Port0 |
| GPO8/DDC0_SCL | I/O | 49 | | General-purpose output signal.<br>Serial Clock I/O for the DDC Port0 |
| GPO9/PWM1 | I/O | 48 | | PWM1/General purpose input/output signal |
| GPO10/PWM0 | I/O | 47 | | PWM0/General purpose input/output signal |

**Power Pin**

| Pin | Type | Pin No. | Drive | Definition |
|---|---|---|---|---|
| CVDD | Power | 53, 86, 122 | | Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended. |
| CGND | Power | 52, 63,123 | | Core Logic Ground |
| DVDD | Power | 54, 72, 98, 116 | | Display Digital Power Supply |

| | | | | |
|---|---|---|---|---|
| DGND | Power | 63, 87, 107, 123 | | Digital Ground |
| PLL_VDD | Power | 46 | | Core logic power supply (1.8V) pin for PLL. External capacitor (0.1uF) connected is recommended. |
| PLL_GND | Power | 43 | | Core Logic Ground pin for PLL. |
| AVCC | Power | 4, 13 | | TMDS Analog VCC must be set to 3.3V. |
| AGND | Power | 1, 7, 10 | | TMDS Analog GND. |
| PVCC | Power | 15 | | TMDS PLL Analog VCC must be set to 3.3V. |
| PGND | Power | 16 | | TMDS PLL Analog GND. |
| ADC_VAA | Power | 18, 28 | | ADC analog power supply |
| ADC_GNDA | Power | 17, 29, 37 | | ADC analog ground |
| | | | | |
| | | | | |

# 6. Functional Description

## 6.1. Power Control

NT68563 supports the whole chip power down function. By setting the CHIP_PWDN bit to '1', NT68563 will go into power down state except the **I2C** logic and **Sync-processor (include SOG Slicer, and TMDS Sync Detect)** will keep alive.

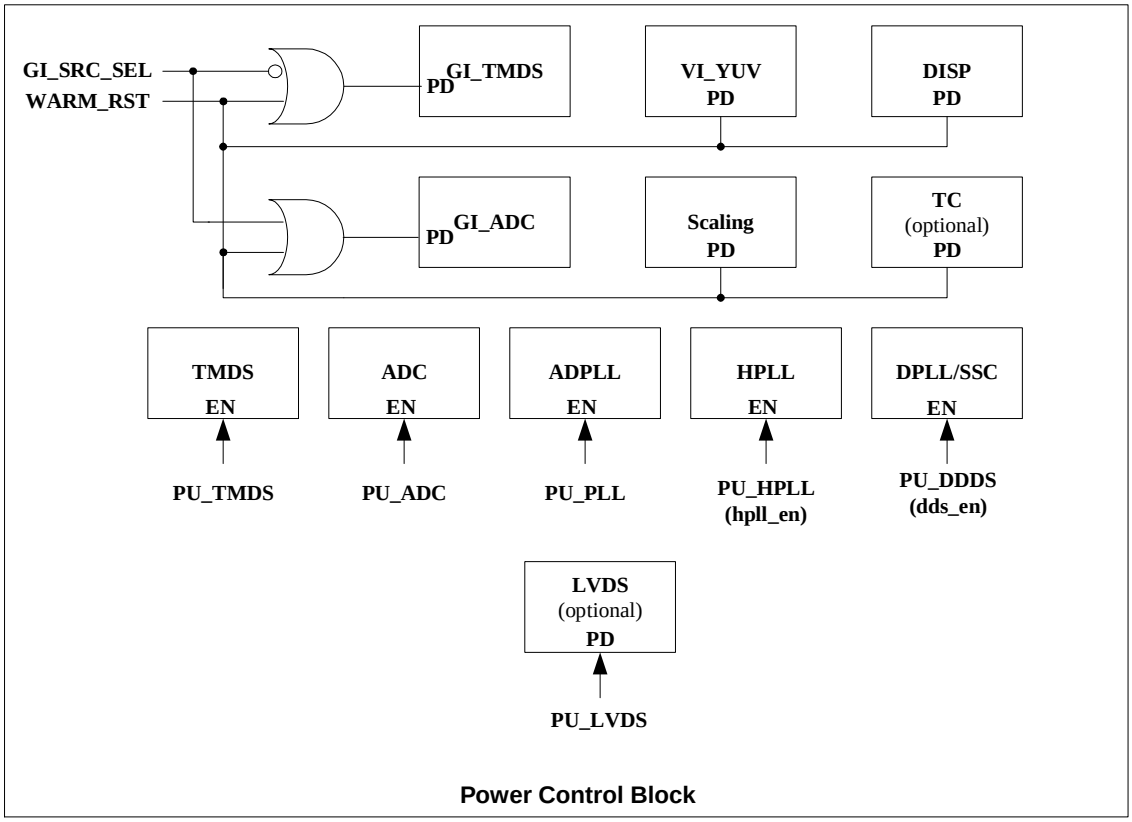



**Figure 6.1-1 Power Control Block**

## 6.2. Analog to Digital Converter (ADC)

NT68563 provides a clock-recovery circuit and an analog-to-digital converter to effectively save the cost of needing external expensive ADC and PLL. The gain and offset circuit is used to adjust the gain (Contrast) of input video amplitude and shift the DC offset voltage (Brightness). The clock-recovery circuit consisting of a high-speed phase lock loop (PLL) is used to generate the clock to sample analog RGB/YPbPr data. This circuit is locked to the HSYNC of the incoming video signal. The analog-to-digital converter (ADC) transfers the input analog RGB/YPbPr video to digital output data with each color 8-bit resolution.

**Gain and Offset Control**

RIN/GIN/BIN are high-impedance input pins that accept the RED, GREEN, and BLUE channel graphics signals. They accommodate input signals ranging from 0.55V to 0.9V full scale. Signals should be AC-couple to these pins.

Due to AC coupling, clamping pulse is needed to define the time during which the input signal is clamped to ground, establishing a black reference. Typically the clamping pulse is defined during the

back porch period of the graphics signal. NT68563 generates the clamping pulse internally and the position and duration are programmable. The simpler clamp-timing generator clamping pulse-starting position and pulse width is defined in 0x021[7:0] and 0x022[7:0].

NT68563 has three independent variable gain amplifiers for each channel with input signal range from 0.55V to 0.9V（p-p）, the full-scale range is set in three 9-bit registers.
NT68563's offset control shifts the entire input range, resulting in a change in image brightness. The three independent variable 8-bit registers provide independent settings for each channel.

**Clamp Pulse generator**
This block circuit called **Clamp pulse generator** generates clamp pulse to ADC. There are two input trigger sources of the clamp generator, one is signal **Hin** from separator and another is Row **Hs** from the HSYNCI0 / HSYNCI1. The polarity and the trigger edge of the **clamp** can be selected by using bit CLMP_POL and bit CLMP_EDG respectively. The trigger delay of the **clamp** is waiting **CLMP_BEG [5:0]** x REFCLK time. The pulse width of the **clamp** output may be selected by **CLMP_WID [5:0]**.

➢ ***Clamp Pulse Timing***

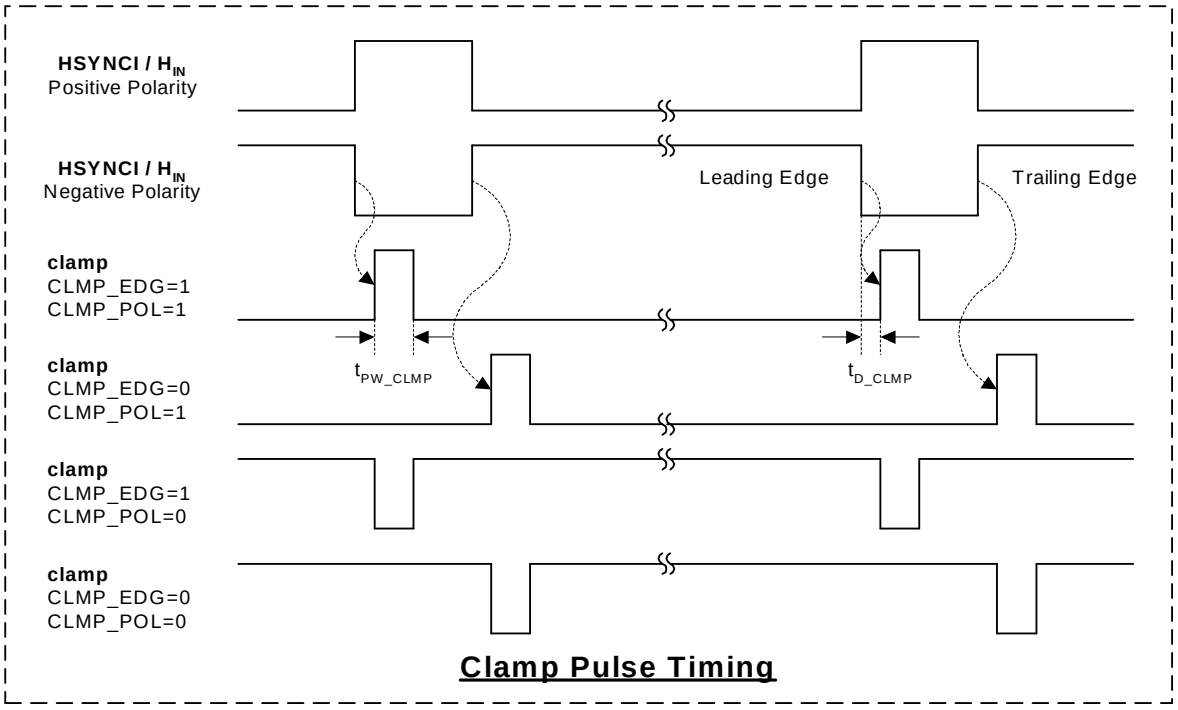



**Figure 6.2-1 Clamp Pulse Timing**

**COAST**
This function is used to cause the pixel clock generator to stop synchronizing with Hsync and continues producing a clock at its current frequency and phase. This is useful when processing composite sync that fails to produce horizontal sync pulses when in the vertical interval.

## 6.3. DVI Receiver

The DVI receiver uses Panel Link Digital technology to support input ranging from VGA to SXGA (25-110 MHz) for X type and VGA to UXGA (25-165 MHz) for E type, which is ideal for desktop and specialty applications.

## 6.4. Graphic Port Capture Interface

The function of Graphic Port Capture Interface is to provide two interfaces between NT68563 and external input devices. It can process non-interlaced and interlaced RGB graphic input, and DVI input. User should select the video input source from Graphic Port (VGA or DVI) and the polarity of external control signal, and then program the H/V captures size registers to indicate the display area.

## 6.5. Video Port Capture Interface

The function of Video Port Capture Interface is to provide Digital YUV interface between NT68563 and video decoder. It can process non-interlaced and interlaced digital YUV video ITU BT656 input. It includes color space conversion for YUV to RGB color space conversion.

## 6.6. Auto Tune

The Auto Tune function consists of Auto Gain, Auto Position, and Auto Phase. With such auto adjustment support it is possible to measure the correct phase, frequency, gain, and offset of ADC. The horizontal and vertical back porches of input image and the horizontal and vertical active regions can also be measured.

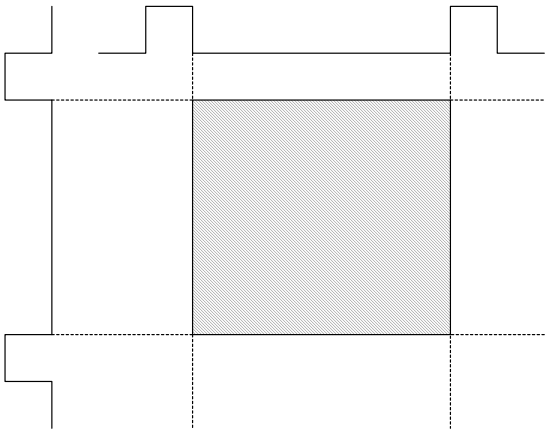


**Figure 6.6-1 DISP_AUTO = 0**

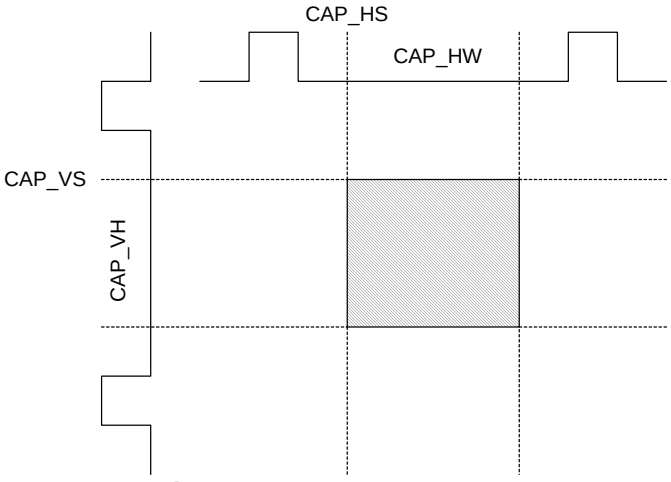



**Figure 6.6-2 DISP_AUTO**

**Auto Gain**

Gain value is the Minimum or Maximum pixel value within the specified input image region for each RGB channel. This function is useful for measuring the noise margin of input video or for auto-contrast calibrating by adjusting ADC' s offset and gain.

**Programming Steps:**

Reference application notice

**Auto Position**

NT68563 provides Horizontal/Vertical back porch and active region information. Users can use these values to set input capture registers to aid in centering the screen automatically, and adjust the ADCPLL's divider value to figure out the correct input pixel frequency.

**Programming Steps:**

Reference application notice

**Auto Clock**

**Programming Steps:**

Reference application notice

**Auto Phase**

**Programming Steps:**

Reference application notice

## 6.7. Video Processor

Video processor consists of Interpolation Control, RGB Gain Control, RGB Offset Control, Hue and Saturation Control, Dithering Control, Gamma Correction Control and sRGB Support.
NT68563's enhanced interpolation method makes the zoomed display image look more smooth and comfortable.
User can adjust the RGB Gain (Contrast) and RGB Offset (Brightness) by the registers in the ADCPLL block, or registers in the Video processor block. But for YUV video input, it is suitable to adjust Contrast and Brightness at here. In addition, it supports all YUV color controls including brightness, contrast, hue and saturation.
Dithering function can provide 16.7 million colors space for 6-bit/color panel. It is recommended to open the dithering function while a 6-bit panel is used.
68563 provide independently horizontal and vertical zoom scaler with adjustable zoom factor from 1/4x to 4x. Each of the zoom scaler uses variable sharpness filter to provide high quality scaling of real-time video and still graphic images.

**Interpolation**

1. Flexible Sharpness Filter

68563 include flexible sharpness filter for horizontal and vertical sharpness adjusting. Users can use them by register programming.

2. Vertical Spatial Interpolation

When interlaced video or images are applied, the 68563 vertical scaling engines will de-interlace the input fields spatially and reposition them to align the display's line map.

3. Advanced Filter

With the aid of two selectable advanced filters when zooming up horizontally, 68563 provides the most undistorted image from the original one.

**sRGB Support**

sRGB is a standard for color exchange proposed by Microsoft and HP. The sRGB controls can be used to make LCD monitors sRGB compliant.

$$\begin{bmatrix} R'_{sRGB} \\ G'_{sRGB} \\ B'_{sRGB} \end{bmatrix} = \begin{bmatrix} A0 & B0 & C0 \\ A1 & B1 & C1 \\ A2 & B2 & C2 \end{bmatrix} \begin{bmatrix} R_{sRGB} \\ G_{sRGB} \\ B_{sRGB} \end{bmatrix} + \begin{bmatrix} Offset_R \\ Offset_G \\ Offset_B \end{bmatrix} \text{ ----------[1]}$$

**Gamma Correction**

- Provides 10-bit gamma correction function
- Hardware piecewise simulation method
- F/W needs to define total 256 end-point value in advance

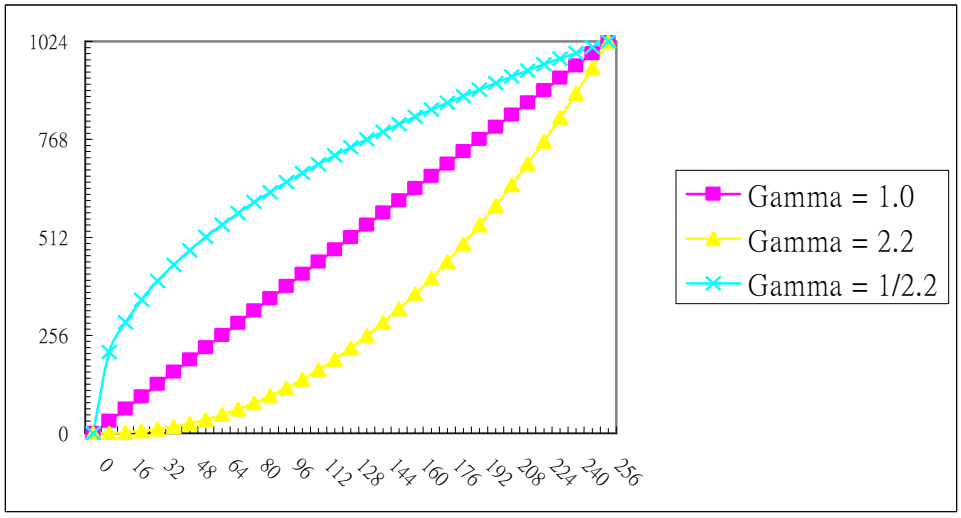



**Figure 6.7-1 Gamma Correction Curve**

| Index Address | **Gamma Table** | Value |
|---|---|---|
| 0 | | LSB0 (2 bits)+MSB0 (8 bits) |
| 1 | | LSB1+MSB1 |
| 2 | | LSB2+MSB2 |
| …. | …. | |
| 254 | | LSB254+MSB254 |
| 255 | | LSB255+MSB255 |

## 6.8. Alternate Frame Sampling (AFS)

Since the limit of ADCPLL's bandwidth, NT68563 can't directly support the VGA modes for those larger than SXGA@75Hz, like as SXGA@85Hz and UXGA@60Hz. But by using the Alternate Frame Sampling technology, NT68563 can accept these input modes with the trade-off of losing some display quality. When AFS is enabled, ADC will sample all even pixels for even frame and odd pixels for odd frame, that cause the ADC's sampling frequency is degraded to half of the source frequency. Then by using Spatial De-alternating Function, we can display all original input images with just little data loss.

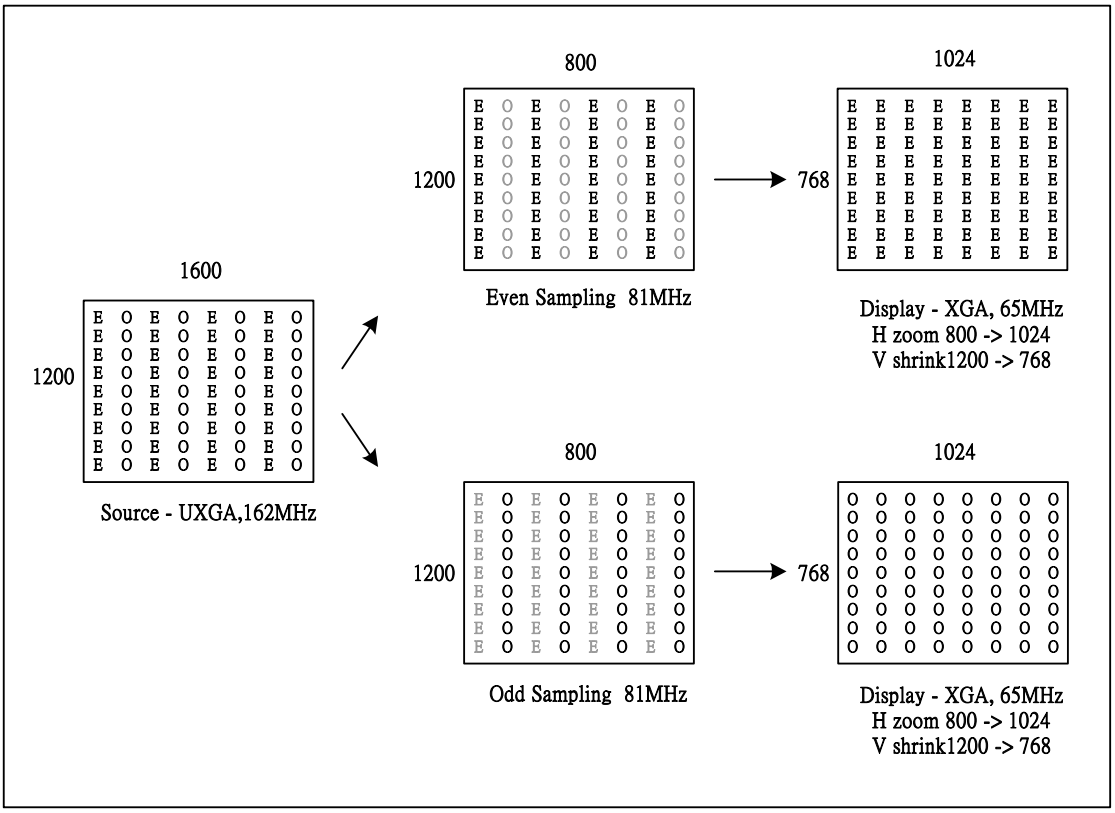



**Figure 6.8-1 Alternate Frame Sampling---Spatial de-alternating**

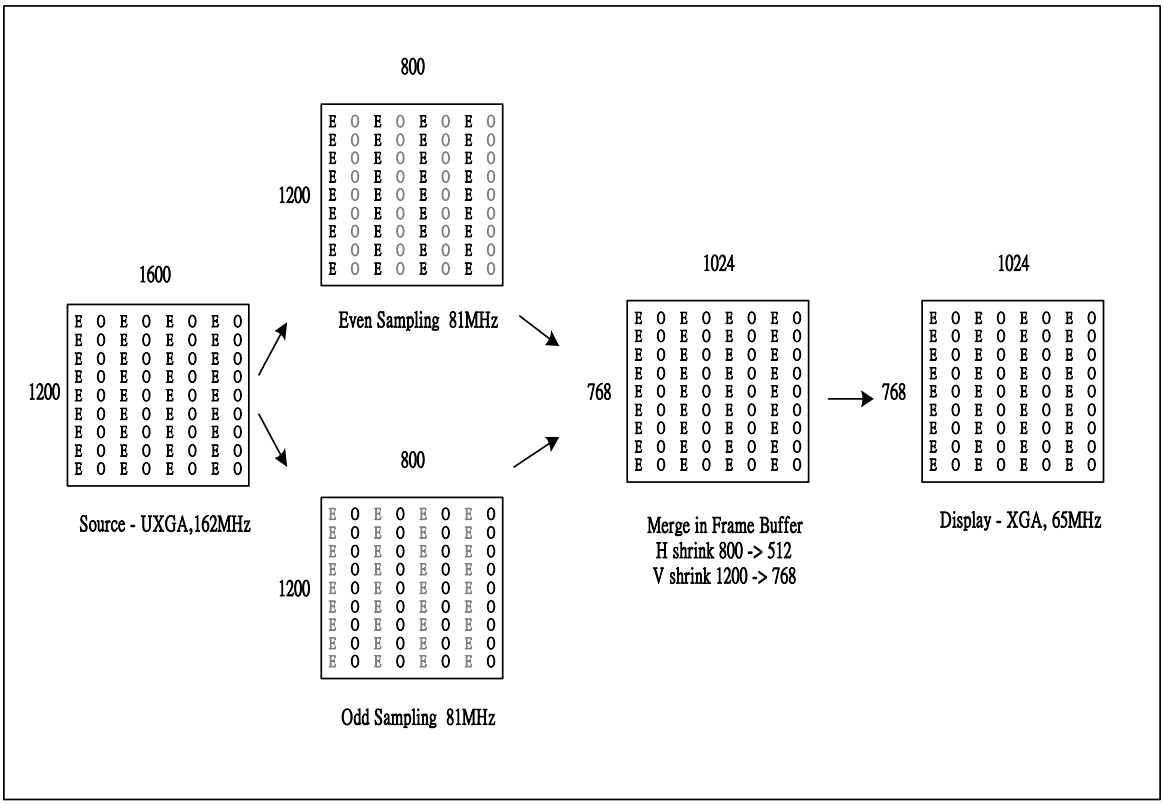



**Figure 6.8-2 Alternate Frame Sampling ---Two Frame Merge**

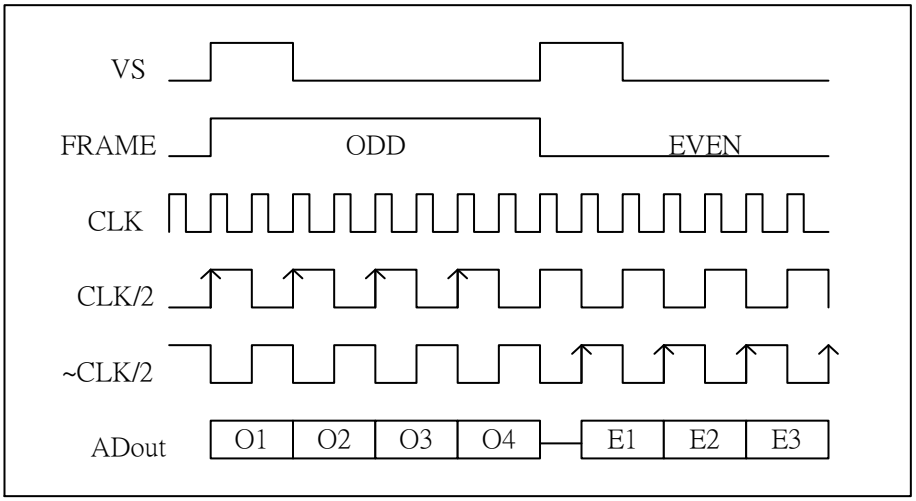



**Figure 6.8-3 De-alternating Timing**

## 6.9. Sync Processor

The NT68563 has a Sync Processor block providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input timing. It is also capable of detecting the field type of interlaced formats.

**Hsync /Vsync Frequency and Polarity Detection**
**GI_HCNT**, the 13 bits Hsync period counter counts the time of 32xHSYNC period, then loads the result into the GI_HCNT latch. The output value will be [((REFCLK / 4 x 32)/HFreq)], updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present.
**GI_VCNT**, the 13 bits Vsync period counter counts the time between two VSYNC pulses, then loads the result into the GI_VCNT latch. The output value will be [(REFCLK/(256 x Vfreq))], updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow.
The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The INT_HPOL interrupt is set when the GI_HPOL value changes. The INT_VPOL interrupt is set when the GI_VPOL value changes.

**H/V Present Check**
The Hsync present function checks the input HSYNCI pulse, GI_HPRE flag is set when HSYNCI is over HSYNC Present High Counter Threshold (HPRE_THR_HI) or cleared when HSYNC is under HSYNC Present Low Counter Threshold (HPRE_THR_LO). The Vsync present function checks the input VSYNCI pulse, the GI_VPRE flag is set when VSYNCI is over VSYNC Present High Counter Threshold (VPRE_THR_HI) or cleared when VSYNC is under VSYNC Present Low Counter Threshold (VPRE_THR_LO). The INT_HPRE interrupt is set when the GI_HPRE value changes. The INT_VPRE interrupt is set when the GI_VPRE /GI_CSPRE value change.

**Timing Change Detection**
The INT_VFREQ/INT_HFREQ interrupt is set when GI_VCNT / GI_HCNT value changes or overflows.

## Extract Vsync from Composite/SOG Signal

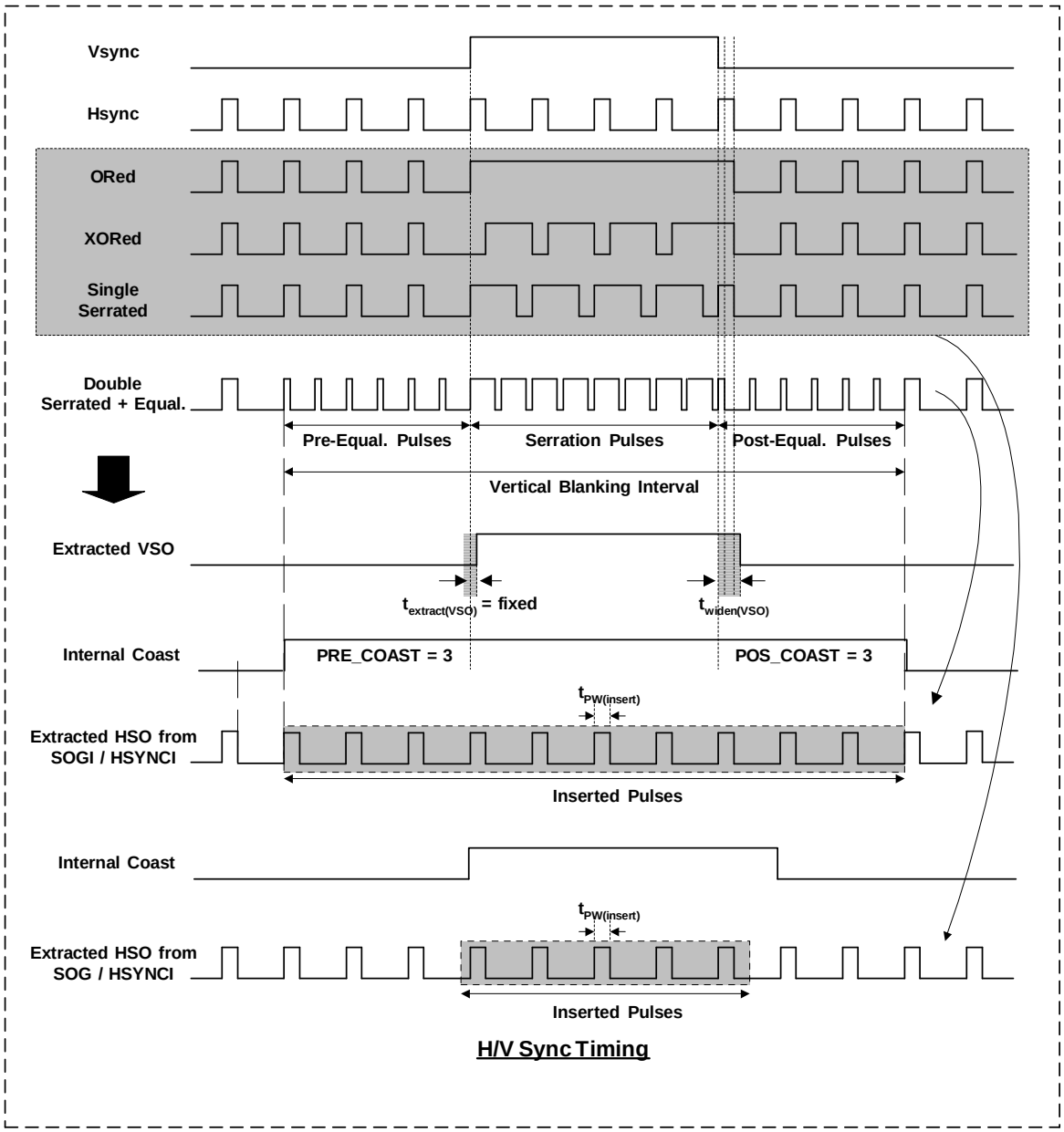



**Figure 6.9-1 H/V Timing**

### Internal Odd/Even Field Detection

Included in the sync detector is circuitry to determine which field is currently being input for interlaced input. To determine the field based on position of VSYNC relative to HSYNC, the GI_FLD_WINBEG (3:0) and GI_FLD_WINEND (3:0) registers are used for Graphic Port and the VI_FLD_WINBEG (3:0) and VI_FLD_WINEND (3:0) registers are used for Video Port. The NT68563 divides each horizontal line into 16 equal intervals. The FLD_WINBEG bits are used to specify at which 1/16$^{th}$ of a line to start looking for the leading edge of VSYNC. The FLD_WINEND bits are used to specify at which 1/16$^{th}$ of a line to stop looking. If the leading edge of VSYNC occurs between during or after the 1/16$^{th}$ line specified by FLD_WINBEG, but no later than the 1/16$^{th}$ line specified by FLD_WINEND, the current field is marked as odd. Otherwise, a leading edge transition outside these boundaries will cause the current field to be marked even.

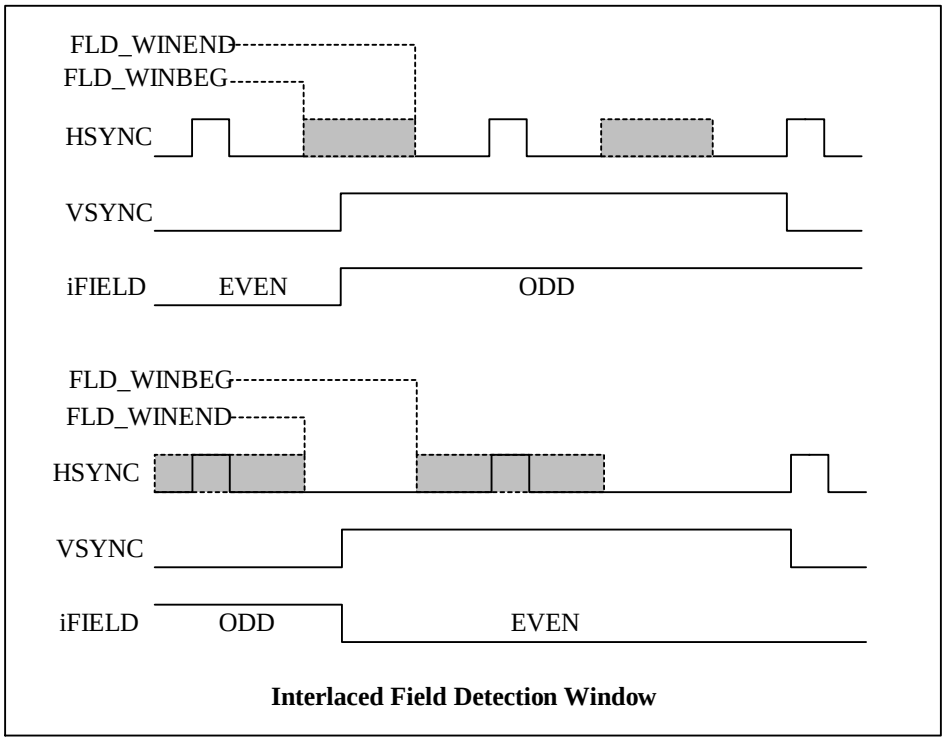



**Figure 6.9-2 Interlaced Field Detection Window**

**Free Run Timing Generator**

This Block can generate various free-running outputs to satisfy various application requirements. The pulse width of the $H_{FREE}$ output is fixed **15 x REFCLK** and the $V_{FREE}$ is **3 HFREEs**. User can properly set the content of HSO Free Run divider, HFREE_DIV, to get the need frequency of the HSO, and set the content VSO Free Run divider, VFREE_DIV, to get the frequency of the VSO. Details refer to the descriptions of the free-run registers HFREE_DIV and VFREE_DIV. Refer to the descriptions of the register for details to get user's need frequencies.

Users can disable H/V free run output by clearing GI_HRUN_EN /GI_VRUN_EN.

**Sync On Green Slicer**

This function is provided to assist with processing signals with embedded sync, typically on the GIN channel. The circuit sliced the signals that with embedded sync, and apply to Sync Separator for extracting Hsync and Vsync.

## 6.10. OSD Function

**NT68563 supports internal OSD with following features:**

- Programmable Multi-color RAM font OSD
- Totally 184 programmable 1 bits/pixel RAM Fonts, 64 programmable 2 bits/pixel RAM Fonts, and 8 programmable 4 bits/pixel RAM Fonts
- Character attributes for 1, 2, 4 bits/pixel
- Optional 10x18, 12x18 Font Matrix Selection
- Internal SRAM allows up to 2048 characters
- Fully Programmable Character Array of 32 Rows by 64 Columns
- 256 palette up to 64K resolution for each R/G/B colors
- Up to 256-Color Selection from a 64K color palette with Color Intensity Attribute on Each Character
- True 256-Color Selection from a 64K color palette for Windows
- Shadowing on Windows with Programmable Shadow Width/Height/Color
- Row To Row and Column To Column Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Programmable Bordering or Shadowing for each character by each row
- Programmable blinking effects for each character
- Background Translucent, transparent, and opaque effects
- Programmable Vertical and Horizontal Positioning for Display
- Each OSD row can be independently zoomed up to 4 times for horizontal and vertical axis
- Top-bottom flip, left-right mirror and 90 degree / 270 degree rotated
- Maximum Pixel CLK of UXGA resolution
- Fade In / Fade Out effect

**OSD Font's Attribute and Code Format, Palette Format Definition:**

OSD Palette Format

| 15:11 | 10:5 | 4:0 |
|---|---|---|
| R | G | B |

OSD Code Format

| 7:0 |
|---|
| Font Index |

OSD Attribute Format

| 15:8 | 7:4 | 3:2 | 1 | 0 |
|---|---|---|---|---|
| PA_Index [7:0] | BG_Index [3:0] | CA_Bit | Mix | Blink |

**Figure 6.10-1**

- Blink : 0 - No blinking
  1 - Blinking (All color is blinking except background color)
- Mix : 0 - Normal
  1 - Translucent ((1- TP_LEVEL) Display + (TP_LEVEL) OSD_BG)
- CA_Bit [1:0] : Character attribute bits/pixel number
  00: one bit/pixel color Font (0-255 font index)
  01: one bit/pixel color Font (256-511 font index)
  10: two-bits/pixel color Font
  11: four bits/pixel color Font
- PA_Index [7:0] / BG_Index [3:0]: Attribute color palette index

**Case A: Pixel is outside an active window**
**One Bit per pixel.**
Foreground '1' Pixel [7:0] <= PA_Index [7:0] + 1
Background '0' Pixel [7:0] <= 0x00 + BG_Index [3:0]

**Two Bit per pixel.**
Foreground '11' Pixel [7:0] <= PA_Index [7:0] + '11'
Foreground '10' Pixel [7:0] <= PA_Index [7:0] + '10'
Foreground '01' Pixel [7:0] <= PA_Index [7:0] + '01'
Background '00' Pixel [7:0] <= 0x00 + BG_Index [3:0]

**Four Bit per pixel.**
Foreground '1111' Pixel [7:0] <= PA_Index [7:0] + '1111'
Foreground '1110' Pixel [7:0] <= PA_Index [7:0] + '1110'
Foreground '1101' Pixel [7:0] <= PA_Index [7:0] + '1101'
Foreground '1100' Pixel [7:0] <= PA_Index [7:0] + '1100'
Foreground '1011' Pixel [7:0] <= PA_Index [7:0] + '1011'
Foreground '1010' Pixel [7:0] <= PA_Index [7:0] + '1010'
Foreground '1001' Pixel [7:0] <= PA_Index [7:0] + '1001'
Foreground '1000' Pixel [7:0] <= PA_Index [7:0] + '1000'
Foreground '0111' Pixel [7:0] <= PA_Index [7:0] + '0111'
Foreground '0110' Pixel [7:0] <= PA_Index [7:0] + '0110'
Foreground '0101' Pixel [7:0] <= PA_Index [7:0] + '0101'

Foreground ‘0100’ Pixel [7:0] <= PA_Index [7:0] + ‘0100’
Foreground ‘0011’ Pixel [7:0] <= PA_Index [7:0] + ‘0011’
Foreground ‘0010’ Pixel [7:0] <= PA_Index [7:0] + ‘0010’
Foreground ‘0001’ Pixel [7:0] <= PA_Index [7:0] + ‘0001’

**Note: If BG_Index [3:0] = ”0000”, indicates that this background color is transparent**
**If BG_Index [3:0] = “0001”, Background ‘0000’ Pixel [7:0] <= PA_Index [7:0]**

**Case B: Pixel is inside an active window**

**One Bit per pixel.**
Foreground ‘1’ Pixel [7:0] <= PA_Index [7:0] + ‘1’
Background ‘0’ Pixel [7:0] <= WINx_ATTR [7:0]

**Two Bit per pixel.**
Foreground ‘11’ Pixel [7:0] <= PA_Index [7:0] + ‘11’
Foreground ‘10’ Pixel [7:0] <= PA_Index [7:0] + ‘10’
Foreground ‘01’ Pixel [7:0] <= PA_Index [7:0] + ‘01’
Background ‘00’ Pixel [7:0] <= WINx_ATTR [7:0]

**Four Bit per pixel.**
Foreground ‘1111’ Pixel [7:0] <= PA_Index [7:0] + ‘1111’
Foreground ‘1110’ Pixel [7:0] <= PA_Index [7:0] + ‘1110’
Foreground ‘1101’ Pixel [7:0] <= PA_Index [7:0] + ‘1101’
Foreground ‘1100’ Pixel [7:0] <= PA_Index [7:0] + ‘1100’
Foreground ‘1011’ Pixel [7:0] <= PA_Index [7:0] + ‘1011’
Foreground ‘1010’ Pixel [7:0] <= PA_Index [7:0] + ‘1010’
Foreground ‘1001’ Pixel [7:0] <= PA_Index [7:0] + ‘1001’
Foreground ‘1000’ Pixel [7:0] <= PA_Index [7:0] + ‘1000’
Foreground ‘0111’ Pixel [7:0] <= PA_Index [7:0] + ‘0111’
Foreground ‘0110’ Pixel [7:0] <= PA_Index [7:0] + ‘0110’
Foreground ‘0101’ Pixel [7:0] <= PA_Index [7:0] + ‘0101’
Foreground ‘0100’ Pixel [7:0] <= PA_Index [7:0] + ‘0100’
Foreground ‘0011’ Pixel [7:0] <= PA_Index [7:0] + ‘0011’
Foreground ‘0010’ Pixel [7:0] <= PA_Index [7:0] + ‘0010’
Foreground ‘0001’ Pixel [7:0] <= PA_Index [7:0] + ‘0001’
Background ‘0000’ Pixel [7:0] <= WINx_ATTR [7:0]

**Palette Address and map**

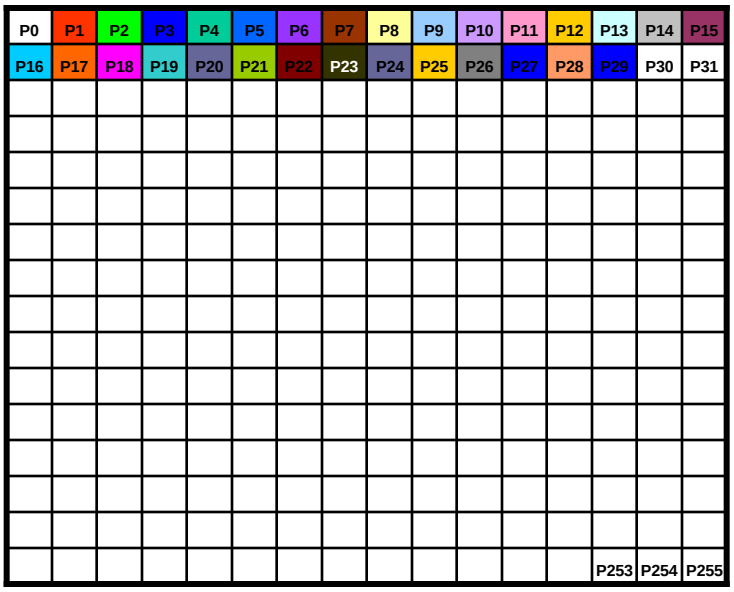



**Figure 6.10-2 Palette**

| Palette N | Palette Address | Bits [15:11] | Bits [10:5] | Bits [4:0] |
|---|---|---|---|---|
| Palette 0 | 0 (0x00H) | R0 [4:0] | G0 [5:0] | B0 [4:0] |
| Palette 1 | 1 (0x01H) | R1 [4:0] | G1 [5:0] | B1 [4:0] |
| Palette 2 | 2 (0x02H) | R2 [4:0] | G2 [5:0] | B2 [4:0] |
| … | … | | | |
| Palette 15 | 15 (0x0FH) | R15 [4:0] | G15 [5:0] | B15 [4:0] |
| Palette 16 | 16 (0x04H) | R16 [4:0] | G16 [5:0] | B16 [4:0] |
| Palette 17 | 17 (0x05H) | R17 [4:0] | G17 [5:0] | B17 [4:0] |
| … | … | | | |
| Palette 254 | 254 (0xFEH) | R254 [4:0] | G254 [5:0] | B254 [4:0] |
| Palette 255 | 255 (0xFFH) | R255 [4:0] | G255 [5:0] | B255 [4:0] |

**Figure 6.10-3 Palette address and map**

## OSD Character Map

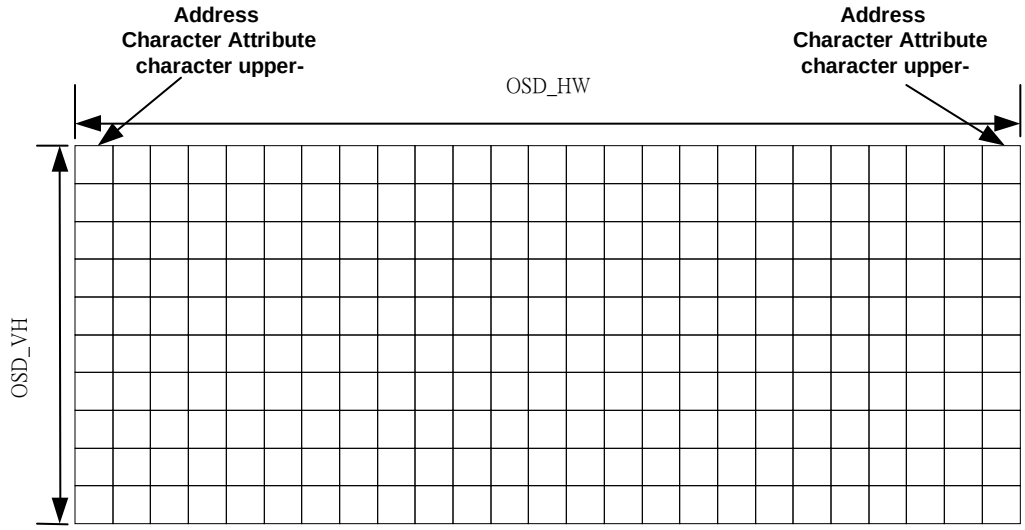



**Figure 6.10-4 OSD Character Map**

## OSD Font Definitions
### One Bit per pixel

One bit per pixel font definitions are arranged in Color Character Font SRAM Memory on a 12-bit by 18-address grid. The One bit per pixel OSD programmable font start address is specified in Register 0x089 ~ 0x088. Odd font definitions are stored in SRAM bits [11:0], and even font definitions are stored in SRAM bits [23:12].

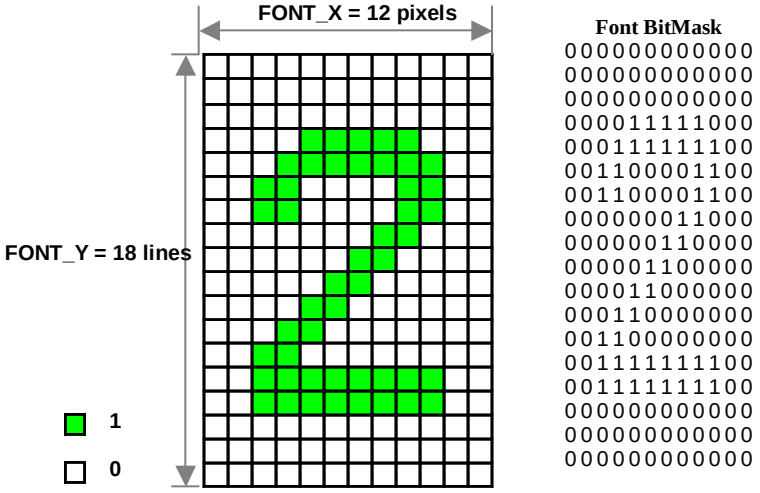



**Figure 6.10-5 One Bit Per Pixel Font**

### Two Bit per pixel

Two bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 18 addresses. The two bit per pixel OSD programmable font start address is specified in Register 0x08B ~ 0x08A. Font definitions are stored in SRAM bits [23:0].

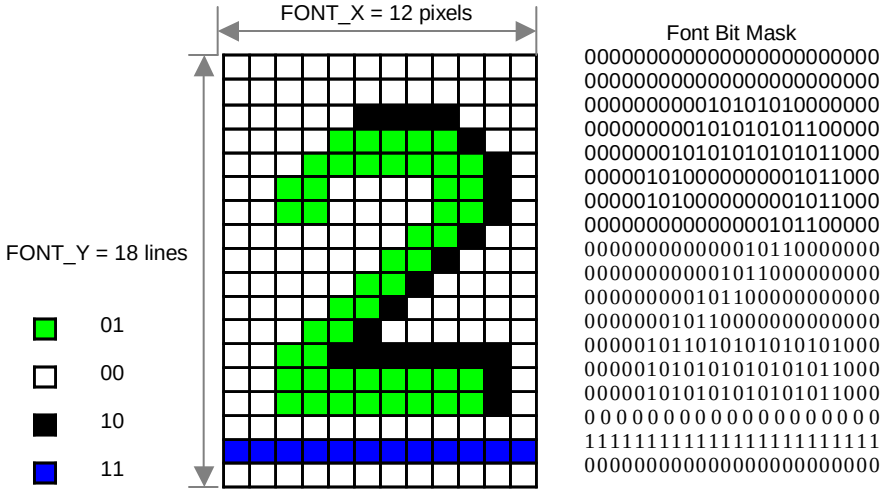



**Figure 6.10-6 Two Bit Per Pixel Font**

### Four Bit per pixel

Four bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 36 addresses. The four bit per pixel OSD programmable font start address is specified in Register 0x08D ~ 0x08C. Each pixel row of a font contains up 12 pixels, with the font row broken up across two consecutive Color Character Font SRAM Memory addresses.

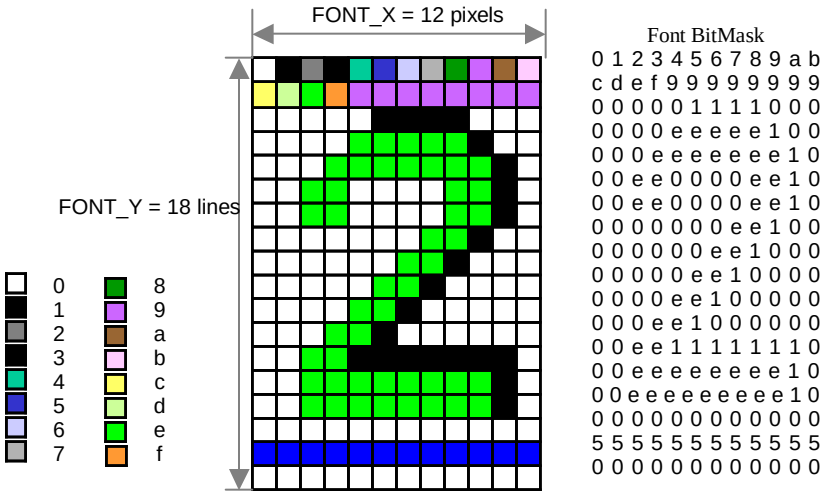



**Figure 6.10-7 Four Bit Per Pixel Font**

**OSD Color Character Font SRAM Memory Arrangement Map:**

A single ported SRAM (4096-words × 24-bits) is used for storing character attribute, code index, and programmable fonts. The following example illustrates the contents of SRAM memory for a sample OSD. The OSD is three rows by four columns.

Note: That the OSD Frame SRAM and Font SRAM share the same on Color Character Font SRAM Memory. Thus, the size of the memory map can be traded off against the number of different memory definitions. In particular, the size of the OSD frame and the number of font data must fit in the Color Character Font SRAM Memory. That is, the following inequality must be satisfied.

(OSD_HW+1)×(OSD_VH+1) + 18×CELING (Number of 1-bit per pixel fonts / 9) × 9 +
2×18×CELING (Number of 2-bit pixel fonts / 9) × 9 +
4×18×CELING (Number of 4-bit pixel fonts / 9) × 9 <= 4096

The programmable font start address setting:

OSD One Bit Font Address (FONT1B_ADDR) = (OSD_HW+1)×(OSD_VH+1)

OSD Two Bits Font Address (FONT2B_ADDR) = OSD One Bit Font Address (FONT1B_ADDR) + (Number of 1-bit per pixel fonts) ×(12×18/24)

OSD Four Bits Font Address (FONT4B_ADDR) = OSD Two Bit Font Address (FONT2B_ADDR) + (Number of 2-bit per pixel fonts) ×(2×12×18/24)

Note: The following inequality must be satisfied

MOD (Number of 1-bit pixel fonts / 9) = 0
MOD (Number of 2-bit pixel fonts / 9) = 0
MOD (Number of 4-bit pixel fonts / 9) = 0

**OSD Frame Definition:**

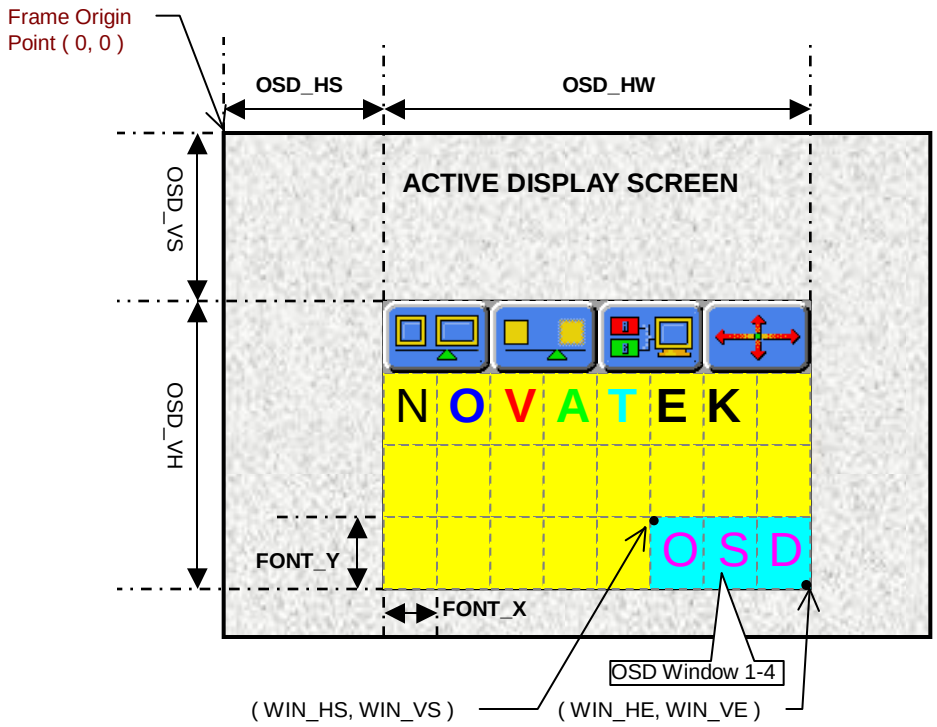



**Figure 6.10-8 OSD Active Frame And Windows**

OSD_HS : OSD Frame Horizontal Start (0 - 2047 pixels)
OSD_HW : OSD Frame Horizontal Width (1 - 64 chars)
OSD_VS : OSD Frame Vertical Start (0 - 2047 pixels)
OSD_VH : OSD Frame Vertical Height (1 - 32 chars)
WIN_HS : OSD Window Horizontal Start (1 - 64 chars)
WIN_HE : OSD Window Horizontal End (1 - 64 chars)
WIN_VS : OSD Window Vertical Start (1 - 32 chars)
WIN_VE : OSD Window Vertical End (1 - 32 chars)
FONT_X : Font X size (12/10 pixels)
FONT_Y : Font Y size (16/18 lines)

## 6.11. DPLL Clock Control

NT68563 Display PLL (Bandwidth 165MHz) for display timing generator.

***Formula*:**
F*out* = (Reference-Freq × DDDS_RATIO [21:0] / DPLL_FREQ_DIV) / $2^{17}$
F*ref* = 14.318 MHz
Note: The value (Reference-Freq × DDDS_RATIO [21:0] / $2^{17}$) must be large to 100 MHz

## 6.12. DISPLAY INTERFACE

NT68563 display interface supports single (24-bit) or dual (48-bit) pixel out format, and supports the 6-bit/color or 8-bit/color LCD panel. Built in internal PLL locking to the reference clock generates all of the display timing to various LCD panels.
NT68563 also provides the programmable display driving capacity to reduce EMI influence as well as programmable clock delay to compensate clock skew.

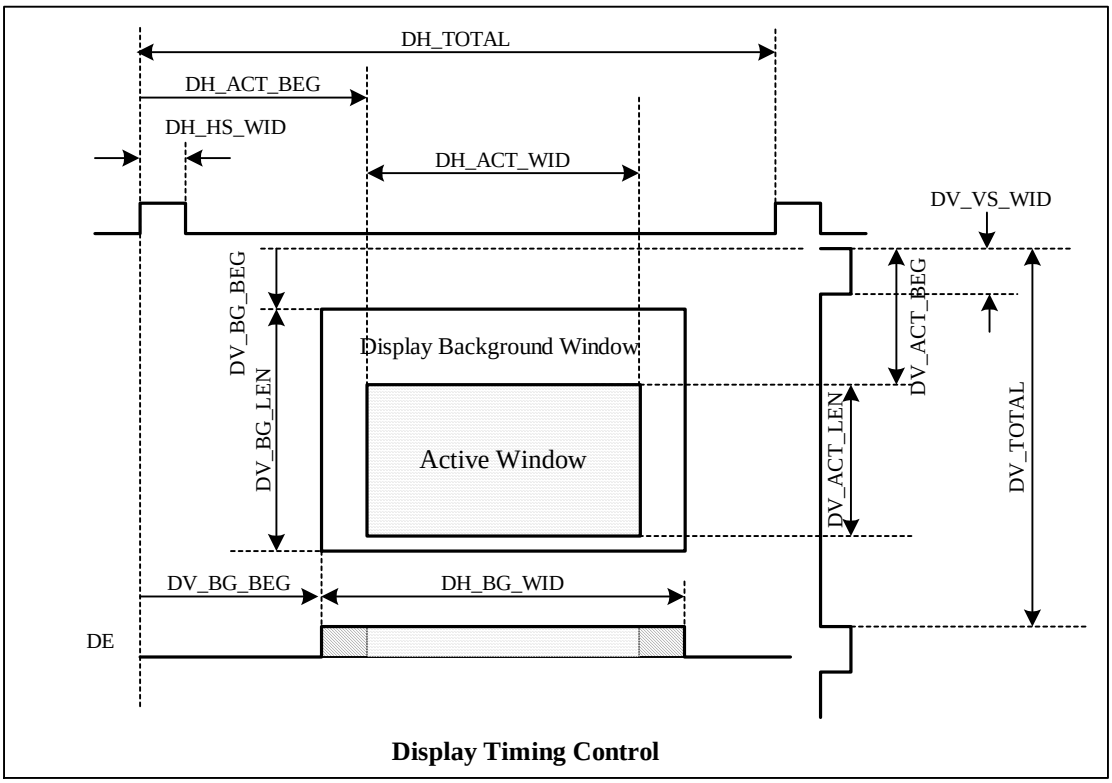



**Figure 6.12-1 Display Timing Control**

### 6.12.1. Scaler Display Data

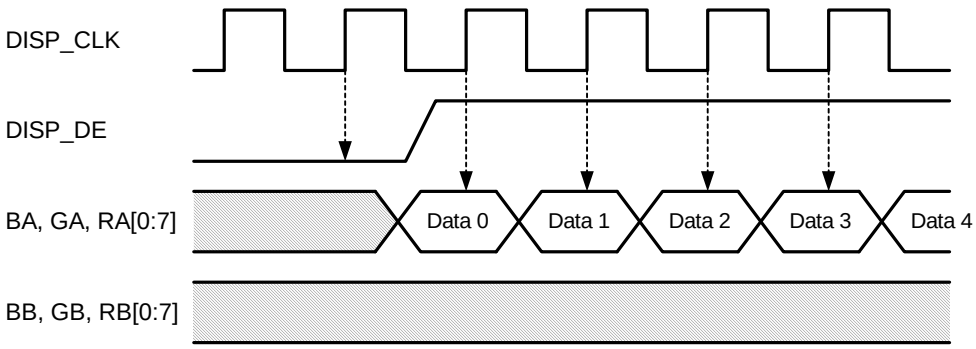



**Figure 6.12-2 Single Pixel Width Display Data**

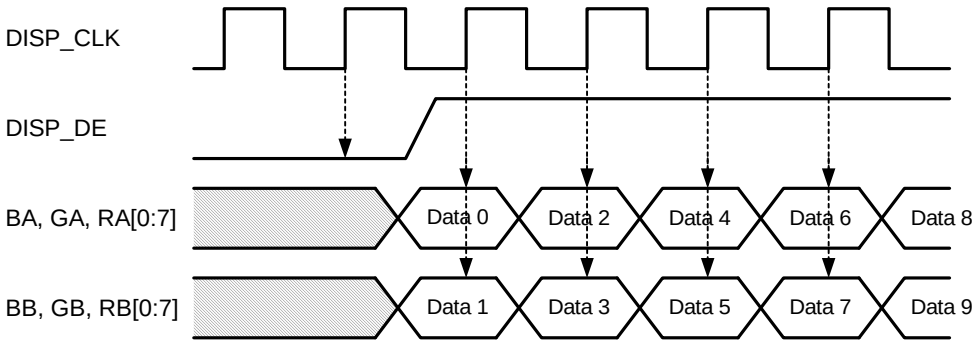



**Figure 6.12-3 Double Pixel Width Display Data**

### 6.12.2. Single/Dual pixel LVDS Transmitter

The NT68563 transmitter is de-signed to support single or dual pixel data transmission between Scaler and Flat Panel Display up to SXGA resolutions. For dual pixel mode, the transmitter converts 24 bits (single Pixel 24-bit color) of CMOS data into 4 LVDS (Low Voltage Differential Signaling) data streams. For single pixel mode, the transmitter converts 48 bits (Dual Pixel 24-bit color) of CMOS data into 8 LVDS (Low Voltage Differential Signaling) data streams Control signals (VSYNC, HSYNC, DE and two user-defined signals) are sent during blanking intervals. At a maximum single pixel rate of 85MHz.

**The LVDS transmitter can support the following:**

1. Single or double pixel mode
2. 24/48-bit panel mapping to the LVDS channels
3. 18/36-bit panel mapping to the LVDS channels
4. Programmable even/odd LVDS swapping
5. Programmable channel swapping (the clocks are fixed)
6. Support up to UXGA 60Hz output

**Supported LVDS 18-bit Panel Data Mappings**

| | |
|---|---|
| Channel 0 | R2, R3, R4, R5, R6, R7, G2 |
| Channel 1 | G3, G4, G5, G6, G7, B2, B3 |
| Channel 2 | B4, B5, B6, B7, HS, VS, DE |
| Channel 3 | Disabled for this mode |

**Panel Data Mappings**

| Dual Pixel mode (When DP_BIT_SHF = 0) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Channel 0 / Channel 4 | R0, R1, R2, R3, R4, R5, G0 | | | | | | | |
| Channel 1 / Channel 5 | G1, G2, G3, G4, G5, B0, B1 | | | | | | | |
| Channel 2 / Channel 6 | B2, B3, B4, B5, HS, VS, DE | | | | | | | |
| Channel 3 / Channel 7 | R6, R7, G6, G7, B6, B7, RSVD | | | | | | | |
| LVDS channel 0 (T0) | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | GA0 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| LVDS channel 1 (T1) | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | BA1 | BA0 | GA5 | GA4 | GA3 | GA2 | GA1 |
| LVDS channel 2 (T2) | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | VS | HS | BA5 | BA4 | BA3 | BA2 |
| LVDS channel 3 (T3) | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Data order | RSVD | BA7 | BA6 | GA7 | GA6 | RA7 | RA6 |
| LVDS channel 4 (T4) | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | GB0 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
| LVDS channel 5 (T5) | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | BB1 | BB0 | GB5 | GB4 | GB3 | GB2 | GB1 |
| LVDS channel 6 (T6) | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | BB5 | BB4 | BB3 | BB2 |
| LVDS channel 7 (T7) | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | BB7 | BB6 | GB7 | GB6 | RB7 | RB6 |

| Dual Pixel mode (When DP_BIT_SHF = 1) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Channel 0 / Channel 4 | R2, R3, R4, R5, R6, R7, G2 | | | | | | | |
| Channel 1 / Channel 5 | G3, G4, G5, G6, G7, B2, B3 | | | | | | | |
| Channel 2 / Channel 6 | B4, B5, B6, B7, HS, VS, DE | | | | | | | |
| Channel 3 / Channel 7 | R0, R1, G0, G1, B0, B1, RSVD | | | | | | | |
| LVDS channel 0 (T0) | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | GA2 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 |
| LVDS channel 1 (T1) | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | BA3 | BA2 | GA7 | GA6 | GA5 | GA4 | GA3 |
| LVDS channel 2 (T2) | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | VS | HS | BA7 | BA6 | BA5 | BA4 |
| LVDS channel 3 (T3) | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | RSVD | BA1 | BA0 | GA1 | GA0 | RA1 | RA0 |
| LVDS channel 4 (T4) | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | GB2 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 |
| LVDS channel 5 (T5) | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | BB3 | BB2 | GB7 | GB6 | GB5 | GB4 | GB3 |
| LVDS channel 6 (T6) | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | BB7 | BB6 | BB5 | BB4 |
| LVDS channel 7 (T7) | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | BB1 | BB0 | GB1 | GB0 | RB1 | RB0 |

## 6.13. Miscellaneous

### 6.13.1. General-Purpose Input Output (GPIO)

- 11 selectable General Purpose Output Pins
- 2 channels shared with HSYNCO, VSYNCO outputs
- 2 selectable output channels with PWM0, PWM1 outputs
- 2 built-in DDC Port, shared with GPO7, GPO8, GPO4, and GPO5
- GPIO Port Configuration

| Designation | Function | I/O | Circuit Structure | Control Bits | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | TCON_EN | DDC1_EN | GI_VSO_EN | BP_VSYNC_EN | GPO4_EN |
| VSO / | GI_VSO | O | Push-Pull | X | 0 | 1 | 0 | X |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DDC1_SDA | IN_VSO | O | Push-Pull | X | 0 | 1 | 1 | X |
| | DDC1_SDA | I/O | | X | 1 | X | X | X |
| | GPO4 | O | - | 1 | 0 | X | X | 1 |
| **Designation** | **Function** | **I/O** | **Circuit Structure** | **Control Bits** | | | | |
| | | | | TCON_EN | DDC1_EN | GI_HSO_EN | BP_HSYNC_EN | GPO5_EN |
| HSO / DDC1_SCL | GI_HSO | O | Push-Pull | X | 0 | 1 | 0 | X |
| | IN_HSO | O | Push-Pull | X | 0 | 1 | 1 | X |
| | DDC1_SCL | I/O | | X | 1 | X | X | X |
| | GPO5 | O | - | 1 | 0 | X | X | 1 |
| **Designation** | **Function** | **I/O** | **Circuit Structure** | **Control Bits** | | | | |
| | | | | TCON_EN | REFCKO_EN | GPO6_EN | | |
| REFCKO | REFCKO | O | - | X | 1 | x | | |
| | GPO6 | O | - | 1 | 0 | 1 | | |
| **Designation** | **Function** | **I/O** | **Circuit Structure** | **Control Bits** | | | | |
| | | | | TCON_EN | DDC0_EN | GPO7_EN | | |
| DDC0_SDA | DDC0_SDA | I/O | - | x | 1 | x | | |
| | GPO7 | O | Push-Pull | 1 | 0 | 1 | | |
| **Designation** | **Function** | **I/O** | **Circuit Structure** | **Control Bits** | | | | |
| | | | | TCON_EN | DDC0_EN | GPO8_EN | | |
| DDC0_SCL | DDC0_SCL | I/O | - | x | 1 | x | | |
| | GPO8 | O | Push-Pull | 1 | 0 | 1 | | |
| **Designation** | **Function** | **I/O** | **Circuit Structure** | **Control Bits** | | | | |
| | | | | TCON_EN | PWM1_EN | GPO9_EN | | |
| PWM1 | PWM1 | I/O | - | X | 1 | 0 | | |
| | GPO9 | O | Push-Pull | 1 | 0 | 1 | | |
| **Designation** | **Function** | **I/O** | **Circuit Structure** | **Control Bits** | | | | |
| | | | | TCON_EN | PWM0_EN | GPO10_EN | | |
| PWM0 | PWM0 | I/O | - | X | 1 | 0 | | |
| | GPO10 | O | Push-Pull | 1 | 0 | 1 | | |

**Table 6.13-1 GPIO Control Circuit Structure**

### 6.13.2. DDC Port Control

The function is designed to comply to the DDC Standard proposed by VESA with the exception that it is not Access. Bus capable. The features:

1. Dual independent input DDC channel
2. Pure hardware solution for VESA DDC1/2B

3. Selectable 128/256 Bytes EDID-Buffer for hardware DDC port

This block is a 128/256-byte selectable dual-mode DDC port. It is designed for use in applications requiring serial transmission of configuration and control information. Two modes of operation have been implemented

- **Transmit Only Mode for DDC1**
- **Bi-directional Mode for DDC2B**

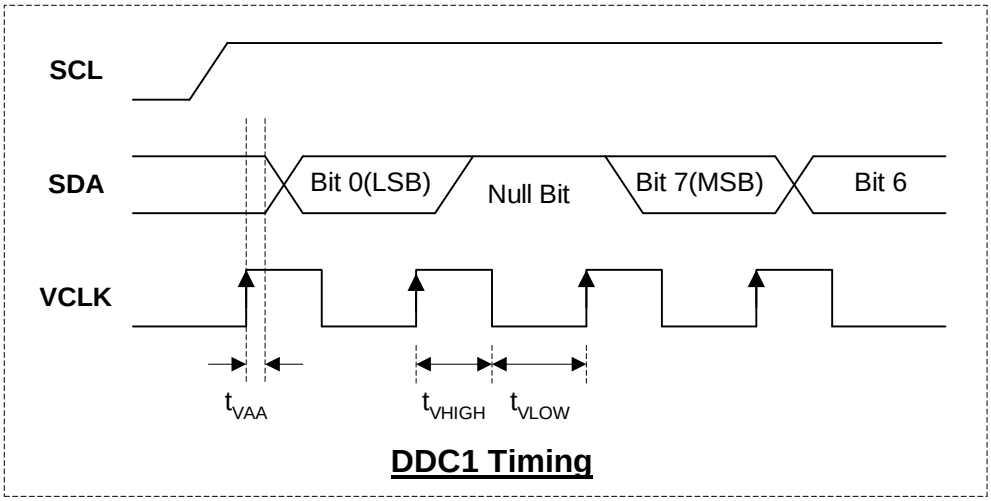



**Figure 6.13-1 DDC1 Timing**

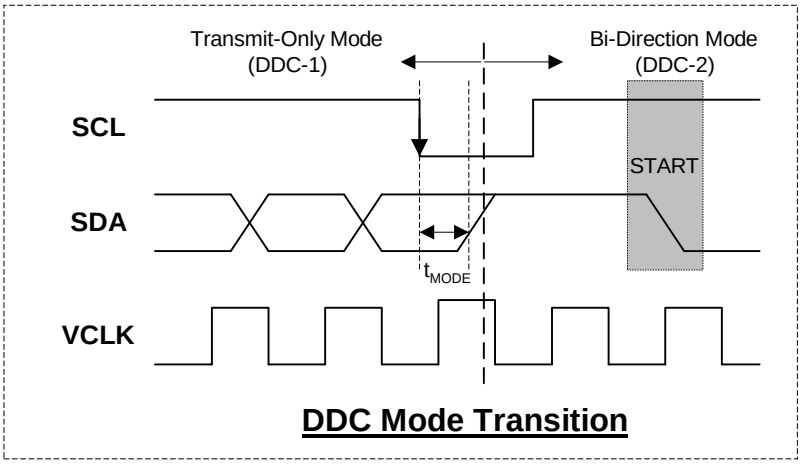



**Figure 6.13-2 DDC Mode Transition Timing**

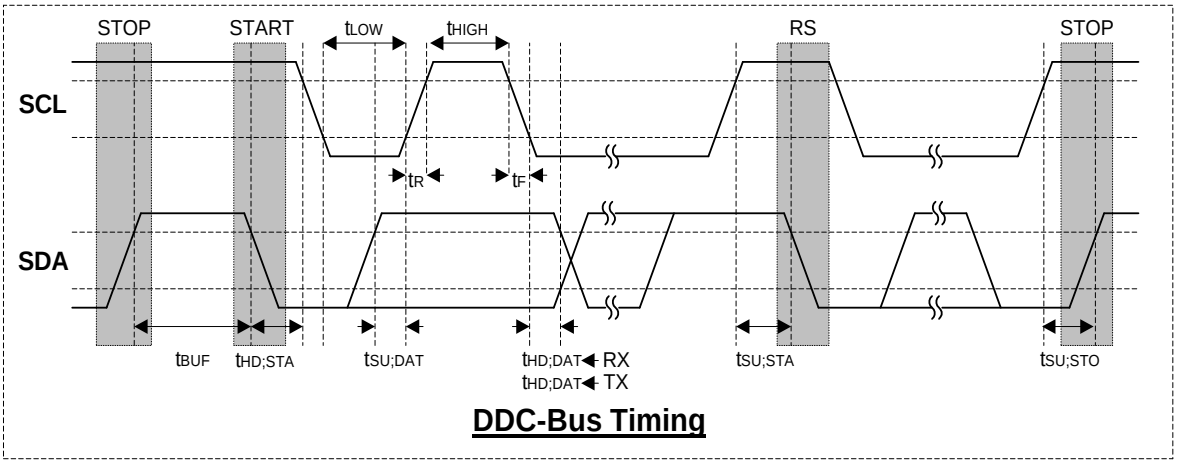



**Figure 6.13-3 DDC-Bus Timing**

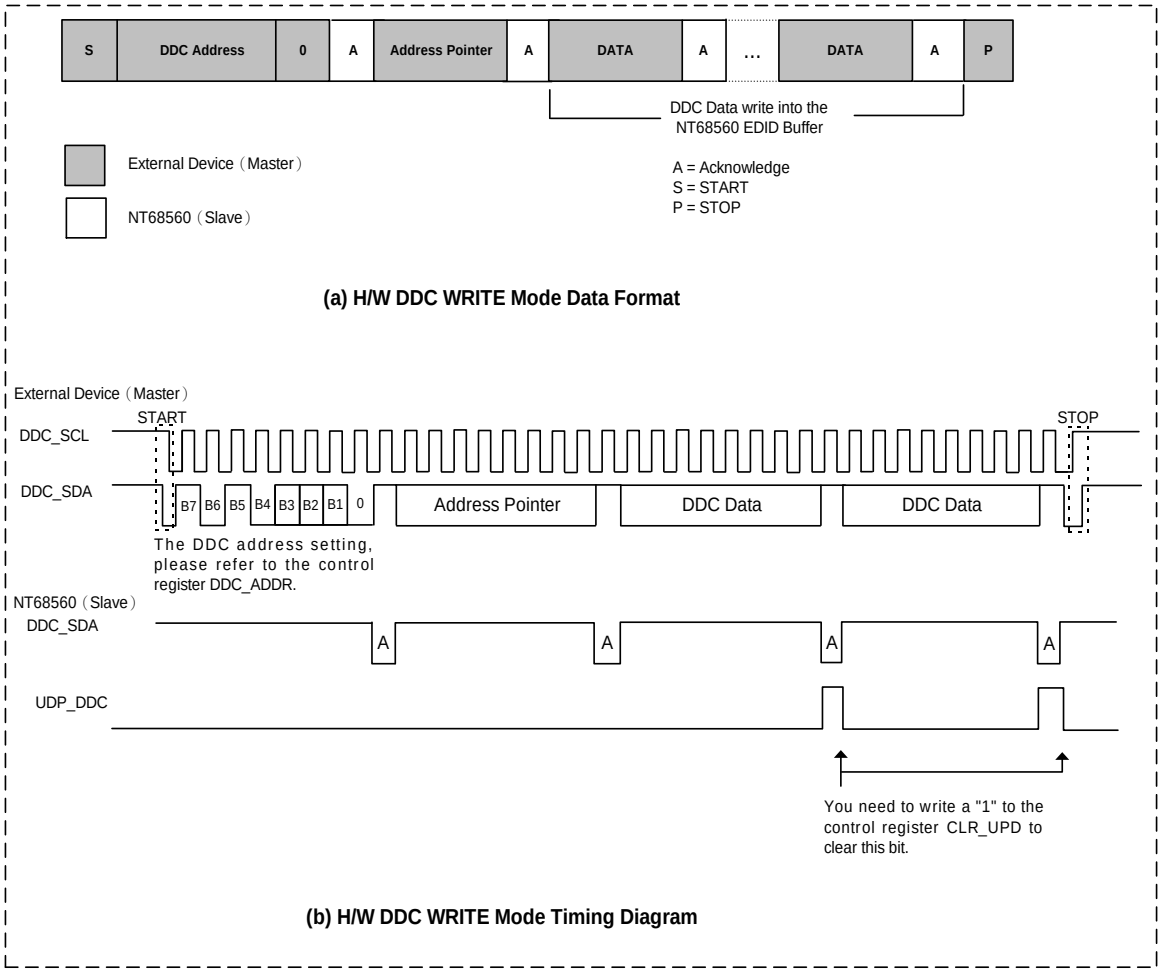



**Figure 6.13-4 H/W DDC Write Mode Timing Diagram**

### 6.13.3. PWM Output

There are two Pulse Width Modulation signal pins available for controlling the LCD back light or audio volume, PWM0 and PWM1. The duty cycle and Frequency of these signals is programmable.

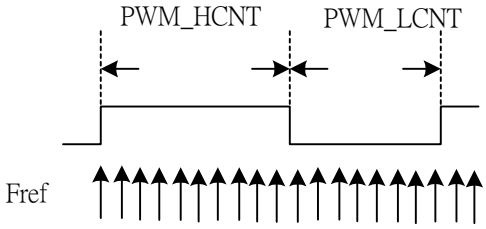



**Figure 6.13-5 Pulse Width Modulation Signal (PWM)**

When clock source select from reference clock

$$F_{PWM\_CLK} = F_{REFCLK} / (PWM\_DIV\ 1 \times PWM\_DIV\ 2)$$

When clock source select from Display Hsync

$$F_{PWM\_CLK} = F_{DISP\_HS} / (PWM\_DIV\ 1 \times PWM\_DIV\ 2)$$

$$F_{PWM} = \frac{F_{PWM\_CLK}}{(PWM\_HCNT + PWM\_LCNT)}$$

$$Duty = \frac{PWM\_HCNT}{(PWM\_HCNT + PWM\_LCNT)}$$

$$PWM\_HCNT = \frac{Duty \times F_{PWM\_CLK}}{F_{PWM}}$$

$$PWM\_LCNT = \frac{(1 - Duty) \times F_{PWM\_CLK}}{F_{PWM}}$$

| PWM_HCNT | PWM_LCNT | PWM Output |
|---|---|---|
| 0 | 0~255 | DC ‘0’ |
| 1~255 | 0 | DC ‘1’ |
| 1~255 | 1~255 | PWM pulse |

## 6.14. MCU Interface

NT68563 supports two host interface one two wires of I2C bus and the other Parallel 4-Bits bus interface and one IRQ output to communicate with MCU.

### 6.14.1. Host Interface

NT68563 support two bus types interface the host CPU. Parallel and I2C bus are select through BUSTYPE pin. When BUSTYPE configuring a '1' will configure chip for parallel interface. A '0' will configure chip for serial interface. It can let us access I/O registers and memory described as follows.

### 6.14.2. I2C Bus

I2C data rate is up to 400K bits/s. NT68563's I2C address can be selected in the range B0~B5, the value of address bit 1/2 depends on the level of pin AD0/ AD1 while NT68563 is on reset state

**EX**:
IF NT68563's AD0/AD1 pins do resisters pull both up. When the reset signal (RSTn pin) is going from low to high, the two pins' value ('1') will be latched, then the I2C address is decided as B6/B7.

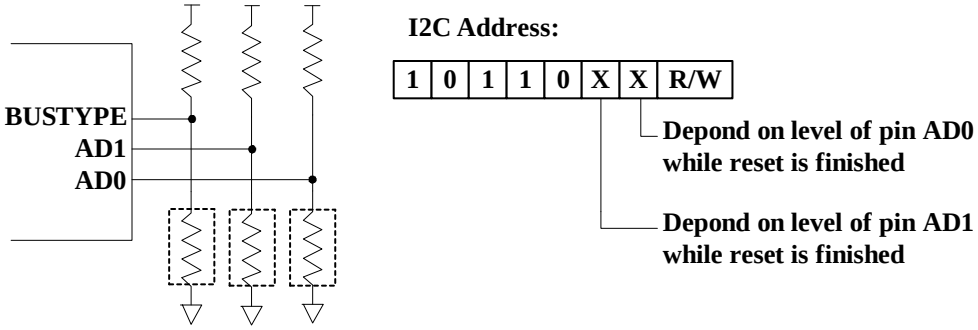
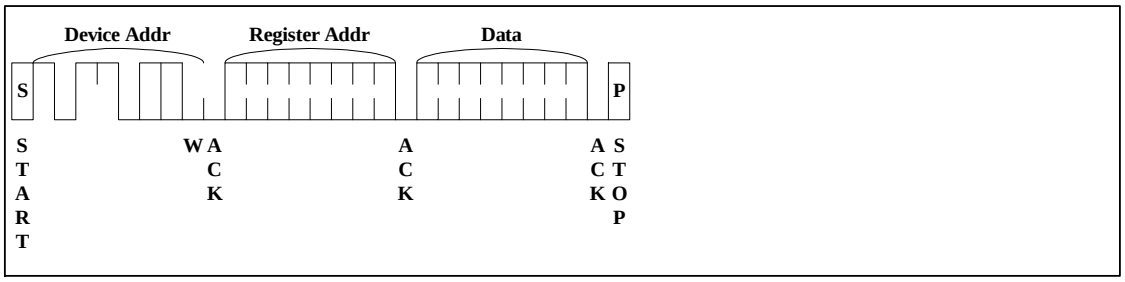



**Figure 6.14-1 I2C Bus Addressing**

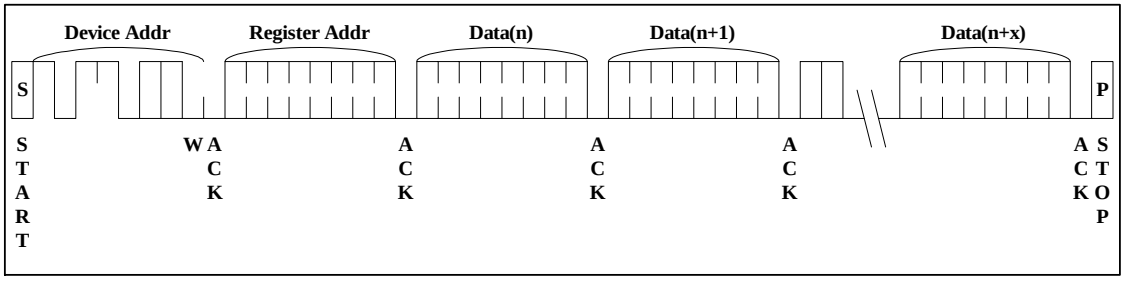
### 6.14.3. I2C Protocol

**General Register R/W**

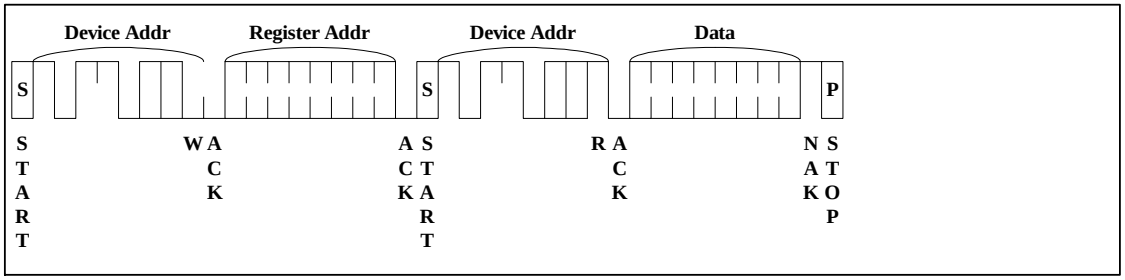
**Byte Write**




**Sequential Write**




**Byte Read**




**Sequential Read**

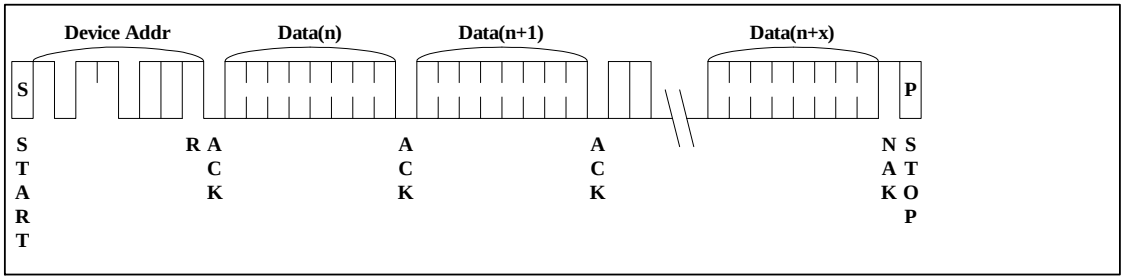
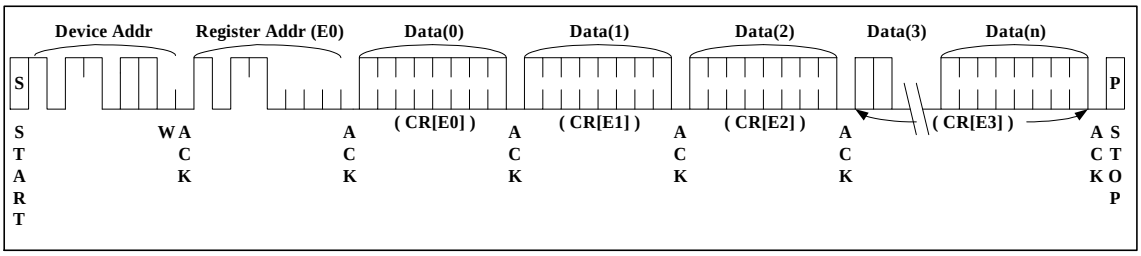



**Figure 6.14-2 I2C General Register Read/Write Protocol**

## Index Port Access R/W

**Index Port Write Access**




**Index Port Read Access**

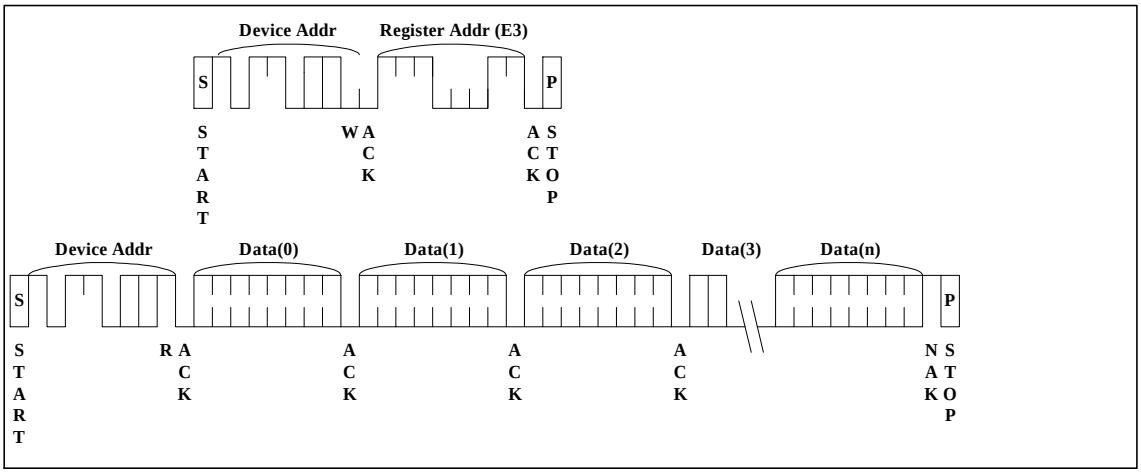
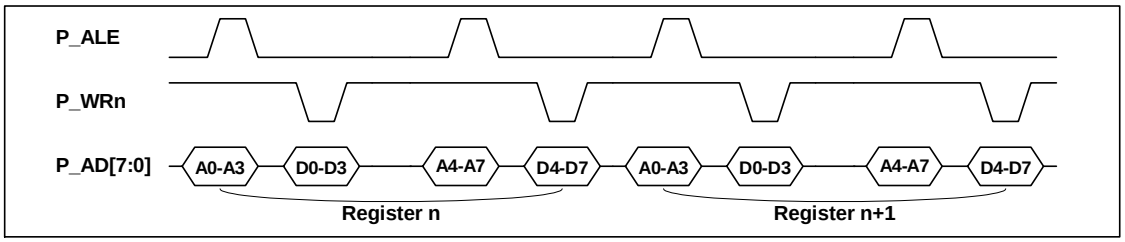



**Figure 6.14-3 I2C Index Port Data Access Protocol**

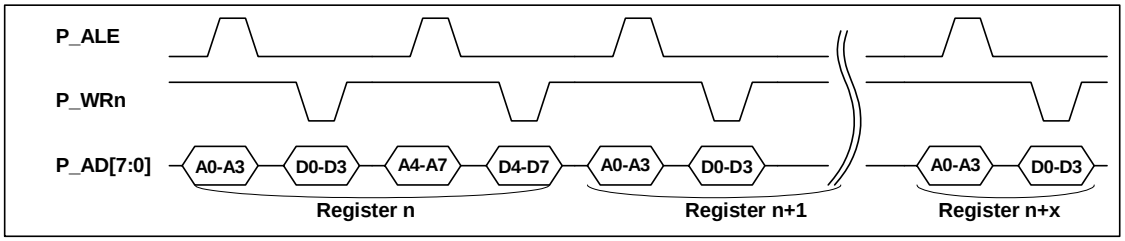
### 6.14.4. Parallel Protocol

**General Register R/W**

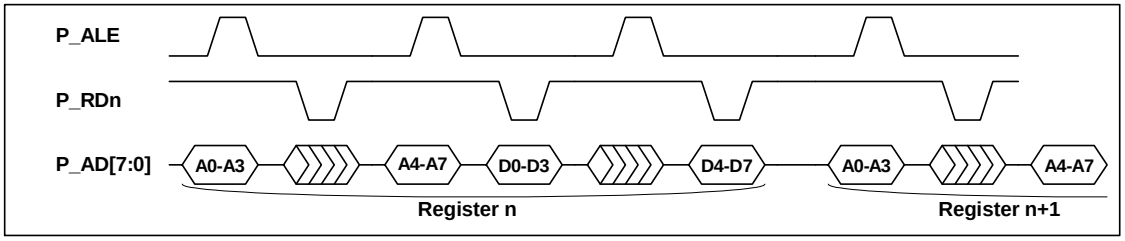
**Byte Write :**




**Sequential Write :**




**Byte Read :**




**Sequential Read :**

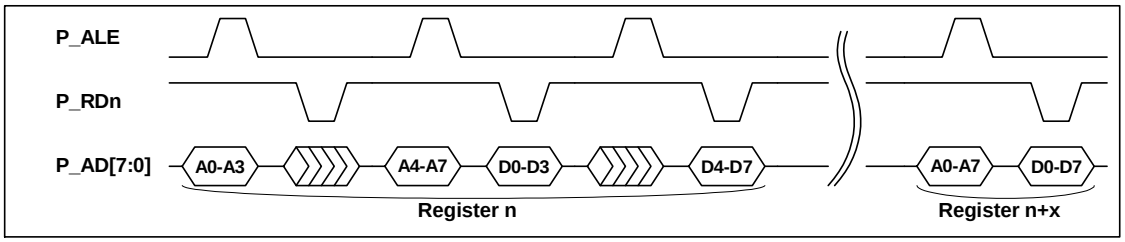



**Figure 6.14-4 Parallel 4-Bus General Register Read/Write Protocol**

## Internal SRAM Write/Read

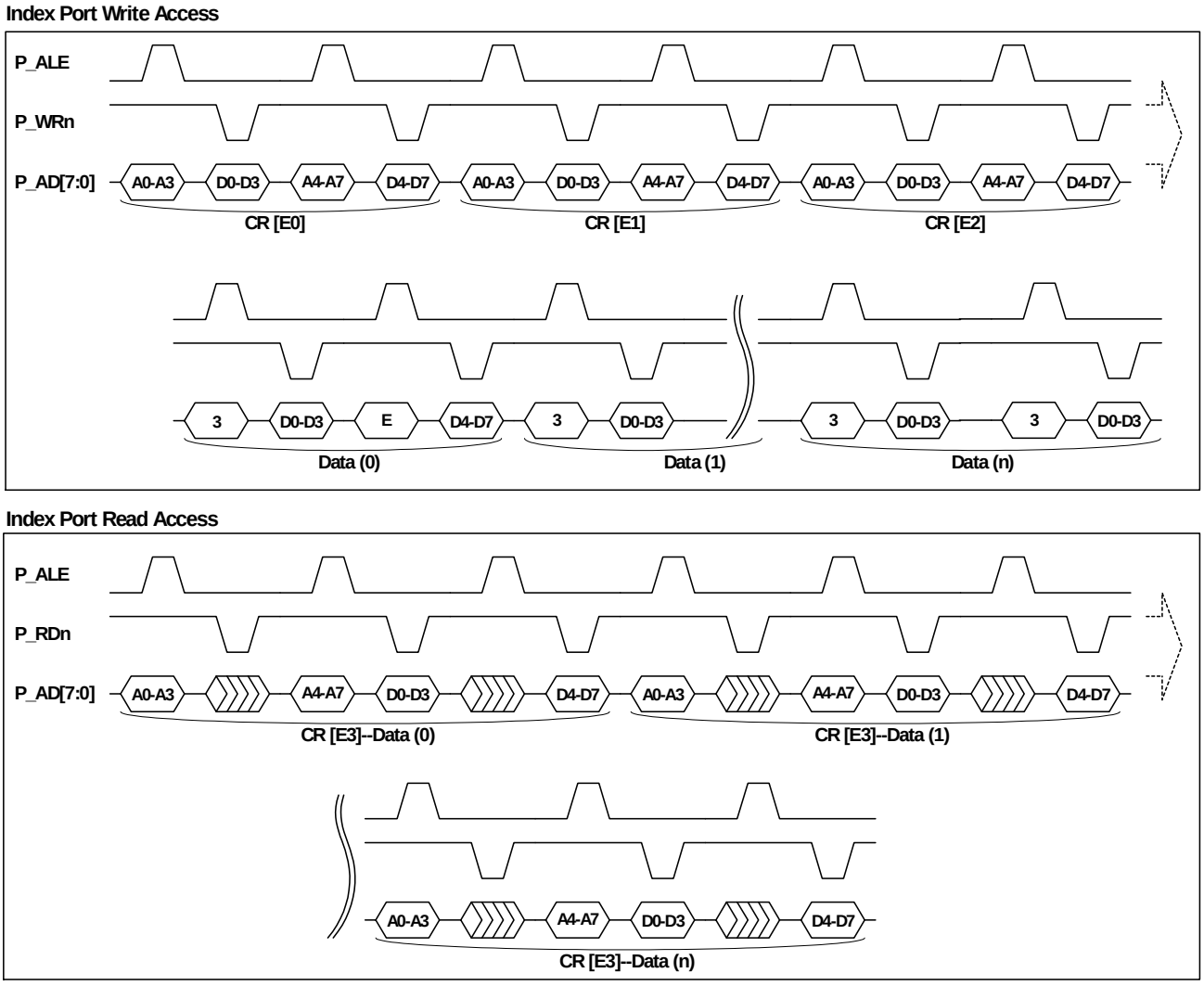



**Figure 6.14-5 Parallel Bus Index Port Access Protocol**

### 6.14.5. IRQn Interrupt Sources

NT68563 provides an interrupt request output pin IRQn. The following figure shows the detail structure of the IRQn sources.

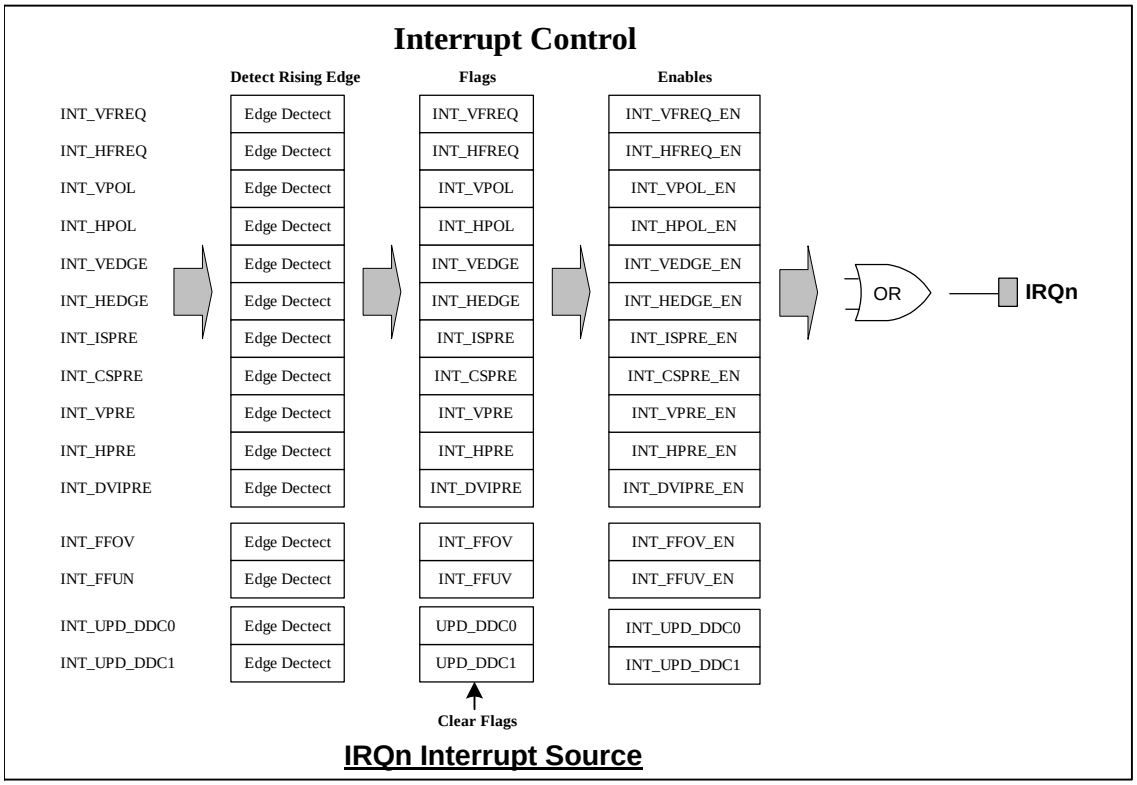



**Figure 6.14-6 IRQn Interrupt Block Diagram**

| INTHV_IRQ | Meaning | Action |
|---|---|---|
| INT_VFREQ | Vsync Frequency Change | It will be activated when the Input frequency of Vsync changes. |
| INT_HFREQ | Hsync Frequency Change | It will be activated when the Input frequency of Hsync changes. |
| INT_VPOL | V-Polarity Change INT | It will be activated when the Input Polarity of Vsync changes. |
| INT_HPOL | H-Polarity Change INT | It will be activated when the Input Polarity of Hsync changes. |
| INT_VEDGE | Vsync Edge INT | It will be activated when the Vsync rising edge is occur. |
| INT_HEDGE | Hsync Edge INT | It will be activated when the Hsync rising edge is occur. |
| INT_ISPRE | Interlaced Sync INT | It will be activated when the Interlaced Sync is present. |
| INT_ CSPRE | Composite Sync INT | It will be activated when the Composite Sync is present. |
| INT_VPRE | Vsync Present INT | It will be activated when the Vsync is present. |
| INT_HPRE | Hsync Present INT | It will be activated when the Hsync is present. |
| INT_DVIPRE | DVI sync Present INT | It will be activated when the DVI sync is present. |
| INT_FFOV | FIFO Overflow INT | It will be activated when the FIFO is overflow |

| | | |
|---|---|---|
| INT_ FFUV | FIFO Underflow INT | It will be activated when the FIFO is underflow |
| INT_UPD_DDC0 | DDC0 updated INT | It will be activated when DDC0 Ram-Buffer contents updated. |
| INT_ UPD_DDC1 | DDC1 updated INT | It will be activated when DDC1 Ram-Buffer contents updated. |

**Table 6.14-1 IRQn Interrupt**

# 7. Electrical Specifications

3.3V Supply voltage range, $V_{3.3}$ (see Note1)……-0.3V to 4V
1.8V Supply voltage range, $V_{18}$ (see Note2)……-0.3V to 1.98V
Output voltage range, Vo……-0.3V to $V_{33}$ +0.3V
Input voltage range (5V Tolerant), Vi……-0.3V to $V_{5V}$ +0.3V
Electrostatic Discharge, $V_{ESD}$……±2.0kV
Ambient Operating temperature, $T_A$……0°C to 70°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds……260°C
Junction Temperature……150°C
Storage temperature range, Tstg……-40°C to 125°C
Storage humidity……< 60% HR
Storage Life (Storage Temperature < 30 ℃)…… 1 year

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.
- Note1: Includes pins ADC_VAA, AVCC, PVCC, DVDD.
- Note2: Includes pins CVDD, PLL_VDD

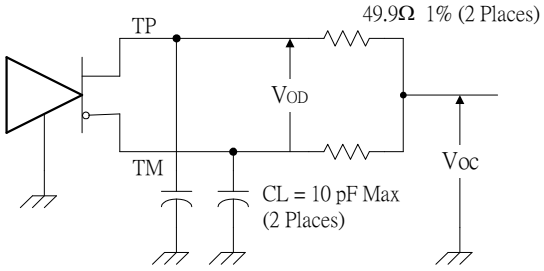
## 7.1. DC Electrical Characteristics

**($T_A$ = 25°C, Oscillator freq. = 14.318MHz, unless otherwise specified)**

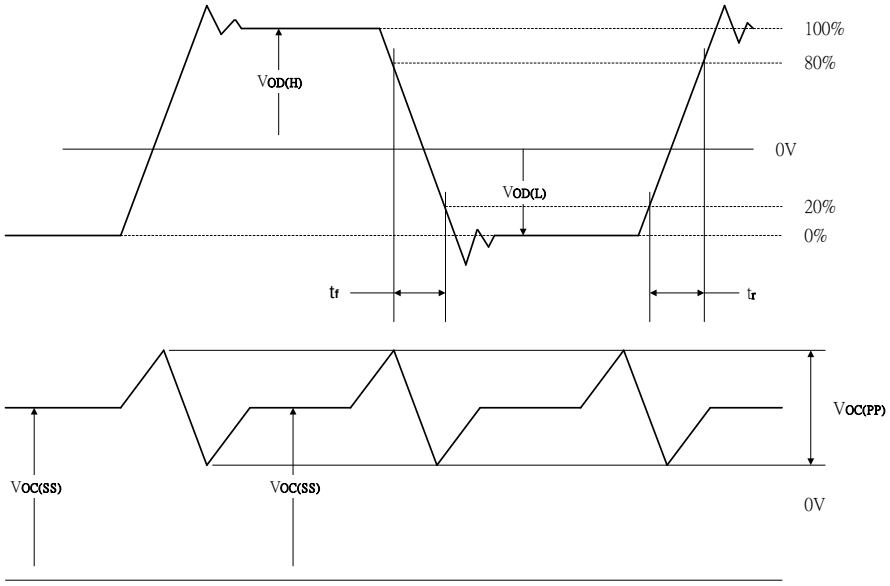
| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Power Requirements** | | | | | | |
| $V_{CVDD}$ | 1.8 V digital power supply | 1.71 | 1.8 | 1.89 | V | CVDD |
| $V_{PLL}$ | PLL power supply | 1.71 | 1.8 | 1.89 | V | PLL_VDD |
| $V_{ADC}$ | R/G/B channel ADC analog power supply | 3.15 | 3.3 | 3.47 | V | ADC_VAA, |
| $V_{TMDSA}$ | TMDS analog power supply | 3.15 | 3.3 | 3.47 | V | AVCC |
| $V_{TMDSP}$ | TMDS PLL power supply | 3.15 | 3.3 | 3.47 | V | PVCC |
| $V_{DDD}$ | Display interface power supply | 3.15 | 3.3V | 3.47 | V | DVDD |
| $I_{VDD}$ | 1.8 V digital power supply current | | TBD | TBD | mA | No Loading (Includes CVDD, PLL_VDD) |
| $I_{ADC}$ | ADC power supply current | | TBD | TBD | mA | No Loading |
| $I_{TMDS}$ | TMDS power supply current | | TBD | TBD | mA | No Loading |
| $I_{DDD}$ | Display interface power supply current | | TBD | TBD | mA | No Loading |
| $I_{DD}$ | Operating current (Total) | | TBD | TBD | mA | No Loading |
| $I_{DDPD}$ | Power down current | | 30 | | mA | No Loading |
| **Digital Outputs** | | | | | | |
| $V_{OH}$ | Output high voltage | 2.0 | | $V_{DD}$ | V | DISP_DE, DISP_VS, DISP_HS, DISP_CLK |
| $V_{OL}$ | Output low voltage | GND | | 0.8 | V | |
| $V_{OH}$ | Output high voltage for PWM/DDC | | | 5 | V | PWM[1:0], DDC_SCL[1:0], DDC_SCL[1:0], |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{OZ}$ | Tri-State Leakage Current | -25 | | 25 | uA | |
| | | | | | | |
| $I_{OH1}$ | Output high current | -16 | | -2 | mA | ($V_{OH}$ = 2.5V) DISP_DE, DISP_VS, DISP_HS, DISP_CLK, REFCKO, |
| $I_{OL1}$ | Output low current | 2 | | 16 | mA | ($V_{OL}$ = 0.4V) DISP_DE, DISP_VS, DISP_HS, DISP_CLK, REFCKO |
| $I_{OH2}$ | Output high current | | | -4 | mA | ($V_{OH}$ = 2.5V) IRQn, IN_HSO, IN_VSO |
| $I_{OL2}$ | Output low current | 4 | | | mA | ($V_{OL}$ = 0.4V) IRQn, IN_HSO, IN_VSO |
| **LVDS Outputs** | | | | | | |
| $\|V_{OD}\|$ | Differential Steady-state Output Voltage Magnitude | 240 | | 490 | mV | $R_L$ = 100Ω, See Figure 7.1.1 |
| $\triangle\|V_{OD}\|$ | Change in the Steady-state Differential Output Voltage Magnitude between Opposite binary States | | | 35 | mV | |
| $V_{OC(SS)}$ | Steady-state Common-mode Output Voltage | 1.125 | | 1.475 | V | See Figure 7.1.1 |
| $V_{OC(PP)}$ | Peak-to-peak Common-mode Output Voltage | | 80 | 150 | mV | |
| $I_{OS}$ | Short-circuit Output Current | | | ±24 | mA | $V_{O(TP)}$ = 0 |
| | | | | ±12 | mA | $V_{OD}$ = 0 |
| $I_{OZ}$ | | | ±1 | | μA | $V_O$ = 0 to Vcc |
| **Analog Input** | | | | | | |
| $V_{IAMIN}$ | Minimum Input Voltage Range | | | 0.55 | V p-p | |
| $V_{IAMAX}$ | Maximum Input Voltage Range | 0.9 | | | V p-p | $V_{IAMAX}$ |
| **Digital Input** | | | | | | |
| $V_{IH}$ | Input high voltage | 2.0 | | $V_{DD}$ | V | Y[7:0], |
| $V_{IL}$ | Input low voltage | GND | | 0.8 | V | |
| $V_{T+(HSYNC)}$ | Schmitt Trigger Positive Going Threshold Voltage for HSYNC Inputs | 1.5 | 1.6 | 2.2 | V | HSYNCI0, HSYNCI1 |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{T-(HSYNC)}$ | Schmitt Trigger Negative Going Threshold Voltage for HSYNC Inputs | 0.7 | 1.1 | 1.4 | V | HSYNCI0, HSYNCI1 |
| $V_{T+(VSYNC)}$ | Schmitt Trigger Positive Going Threshold Voltage for VSYNC Inputs | | 1.8 | 2.0 | V | VSYNCI0, VSYNCI1 |
| $V_{T-(VSYNC)}$ | Schmitt Trigger Negative Going Threshold Voltage for VSYNC Inputs | 0.8 | 1.5 | | V | VSYNCI0, VSYNCI1 |
| $V_{IHC}$ | Clock high voltage | 2.0 | | $V_{DD}$ | V | YUV_CLK, |
| $V_{ILC}$ | Clock low voltage | GND | | 0.4 | V | |
| $I_{IH}$ | Input high current | -25 | | 25 | $\mu$A | ($V_{IH}$ = 2.5V) |
| $I_{IL}$ | Input low current | -25 | | 25 | $\mu$A | ($V_{IL}$ = 0.4V) |

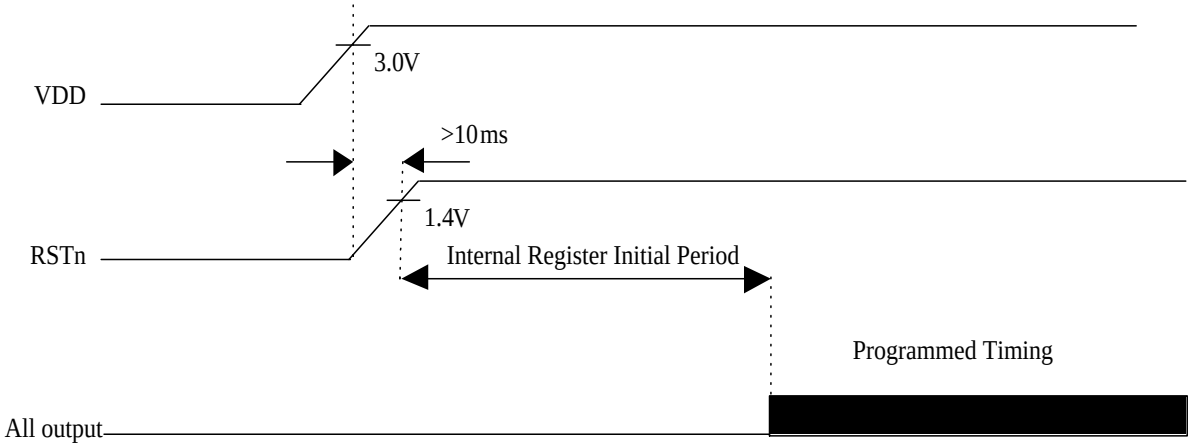



(a)SCHEMATIC




(b) WAVEFORMS

**Figure 7.1-1 Test Load and Voltage Definitions for LVDS Outputs**




**Power -up Sequence**

**Figure 7.1-2 Power-up Sequence**

## 7.2. AC Electrical Characteristics

(VDD=3.3V, TA=25°C, Oscillator freq.=14.318MHz, unless otherwise specified)

**ADCPLL**

| Phase-locked loop | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $j_{PLL}$ | Short term jitter | fclkout=165MHz | - | - | 120 | ps |
| | Long term jitter | fclkout=165MHz | - | - | 1.2 | ns |
| DR | Divider ratio | - | 2 | - | 4096 | |
| $f_{CLKIN}$ | Input clock frequency range | - | 15 | - | 110 | kHz |
| $f_{CLKOUT}$ | Output clock frequency range | XF type<br>EF type | 12<br>12 | - | 110<br>165 | MHz |
| $t_{COAST}$ | Maximum coast mode time | - | - | - | 3 | ms |
| $t_{CAP}$ | PLL capture time | In start-up conditions | - | - | 5 | ms |
| $\delta$ | CKOUT clock duty cycle | 165 MHz output | 45 | 50 | 55 | % |

| Clamping Pulse | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $t_{DELAY}$ | Clamp pulse delay time | CLAMP_BEG<5:0>=0x00 | - | 0 | - | 4/CKOUT |
| | | CLAMP_BEG<5:0>=0x0F | - | 15 | - | 4/CKOUT |
| $t_{WIDTH}$ | Clamp pulse width | CLAMP_WID<5:0>=0x01 | - | 1 | - | 4/CKOUT |
| | | CLAMP_WID<5:0>=0x0F | - | 15 | - | 4/CKOUT |
| $t_{COR1}$ | Clamp correction time to within ±10 mV | ±100mV black level input variation; clamp capacitor = 4.7nF | - | - | 300 | ns |
| $t_{COR2}$ | Clamp correction time to less than 1 LSB | ±100mV black level input variation; clamp capacitor = 4.7nF | - | - | 10 | Lines |

| Analog-to-Digital Converter | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| fs | Sampling frequency | X type<br>E type | 10<br>10 | - | 110<br>165 | MHz |
| B | Bandwidth | - | 150 | - | - | Mhz |
| $G_{MATCH}$ | Channel to channel match | - | - | 2 | 5 | % |
| Vin(p-p) | Input signal voltage (peak-peak) | Corresponding to full scale output | 0.55 | 0.7 | 0.9 | V |
| DNL | DC differential non linearity | From analog input to digital output; ramp input; $f_{CLK}$ = 165 MHz (E type); $f_{CLK}$ = 110 MHz (X type); | - | ±0.5 | ±0.9 | LSB |

| | | | | | | |
|---|---|---|---|---|---|---|
| INL | DC integral non linearity | From analog input to digital output; ramp input $f_{CLK}$ = 165MHz | - | ±0.6 | ±1.5 | LSB |
| ENOB | Effective number of bits | From analog input to digital output;10KHz sine wave input; ramp input; $f_{CLK}$ = 165MHz (E type); $f_{CLK}$ = 110MHz (X type); | - | 7 | - | bits |
| THD | | Input 1V(p-p) and 10MHz | - | - | 1 | % |

No Missing Codes is guaranteed.

| Signal-to-Noise Ratio | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| S/N | Signal-to-noise ratio | Maximum gain<br>X type -- $f_{CLK}$=110MHz<br>E type -- $f_{CLK}$=165MHz | - | 45 | - | dB |
| | | Minimum gain<br>X type -- $f_{CLK}$=110MHz<br>E type -- $f_{CLK}$=165MHz | - | 44 | - | dB |

**TMDS Receiver**

| TMDS Receiver | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{OP}$ | Operating Frequency range | XF type<br>EF type | 25<br>25 | - | 110<br>165 | MHz |
| $t_{JJT}$ | Jitter tolerance | | 2 | - | - | ns |
| $t_{START}$ | Receiver Startup Time | | - | - | 10 | ms |
| $t_{DPS}$ | Intra-Pair (+ to -) Differential Input Skew | 165MHz 1 pixel/clock | | | 290 | ps |
| $t_{CCS}$ | Channel to Channel Differential Input Skew | 165MHz 1 pixel/clock | | | 5.0 | ns |
| $C_{IN}$ | TMDS Input Pin Capacitance | | - | 7 | - | pF |

**Sync Processor (Oscillator freq.=12MHz)**

| H/V Sync Processor | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{VSYNC}$ | Vsync Input Frequency | Vsync Duty Cycle = 40% | 15 | - | 250 | Hz |
| $f_{VCLK}$ | Vsync Input Frequency for DDC-1 Mode | Supply VCLK for DDC-1 mode only | - | - | 25 | KHz |
| $t_{VPW}$ | VSYNC input Pulse Width | Vsync Duty Cycle < 40% | - | - | 4.43 | ms |
| $f_{HSYNC}$ | Hsync Input Frequency | Hsync Duty Cycle = 40% | 15 | - | 250 | KHz |
| $t_{HPW}$ | HSYNC input Pulse Width | Hsync Duty Cycle < 40% | - | - | 8.66 | us |
| $t_{HPW(COMP)}$ | HSYNC input Pulse Width | Hsync Duty Cycle < 40% | - | - | 8.66 | us |
| $t_{HTTT(COMP)}$ | Horizontal total time - $t_{HPW(COMP)}$ | | 8.66 | | | us |

**I2C Bus Timing**

| I2C Bus Timing | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $f_{SCL}$ | SCL clock frequency | 0.00 | 400 | kHz |
| $t_{SUSTO}$ | STOP setup time | 0.60 | | us |
| $t_{BUF}$ | Bus free time between a STOP and START | 1.30 | | us |
| $t_{HDSTA}$ | START hold time | 0.60 | | us |
| $t_{LOW}$ | SCL clock pulse width low | 1.30 | | us |
| $t_{IICR}$ | IIC bus rise time | | 300 | ns |
| $t_{HDDAT}$ | DATA hold time | 0.00 | | us |
| $t_{HIGH}$ | SCL clock pulse width high | 0.60 | | us |
| $t_{ICF}$ | IIC bus fall time | | 300 | ns |
| $t_{SUDAT}$ | Data setup time | 100 | | ns |
| $t_{SUSTA}$ | START setup | 0.60 | | us |

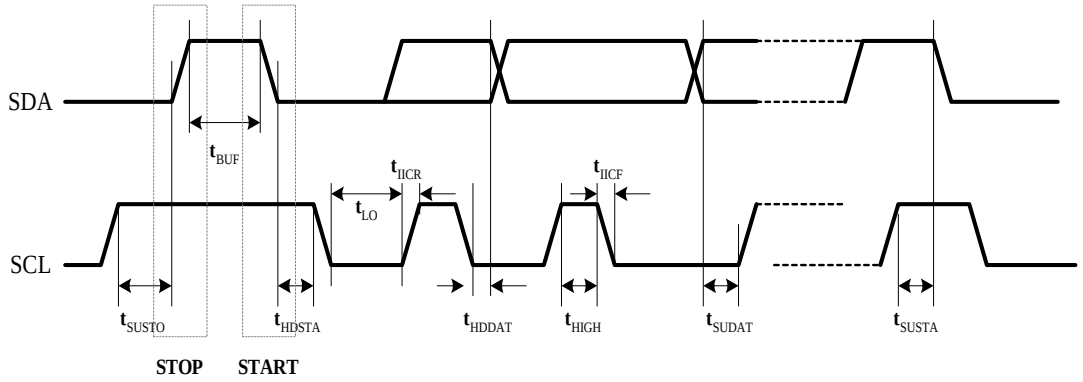


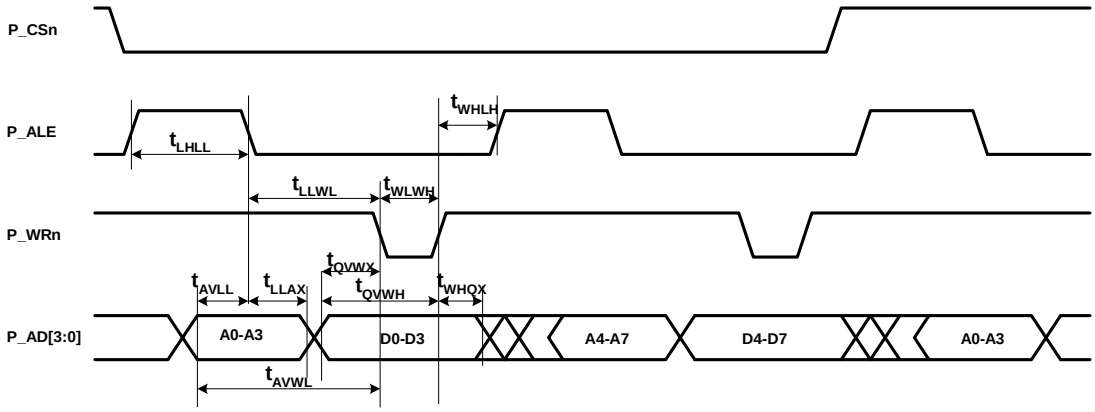

**Figure 7.2-1 I2C Bus Timing**

**Parallel 4-Bits Bus Interface Timing**

| Symbol | Parameter | | | Variable Osc. | | |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Unit |
| $t_{LHLL}$ | ALE Pulse Width | 10 | | 2 $t_{CLCL}$ – Δ | | ns |
| $t_{AVLL}$ | Address Valid to ALE Low | 2 | | $t_{CLCL}$ – Δ | | ns |
| $t_{LLAX}$ | Address Held After ALE Low | 1 | | $t_{CLCL}$– Δ | | ns |
| $t_{RLRH}$ | RD Pulse Width | 30 | | 6 $t_{CLCL}$ – Δ | | ns |
| $t_{WLWH}$ | WR Pulse Width | 30 | | 6 $t_{CLCL}$ – Δ | | ns |
| $t_{RLDV}$ | RD Low to Valid Data In | 10 | 60 | | 4 $t_{CLCL}$ | ns |
| $t_{RHDX}$ | Data Hold After RD | 0 | | 0 | 2 $t_{CLCL}$ | ns |
| $t_{RHDZ}$ | Data Float After RD | | 20 | | 2 $t_{CLCL}$ | ns |
| $t_{LLDV}$ | ALE Low to Valid Data In | | 55 | | 8 $t_{CLCL}$ – 150 | ns |
| $t_{AVDV}$ | Address to Valid Data In | | 60 | | 9 $t_{CLCL}$ – 165 | ns |
| $t_{LLWL}$ | ALE Low to RD or WR | 8 | 125 | 3 $t_{CLCL}$– Δ | 3 $t_{CLCL}$ + Δ | ns |
| $t_{AVWL}$ | Address Valid to RD or WR Low | 20 | | 4 $t_{CLCL}$ – 130 | | ns |
| $t_{QVWX}$ | Data Valid to WR Transition | 0 | | $t_{CLCL}$– Δ | | ns |
| $t_{WHQX}$ | Data Hold After WR | 0 | | $t_{CLCL}$– Δ | | ns |
| $t_{QVWH}$ | Data valid to WR high | 10 | | $t_{CLCL}$– Δ | | ns |
| $t_{RLAZ}$ | Data Float After RD | | 15 | | 0 | ns |
| $t_{WHLH}$ | RD or WR High to ALE High | 0 | 45 | $t_{CLCL}$– 40 | $t_{CLCL}$ + 40 | ns |

**Note: The "Δ" is ? ns**

**Write Operation:**




**Read Operation:**

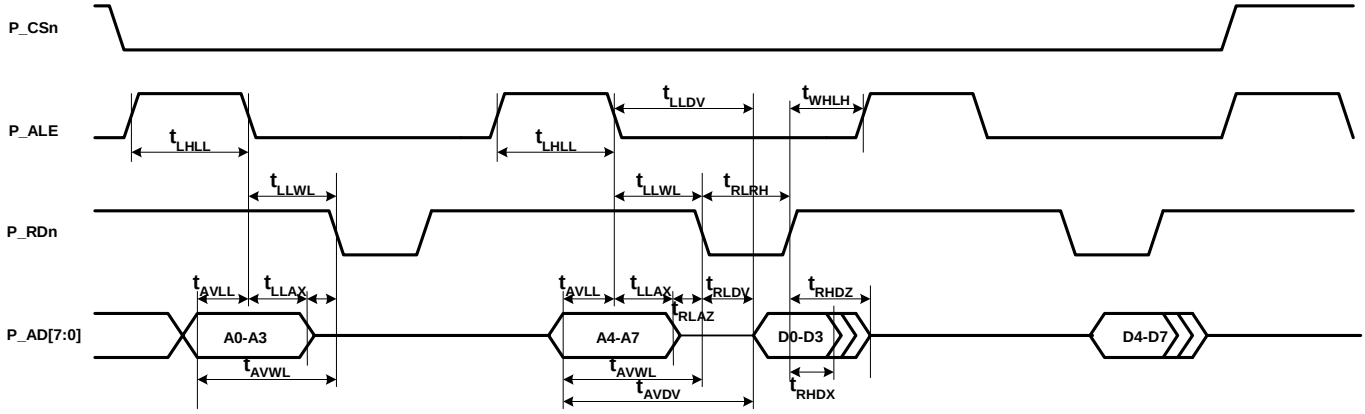



**Figure 7.2-2 Parallel 4-Bit Bus Interface Timing**

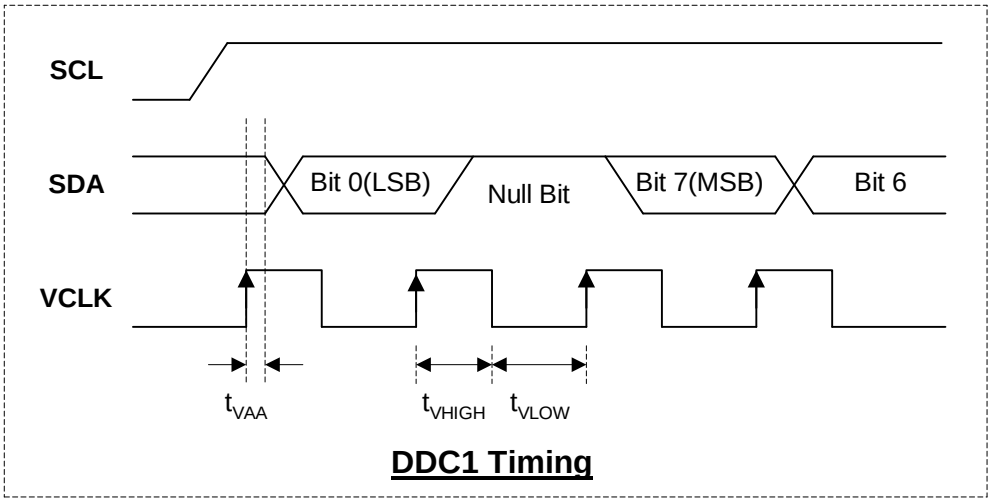
**DDC Bus Timing**

**DDC1 Mode:**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $t_{VAA}$ | Data Valid from the low-to-high edge of the VCLK | - | - | 1000 | ns | |
| $t_{MODE}$ | Time for Transition to DDC2B Mode from DDC1 | - | - | 500 | ns | |

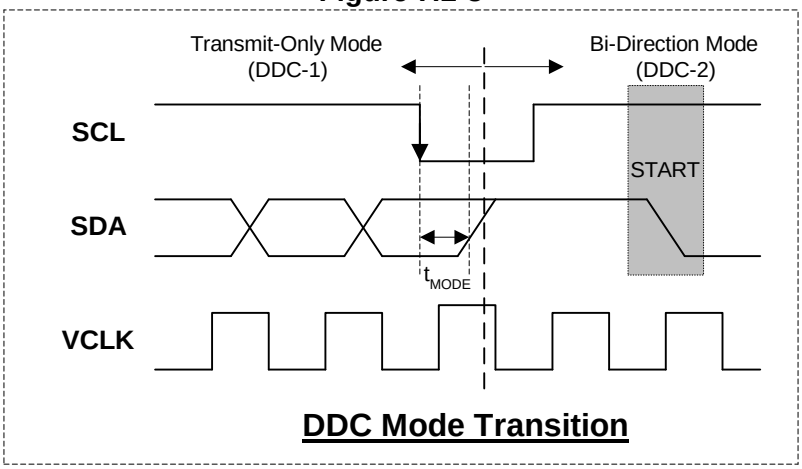
Note:

VCLK comes from Separate VSYNCI or is extracted from Composite Sync. The internal noise filter will cause a filter time delay of the VCLK.




**DDC1 Timing**

**Figure 7.2-3**

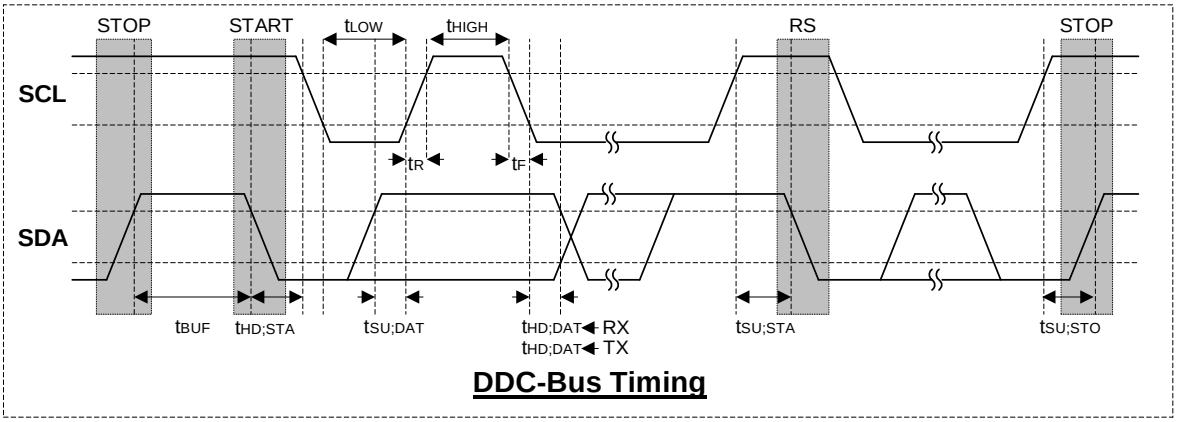



**DDC Mode Transition**

**Figure 7.2-4**

**DDC2B Mode**

| Symbol | Parameter | | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max | Min | Max | |
| $f_{SCL}$ | SCL Clock Frequency | | | 100 | | 400 | KHz |
| $t_{BUF}$ | Bus Free Between a STOP and START Condition | | 4.7 | | 1.3 | | us |
| $t_{HD;STA}$ | Hold Time for START Condition | | 4.0 | | 0.6 | | us |
| $t_{LOW}$ | LOW Period of The SCL Clock | | 4.7 | | 1.3 | | us |
| $t_{HIGH}$ | HIGH Period of The SCL Clock | | 4.0 | | 0.6 | | us |
| $t_{SU;STA}$ | Set-up Time for a Repeated START Condition | | 4.7 | | 0.6 | | us |
| $t_{HD;DAT}$ | Data Hold Time | Transmitter | 0.1 | | 0.1 | 0.9 | us |
| | | Receiver | 0 | | 0 | | |
| $t_{SU;DAT}$ | Data Set-up Time | | 250 | | 100 | | ns |
| $t_r$ | Rise Time of Both SDA and SCL Signals | | | 1000 | | 300 | ns |
| $t_f$ | Fall Time of Both SDA and SCL Signals | | | 300 | | 300 | ns |
| $t_{SU;STO}$ | Set-up Time for STOP Condition | | 4.0 | | 0.6 | | us |
| $t_{SP}$ | Pulse Width of spikes which must be suppressed by the input filter | | 0 | 50 | 0 | 50 | ns |
| $C_I$ | Capacitance for each Bus Pin | | - | 10 | | 10 | pF |
| $C_b$ | Capacitive load for each Bus Line | | - | 400 | | 400 | pF |




**DDC-Bus Timing**

**Figure 7.2-5**

**LVDS Timing**

| Symbol | Parameter | Min. | Typ.* | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $t_{d0}$ | Delay Time, TCLK↓ to Serial Bit Position 0 | -0.4 | | 0.3 | ns | |
| $t_{d1}$ | Delay Time, TCLK↓ to Serial Bit Position 1 | 1.8 | | 2.5 | ns | |
| $t_{d2}$ | Delay Time, TCLK↓ to Serial Bit Position 2 | 4.0 | | 4.7 | ns | |
| $t_{d3}$ | Delay Time, TCLK↓ to Serial Bit Position 3 | 6.2 | | 6.9 | ns | |
| $t_{d4}$ | Delay Time, TCLK↓ to Serial Bit Position 4 | 8.4 | | 9.1 | ns | |
| $t_{d5}$ | Delay Time, TCLK↓ to Serial Bit Position 5 | 10.6 | | 11.3 | ns | $t_c$ = 15.38 ns (± 0.2%), \|Input Clock Jitter\| < 50 ps** See Figure 7.2.6 |
| $t_{d6}$ | Delay Time, TCLK↓ to Serial Bit Position 6 | 12.8 | | 13.5 | ns | |
| $t_{d7}$ | Delay Time, CLKIN↑ or CLKIN ↓ to TCLK↑ | 3.0 | 4.2 | 5.5 | ns | $t_c$ = 15.38 ns (± 0.2%), \|Input Clock Jitter\| < 50 ps ** See Figure 7.2.6 |
| $t_w$ | Pulse Duration, High-Level Output Clock | $0.35t_c$ | $\frac{4}{7}t_c$ | $0.65t_c$ | ns | |
| $t_t$ | Transition Time, Differential Output Voltage ($t_r$ or $t_f$) | 260 | 700 | 1500 | ps | See Figure 7.2.6 |
| $t_{en}$ | Enable Time, $\overline{PWDN}$ ↑ to Phase Lock (TCLK Valid) | | | 10 | ms | See Figure 7.2.7 |
| $t_{dis}$ | Disable Time, $\overline{PWDN}$ ↓ to Off State (TCLK Low) | | | 100 | ns | See Figure 7.2.8 |

* All typical values are at VCC = 3.3V, $T_A$ = 25°C

****** |Input Clock Jitter| is the magnitude of the change in the input clock period.

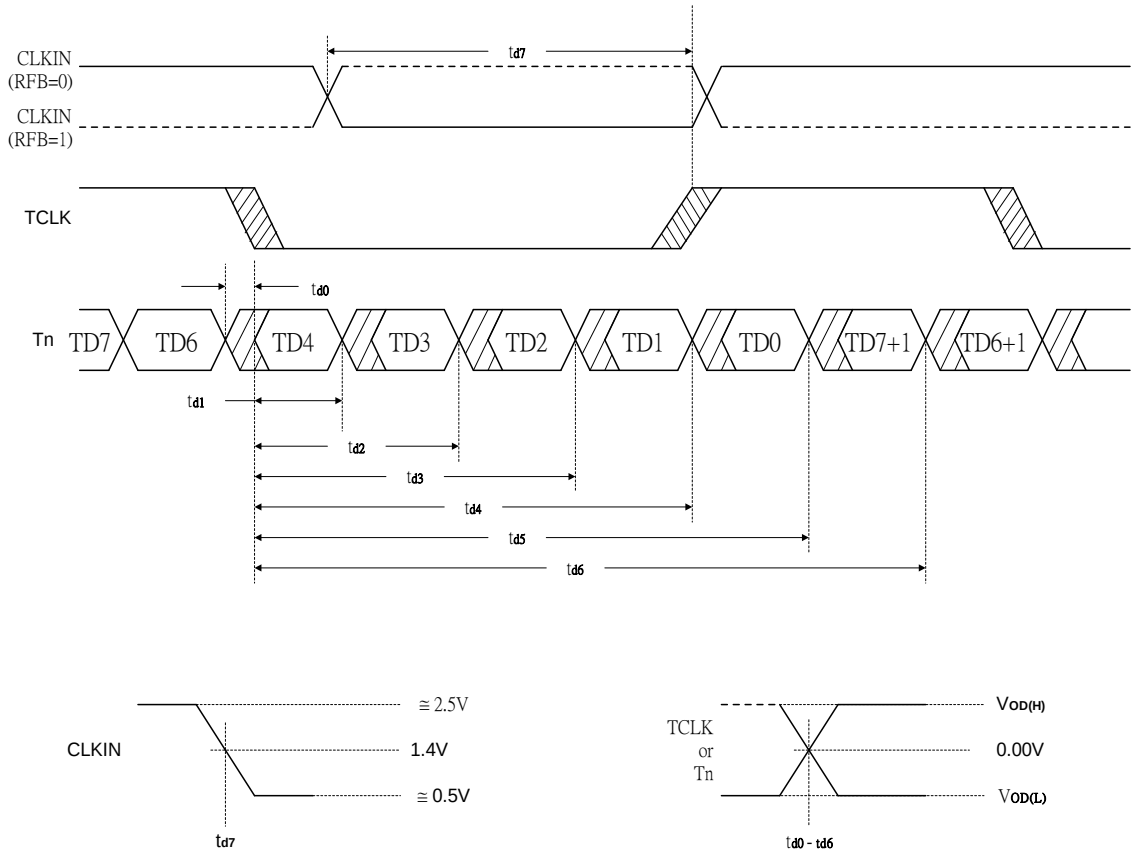



**Figure 7.2-6 LVDS Timing Definitions**

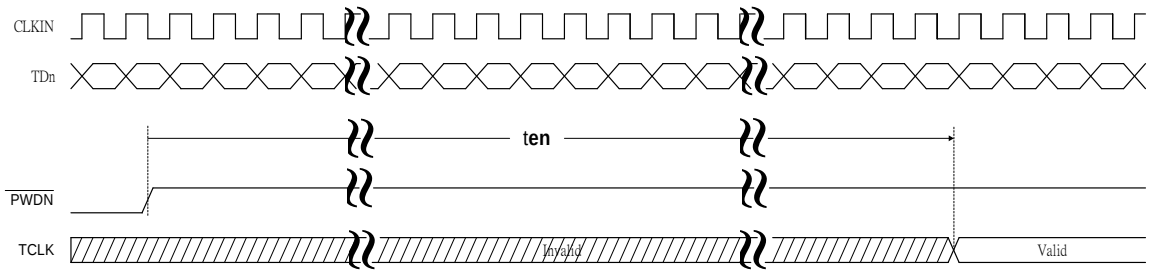



**Figure 7.2-7 LVDS Enable Time Waveforms**

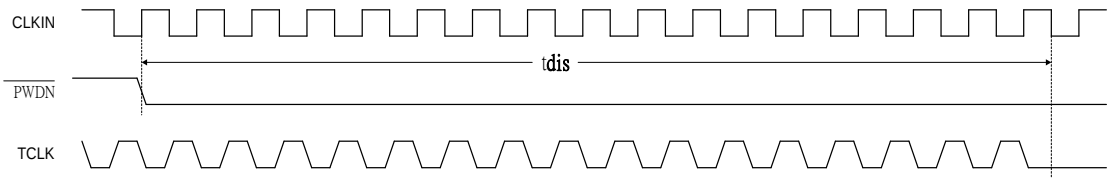



**Figure 7.2-8 LVDS Disable Time Waveforms**

# 8. Application Circuit

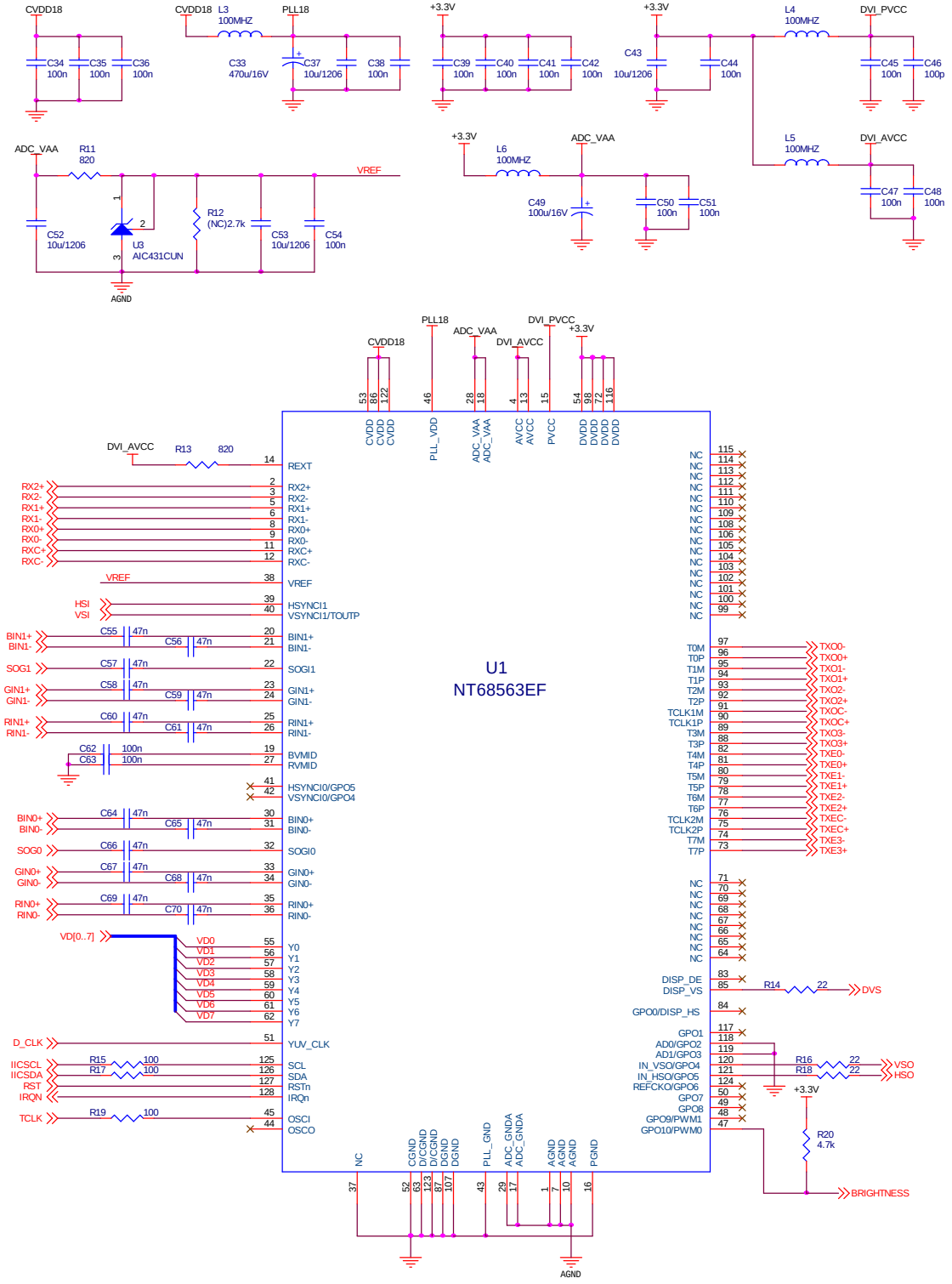



**Figure 8-1 Application Circuit**

# 9. Registers Mapping

| | Block Name | | Byte Offset | Size (bytes) | |
|---|---|---|---|---|---|
| | | | | | |
| | ADC PLL Interface | Page 0 | 0x000 ~ 0x017 | 32 | |
| | DVI Input Control 1 | | 0x018 ~ 0x01E | | |
| | Graphic Port Control | | 0x020 ~ 0x03F | 32 | |
| | Video Port Control | | 0x040 ~ 0x05F | 32 | |
| | Back End Image Processing | | 0x060 ~ 0x064 | 4 | |
| | NR Control | | 0x068 ~ 0x06F | 8 | |
| | GPIO Control | | 0x070 ~ 0x073 | 4 | |
| | PWM Control | | 0x074 ~ 0x077 | 4 | |
| | DDC Control | | 0x078 ~ 0x07D | 6 | |
| | OSD Control | | 0x080 ~ 0x0CF | 80 | |
| | Index Port Access Control | | 0x0E0 ~ 0x0E3 | 4 | |
| | Misc. Access Control | | 0x0E5 ~ 0x0E6 | 2 | |
| | HS Digital PLL | | 0x0D0 ~ 0x0DF<br>0x0E8 ~ 0x0EF | 24 | |
| | Display Digital PLL & SSC | | 0x0F0 ~ 0x0F7 | 8 | |
| | Gauge Control | | 0x0F8 ~ 0x0FD | 5 | |
| | Page Control | | 0x0FF | 1 | |
| | | | | | |
| | Power Control | Page 1 | 0x101 ~ 0x102 | 2 | |
| | Auto Tune | | 0x106 ~ 0x12F | 32 | |
| | Bright Frame Display | | 0x130 ~ 0x13B | | |
| | Display General Control | | 0x150 ~ 0x18F | 48 | |
| | Sync Processor | | 0x196 ~ 0x1B0 | 27 | |
| | sRGB Control | | 0x1D0 ~ 0x1DF | 16 | |
| | Test Mode | | 0x1E0 ~ 0x1FE | 31 | |
| | Page Control | | 0x1FF | 1 | |
| | | | | | |

## 9.1. ADC Interface

| 0x000 | | ADCPLL Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | | Reserved | |
| 6 | | Reserved | |
| 5 | | Reserved | |
| 4 | HPLL_HSYNC_SEL | HPLL Hsync input signal selection<br>0: HSYNCI (pad sync from HSYNCI0 or HSYNCI1)<br>1: SYNC_HS (Internal signal from sync processor) | |
| 3 | HSYNC_SEL | PLL Hsync input signal selection<br>0: HSYNCI (HSYNCI0/HSYNCI1)<br>1: SOGI | |
| 2 | | Reserved | |
| 1 | REG_VREF | ADCPLL reference voltage (2.5V) source select<br>0: External (from VREF pin)<br>1: Internal (from internal regulator) | |
| 0 | | Reserved | |

Default: 1010 0000B

| 0x001 | | Red Channel Gain Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | RGAIN[8:1] | The RAGAIN[7:0] that sets the gain of the R channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing RGAIN results in the picture having less contrast. | |

Default: 1000 0000B

| 0x002 | | ADC test control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-3 | | Reserved | |
| 2-0 | CMCTL[2:0] | | |

Default: 0000 0010B

| 0x003 | | Red Channel DC Shift Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | RCSC [7:0] | Control the R channel DC shift value to compensate the color excursion. Bigger value gives less brightness. | |

Default: 0100 0000B

| 0x004 | | Green Channel Gain Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GGAIN[8:1] | The GAGAIN[7:0] that sets the gain of the G channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing GGAIN results in the picture having less contrast. | |

Default: 1000 0000B

| 0x005 | ADC test control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-5 | | Reserved |
| 4 | CMP2I | |
| 3-0 | GNB[3:0] | |

Default: 0000 0000B

| 0x006 | | Green Channel DC Shift Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GCSC [7:0] | Control the G channel DC shift value to compensate the color excursion. Bigger value gives less brightness. | |

Default: 0100 0000B

| 0x007 | | Blue Channel Gain Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BGAIN[8:1] | The BAGAIN[7:0] that sets the gain of the B channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing BGAIN results in the picture having less contrast. | |

Default: 1000 0000B

| 0x008 | | ADC Channel and MID Clamp Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-4 | | Reserve | |
| 3 | YUV_SEL0 | Input Type Select.<br>0: Analog (RGB)<br>1: Digital (YUV) | |
| 2 | CHANNEL_SEL | Input Mux Control.<br>0: Channel 0<br>1: Channel 1 | |
| 1 | BMID | Blue Clamp Select<br>0: Clamp to ground<br>1: Clamp to midscale | |
| 0 | RMID | Red Clamp Select<br>0: Clamp to ground<br>1: Clamp to midscale | |

Default: XXXX 0000B

| 0x009 | | Blue Channel DC Shift Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BCSC[7:0] | Control the B channel DC shift value to compensate the color excursion. Bigger value gives less brightness. | |

Default: 0100 0000

| 0x00A | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | Reserved | |

Default: XXXX 0110B

| 0x00B | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |

| | | |
|---|---|---|
| 7-0 | | Reserved |

Default: 1001 0111B

| 0x00C | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | Reserved |

Default: 0101 0101B

| 0x00D | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-6 | | Reserved |

Default: 0100 0000B

| 0x00E | ADC PLL Power-up Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | | Reserved |
| 6 | | Reserved |
| 5 | BGAIN[0] | BGAIN bit 0 |
| 4 | GGAIN[0] | GGAIN bit 0 |
| 3 | RGAIN[0] | RGAIN bit 0 |
| 2 | PU_Badc1 | 1= Power-up B channel A2D converter. |
| 1 | PU_Gadc1 | 1= Power-up G channel A2D converter. |
| 0 | PU_Radc1 | 1= Power-up R channel A2D converter. |

Default: 1111 1111B

| 0x00F | ADC Status | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | Reserved |

Default: 0000 0000B

| 0x00F | ADC Status | W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | Reserved |

Default: 0000 0000B

| 0x010 | Analog Bandwidth Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-4 | | Reserved |
| 3 | | |
| 2-1 | ADC_BW [1:0] | Analog bandwidth select<br>11 : 500 MHz<br>10 : 300 MHz<br>01 : 150 MHz<br>00 : 75 MHz |
| 0 | | Reserved |

Default: XXXX X11XB

| 0x011 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | Reserved |

Default: XXXX XXXXB

| 0x012 | SOG Slicer Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-3 | SOG_THR [4:0] | The comparator threshold of the Sync-on-Green Slicer to be adjusted.<br>This register adjust it in steps of 10 mV, with the setting<br>10 mV <= SOG_THR <=330 mV |
| 2 | EN_SOG_SLICER | Enable internal SOG Slicer.<br>0 = Disable<br>1 = Enable |
| 0-1 | | Reserved |

Default: 0111 11XXB

| 0x013 | White Balance Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-2 | | Reserved |
| 1-0 | VREF[1:0] | Select the signal source for VGA input. When VR1 or VR2 is selected, the PLL will go into free-run state.<br>00: VR0. Internal zero voltage.<br>01: VR2. Internal reference voltage 2. (0.35V)<br>10: VR2. Internal reference voltage 2. (0.7V)<br>11: Normal. From external RGB input pin. |

Default: XXXX XX11B

| 0x014 | Hsync Trigger Level Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 6-4 | HS_THR_H | The trigger level threshold of the sync high level to be adjusted.<br>This register adjust it in steps of 100 mV, with the setting<br>1500 mV <= HS_THR_H <=2200 mV |
| 2-0 | HS_THR_L | The trigger level threshold of the sync low level to be adjusted.<br>This register adjust it in steps of 100 mV, with the setting<br>700 mV <= HS_THR _L<=1400 mV |

Default: X000 X000B

| 0x015 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

Default: XXXX XXXXB

## 9.2. DVI Input Control 1

| 0x016 | DVI Clock Detection | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | DVI_CLK | DVI clock detection |

Default: XXXX XXXXB

| 0x017 | DVI Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

Default: XXXX XXXXB

| 0x018 | DVI Control 1 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-6 | DPLL_LOOP_FIT [1:0] | TMDS PLL loop filter control |
| 5 | BSTREAM_CHK | Bit Stream error correction control<br>0 = Disable<br>1 = Enable |
| 4 | FSM_RST | DPLL FSM Disable<br>0 = Enable<br>1 = Disable |
| 3 | SYNC_SEL | Sync is generated from R channel or B channel<br>0 = From B Channel (RX0)<br>1 = From R Channel (RX2) |
| 2 | FORCE_BND_EEC | Force boundary error correction enable |
| 1 | BND_EEC_EN | Adaptive boundary error correction enable |
| 0 | DPLL_ACT | TMDS DPLL working mode selection |

Default: 0000 0000B

| 0x019 | DVI Control 2 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-6 | DVI_DET_CHANNEL [1:0] | Detection channel select<br>00: RX0<br>01: RX1<br>10: TX2<br>11: Reserved |
| 5-4 | DVI_TRIG_SRC [1:0] | Detection trig point select<br>00: V Sync<br>Other: Always trig |
| 3-2 | | Reserved |
| 1 | DPLL_FSM_MOD | DPLL FSM mode select<br>0 = 3 state FSM<br>1 = 5 state FSM |
| 0 | EXT_UDCHK_EN | Extend up/down check enable |

Default: 0000 0000B

| 0x01A | DVI Control 3 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-6 | DVI_DET_LEN [1:0] | DVI detection length<br>00: 32<br>01: 64<br>10: 96<br>11: 128 |
| 5-4 | DVI_DET_TYPE [1:0] | DVI detection type |
| 3 | | Reserved |
| 2 | DVI_DET_SYNC_POL | DVI detection sync polarity invert<br>0 = Normal<br>1 = Inverted |
| 1 | DVI_DET_RDY | DVI detection data ready |

| | | |
|---|---|---|
| | | 0 = No data<br>1 = Ready |
| 0 | DVI_DET_EN | DVI detection data enable |

Default: 0000 0000B

| 0x01B | | DVI Control 4 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DVI_DET_DATA [7:0] | DVI detection data | |

Default: 0000 0000B

| 0x01C | | DVI Control 5 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DVI_CLK_DLY | Control the delay of recovered clock | |

Default: 0000 0000B

| 0x01D | | DVI Control 6 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | DVI_CLK_DLY_EN | Enable the delay of recovered clock | |
| 6-0 | DVI_PLL_BW | Bandwidth control of PLL | |

Default: 0001 1111B

| 0x01E | | DVI Control 7 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DVI_EQ_DATA | Equalizer bias current control | |

Default: 0111 1000B

## 9.3. Pre-Pattern Control

| 0x01F | | Pre-Pattern Control R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | PRE_PATT_EN | Pre-Pattern Enable.<br>0 = Disable<br>1 = Enable |
| 6 | PRE_INV | Pre-Pattern Data invert<br>0 = Normal<br>1 = Invert the RGB Data |
| 5 | PRE_CBAR_EN | Paste a Cross Bar on the built-in Pre-pattern and the Bar's gray level is controlled via CBAR_FG[7:0] register (0x15A)<br>0 = Disable<br>1 = Enable |
| 4 | PRE_PATT_BK | Built-in pre-pattern bank Select<br>0 = Bank 0<br>1 = Bank 1 |
| 3-0 | PRE_PATT_SEL [3:0] | Select built-in pre-pattern type<br>Pattern number = 0~7<br><br>If PRE_PATT_BK = Bank 0<br>0000 = Reserved<br>0001 = Dot Moiré<br>0010 = Vertical Line Moire (1B1W)<br>0011 = Vertical Line Moire (2B1W)<br>0100 = Vertical Line Moire (2B2W)<br>0101 = 256 V_Gray Bar<br>0110 = 256 H_Gray Bar<br>0111 = Horizontal Line Moire (1B1W)<br>1000 = Horizontal Line Moire (2B1W)<br>1001 = Horizontal Line Moire (2B2W)<br>1010 = Chat Pattern<br>1011 = White Pattern<br>11xx = Rectangular pattern, outline width is defined by xx bits.<br>00 = 1 pixel<br>01 = 3 pixels<br>10 = 5 pixels<br>11 = 7 pixels<br><br>If PATT_BK = Bank 1<br>0000 = Black pattern<br>0001~1111 = Reserved |

Default: 0000 0000B

## 9.4. Graphic Port Control

- ADC/TMDS/Digital input source selection
- Clamp pulse
- Interlace decision window
- Mask window
- Capture window

**General Control**

| 0x020 | | Graphic Port Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | GI_VSYNC_EDGE | Select the V sync referenced edge.<br>0 = Leading edge<br>1 = Trailing edge | |
| 6 | GI_IFLD_INV | Invert the internal field reference signal for data merging priority<br>0 = Normal<br>1 = Invert | |
| 5 | GI_MKWIN_EN | Mask Window Enable. When GI_MKWIN_EN =1, GI_HMASK_BEG, GI_HMASK_END, GI_VMASK_BEG and GI_VMASK_END are used to set the window around the HSYNC and VSYNC during which the captured data is 0x000 and auto tune is ignored. This filters out noise occurring on the RGB channels around the HSYNC and VSYNC pulse.<br>0 = Disable<br>1 = Enable | |
| 4 | GI_WRAP_SEL | Wrap around method select.<br>0 = Wrap around<br>1 = Wrap black | |
| 3 | GI_HSYNC_EDGE | Select the H sync referenced edge.<br>0 = Leading edge<br>1 = Trailing edge | |
| 2 | GI_INTE_EN | Interlaced input enable. When GI_INTE_EN =1, the field status is reference to internal field detector.<br>0 = Non-interlaced<br>1 = Interlaced | |
| 1 | GI_SRC_SEL | Graphic input source select<br>0 = ADC<br>1 = TMDS/Digital | |
| 0 | GI_CAP_EN | Graphic input capture enable<br>0 = Disable<br>1 = Enable | |

Default: 0000 0000B

| 0x021 | | Clamp Pulse Begin | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | CLAMP_EDG | Clamp Pulse Reference Edge<br>0 = GHS rising edge<br>1 = GHS falling edge | |
| 6 | CLAMP_POL | Clamp Pulse Polarity.<br>0 = Active Low<br>1 = Active High | |
| 5-0 | CLAMP_BEG [5:0] | Clamp Pulse Begin. (Unit 4xCLP_REFCLK)<br>CLAMP_BEG =5, means waiting 5 x 4CLP_REFCLK after GHS edge to begin the pulse. | |

Default: 0000 0000B

| 0x022 | | Clamp Pulse Width | R/W |
|---|---|---|---|
| Bits | Name | Description | |

| | | |
|---|---|---|
| 7 | CLAMP_EN | Clamp Pulse Enable<br>0 = Disable<br>1 = Enable |
| 6 | CLP_CLK_SEL | Clamp Pulse Reference clock (CLP_REFCLK = Capture Clock) Select<br>0 = CLP_REFCLK<br>1 = 2 x CLP_REFCLK |
| 5-0 | CLAMP_WID [5:0] | Clamp Pulse Width.(unit 4xCLP_REFCLK)<br>CLAMP_WID =5, means pulse width being 6 x 4CLP_REFCLK wide. |

Default: 0000 1111B

| **0x023** | | **Digital Port Input Control** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | YPbPr_EN | YPbPr Input Enable | |
| 6 | CLAMP_SOURCE | Clamp source select.<br>0 = selects Row Hs to be used for clamping.<br>1 = selects Sync Separated Hsync to be used for clamping. | |
| 5 | HS_DEJITTER_EN | For TMDS input mode, This bit enables/disable the HSYNC De-jitter function.<br>0 = Disable<br>1 = Enable | |
| 4 | DEJITTER_RST | For TMDS input mode, De-jitter reset<br>0 = Normal<br>1 = Reset | |
| 3 | HCAP_DE_EN | For TMDS input mode, active data is enclosed by DE signal. Hardware can automatically capture the first data and bypass the setting of capture begin registers (0x034~0x035). This bit is effective if DVI_SYNC_SEL=1 (0x192 bit 7).<br>0 = According to horizontal capture registers<br>1 = According to DE signal | |
| 2-1 | | | |
| 0 | | | |

Default: 0000 0000B

| **0x024** | | **ADCLK Delay Control** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | Reserved | |
| 3-0 | | Reserved | |

Default: 0000 0000B

| **0x025** | | **ADCLK Delay & Invert Control** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 6 | CLKI_INV | Internal data latch clock invert<br>0 = Normal<br>1 = Invert | |
| 5 | | Reserved | |
| 4 | | Reserved | |
| 3-0 | CLKI_DLY | Internal data latch clock delay (0.5nS/step)<br>0~15 step | |

Default: X000 0000B

| 0x026 | | Data Delay & Swap Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | CLAMP_MASK_EN | Clamping pulse mask enable | |
| 6 | | Reserved | |
| 5 | CAP_RB_SWAP | Capture R/B channel swap<br>0 = Normal<br>1 = Swap | |
| 4 | | Reserved | |
| 3 | | Reserved | |
| 2 | CAP_BIT_SWAP | Capture data bit swap D7-D0 -> D0-D7<br>0 = Normal<br>1 = Swap | |
| 1 | | Reserved | |
| 0 | CAP_DATA_DLY | Capture data delay<br>0 = Normal<br>1 = Delay 1 ADCLK | |

Default: 0000 0000B

| 0x027 | | Vsync and DE Delay | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 6-4 | GI_DEDLY [2:0] | Delay the graphic port internal DE pulse by input pixel clock to avoid the unmatched data phase<br>-4~+3 pixel clocks delay | |
| 3-0 | GI_VSDLY [3:0] | Delay the graphic port VSYNC pulse by input pixel clock to avoid the confusion of 1st HSYNC recognized following VSYNC leading edge.<br>0~15 pixel clocks delay | |

Default: X011 0001B

| 0x028 | | Hsync edge detection control 1 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-6 | | Reserved | |
| 5-4 | | Reserved | |
| 3-2 | | Reserved | |
| 1 | | Reserved | |
| 0 | | Reserved | |

Default: 0000 0000B

| 0x029 | | Hsync edge detection control 2 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | | Reserved | |
| 6 | | Reserved | |
| 5-4 | | Reserved | |
| 3 | | Reserved | |
| 2 | | Reserved | |
| 1-0 | | Reserved | |

Default: 0000 0000B

**Mask Window Define**

| 0x02A | Horizontal Mask Window Begin | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GI_HMASK_BEG [7:0] | Horizontal Mask Window Begin. When GI_MKWIN_EN =1, this register sets the number of clocks after the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune starts outside this window. |

Default: 0000 0000B

| 0x02B | Horizontal Mask Window End | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GI_HMASK_END [7:0] | Horizontal Mask Window End. When GI_MKWIN_EN =1, this register sets the number of clocks before the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune stops. |

Default: 0000 0000B

| 0x02C | Vertical Mask Window Begin | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GI_VMASK_BEG [7:0] | Vertical Mask Window Begin. When GI_MKWIN_EN =1, this register sets the number of lines after the referenced edge of the VSYNC pulse in which the captured data is '0x00' and auto-tune starts outside this window. |

Default: 0000 0000B

| 0x02D | Vertical Mask Window End | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GI_VMASK_END [7:0] | Vertical Mask Window End. When GI_MKWIN_EN =1, this register sets the number of lines before the referenced edge of the VSYNC pulse in which the captured data is '0x00' and the auto-tune stops. |

Default: 0000 0000B

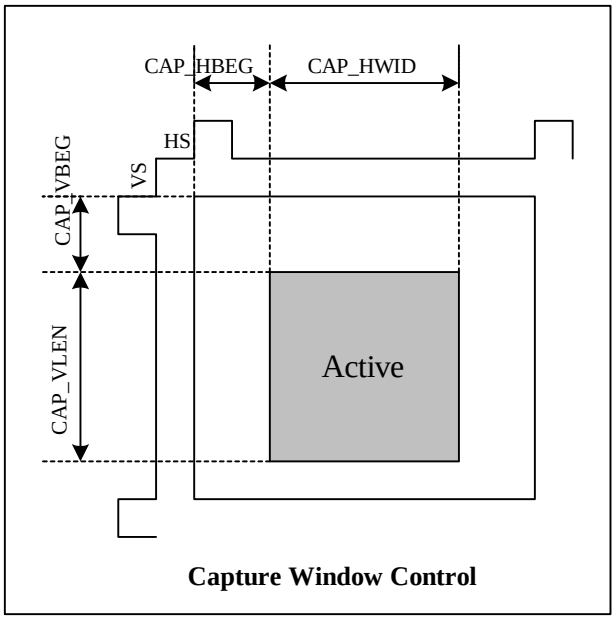



**Figure 9.4-1**

**Capture Window Control**

| 0x02E | Capture Vertical Begin for Odd Field -lo | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GI_CAP_VBEGO [7:0] | Vertical Capture Begin for Odd Field. GI_CAP_VBEGO indicates how many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGO =3, means waiting 3 lines to begin capture. This register is double-buffered. |

Default: 0000 0000B

| **0x02F** | **Capture Vertical Begin for Odd Field -hi** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 2-0 | GI_CAP_VBEGO [10:8] | MSB of GI_CAP_VBEGO. This register is double-buffered. |

Default: XXXX X000B

| **0x030** | **Capture Vertical Begin for Even Field -lo** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-0 | GI_CAP_VBEGE [7:0] | Vertical Capture Begin for Even Field. GI_CAP_VBEGE indicates how many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGE =3, means waiting 3 lines to begin capture. This register is double-buffered. |

Default: 0000 0000B

| **0x031** | **Capture Vertical Begin for Even Field -hi** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 2-0 | GI_CAP_VBEGE [10:8] | MSB of GI_CAP_VBEGE. This register is double-buffered. |

Default: XXXX X000B

| **0x032** | **Capture Vertical Length -lo** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-0 | GI_CAP_VLEN [7:0] | Vertical Capture Length. GI_CAP_VLEN indicates how many lines to capture. GI_CAP_VLEN = 3, means capturing 3 lines. This register is double-buffered. |

Default: 0000 0000B

| **0x033** | **Capture Vertical Length –hi** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 2-0 | GI_CAP_VLEN [10:8] | MSB of GI_CAP_VLEN. This register is double-buffered. |

Default: XXXX X000B

| **0x034** | **Capture Horizontal Begin –lo** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-0 | GI_CAP_HBEG [7:0] | Horizontal Capture Begin. GH_CAP_HBEG indicates how many pixels to wait after referenced edge of HSYNC before starting image capture. GH_CAP_HBEG =3, means waiting 3 pixels to begin capture. This register is double-buffered. |

Default: 0000 0000B

| **0x035** | **Capture Horizontal Begin –hi** | **R/W** |
|---|---|---|
| Bits | Name | Description |

| | | |
|---|---|---|
| 3-0 | GI_CAP_HBEG [11:8] | MSB of GI_CAP_HBEG.<br>This register is double-buffered. |

Default: XXXX 0000B

| 0x036 | | Capture Horizontal Width –lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_CAP_HWID [7:0] | Horizontal Capture Width. GI_CAP_HWID indicates how many pixels to capture. GI_CAP_HWID = 3, means capturing 3 pixels.<br>This register is double-buffered. | |

Default: 0000 0000B

| 0x037 | | Capture Horizontal Width –hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | GI_CAP_HWID [11:8] | MSB of GI_CAP_HWID.<br>This register is double-buffered. | |

Default: XXXX 0000B

| 0x038 | | Alternate sampling control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3 | DE_MK_EN | For TMDS mask DE Mode enable | |
| 2 | CLK_MK_EN | Capture clock mask enable | |
| 1 | GI_ALT_INV | The alternate sampling reference frame signal polarity control<br>0 = Active Low<br>1 =Active High | |
| 0 | GI_ALT_EN | Input alternate sampling enable. This bit should be enabled for input graphic pixel rate lager than SXGA@75Hz, .<br>0 = Disable<br>1 = Enable | |

Default: XXXX XX00B

| 0x039 | | Clock mask window control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | CLK_MASK_WID | Clock mask width. When CLK_MK_EN =1, this register sets the number of clocks after the internal de signal. Unit: 2 ADC sample clock | |

| 0x03A~0x03B | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: XXXX XXXXB

| 0x03C | | DVI Input Horizontal Active Width-lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DVI_CAP_HWID [7:0] | The active window horizontal width. The value is valid only for DVI interface is enabled and the SYNC input source is from DVI DE signal | |

Default: 0000 0000B

| 0x03D | | DVI Input Horizontal Active Width-hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | DVI_CAP_HWID | MSB of DVI_CAP_HWID | |

| | | |
|---|---|---|
| | [11:8] | |

Default: XXXX 0000B

| 0x03E | | DVI Input Vertical Active Length-lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DVI_CAP_VLEN [7:0] | The active window vertical length. The value is valid only for DVI interface is enabled and the SYNC input source is from DVI DE signal | |

Default: 0000 0000B

| 0x03F | | DVI Input Vertical Active Length-hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | DVI_CAP_VLEN [10:8] | MSB of DVI_CAP_VLEN | |

Default: XXXX X000B

## 9.5. Video Port Control

**General Control**

| 0x040 | Video Port Control 1 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | | Reserved |
| 6:5 | VI_BT656_EN | When Video port is active, select between 8-bit wide or 16-bit wide data capture.<br>00 = Reserved<br>01 = Reserved<br>1X = 8-bit wide BT656 processing from Video Port (YUV0 / YUV1) |
| 4 | UV_SWAP | Swap the order of received UV data.<br>0 = Normal<br>1 = Swap |
| 3 | YUV_PORT_SEL | YUV input port selection.<br>0 = YUV0 (Located from Pin55~62)<br>1 = YUV1 (Located from Pin30~37) |
| 2 | EXFLD_EN | Select field indicator source. When VI_INTE_EN =1, this bit is in effect.<br>0 = From internal field detector<br>1 = From external EX_FIELD pin |
| 1 | VI_INTE_EN | Interlaced input enable. When VI_INTE_EN =1, the field status is reference to internal field detector or external EXFLD input signal.<br>0 = Non-interlaced<br>1 = Interlaced |
| 0 | VI_CAP_EN | Input capture enable<br>0 = Disabled<br>1 = Enabled |

Default: X000 0000B

| 0x041 | Video Port Control 2 | R/W |
|---|---|---|
| Bits | Name | Description |
| 5 | VI_CAP_656_AUTO | For BT656 mode, when VI_CAP_656_AUTO = “1”. Hardware referee to the setting of capture registers to capture the active data<br>0 = Disable<br>1 = Enable |
| 4 | VI_MKWIN_EN | Mask Window Enable. When GI_MKWIN_EN =1, GI_HMASK_BEG, GI_HMASK_END, GI_VMASK_BEG and GI_VMASK_END are used to set the window around the HSYNC and VSYNC during which the captured data is 0x00 and auto tune is disabled. This filters out noise occurring on the RGB channels around the HSYNC and VSYNC pulse.<br>0 = Disable<br>1 = Enable |
| 3 | VI_WRAP_SEL | Wrap around method select<br>0 = Wrap around<br>1 = Wrap black |
| 2 | VI_SYNC_EDGE | Select the H/V sync reference edge.<br>0 = Leading edge<br>1 = Trailing edge |
| 1 | VCAP_656_EN | For BT656 mode, active data is enclosed by SAV/EAV code. Hardware can automatically capture the active data and bypass the setting of capture |

| | | |
|---|---|---|
| | | registers except the Horizontal Capture Width.<br>0 = According to vertical capture registers<br>1 = According to SAV/EAV code |
| 0 | HCAP_656_EN | For BT656 mode, active data is enclosed by SAV/EAV code. Hardware can automatically capture the active data and bypass the setting of capture registers except the Horizontal Capture Width.<br>0 = According to horizontal capture registers<br>1 = According to SAV/EAV code |

Default: XX00 0000B

| **0x042** | **Polarity Control** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 5 | VI_656CLK_INV | Invert the polarity of CLK for internal BT656 data processing unit<br>0 = Normal<br>1 = Invert |
| 4 | VI_IFLD_INV | Invert the internal field reference signal for data merging priority<br>0 = Normal<br>1 = Invert |
| 3 | VI_601CLK_INV | Invert the polarity of CLK for internal ITU601 data processing unit<br>0 = Normal<br>1 = Invert |
| 2 | | Reserved |
| 1 | | Reserved |
| 0 | | Reserved |

Default: XX00 0X00B

| **0x043** | **VSYNC Delay** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 3-0 | VI_VSDLY [3:0] | Delay the video port VSYNC pulse by input pixel clock to avoid the confusion of 1st HSYNC recognized following VSYNC trailing edge.<br>0~15 pixels delay |

Default: XXXX 0001B

**Mask Window Define**

| **0x047** | **Horizontal Mask Window Begin** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-0 | VI_HMASK_BEG [7:0] | Horizontal Mask Window Begin. When VI_MKWIN_EN =1, this register sets the number of clocks after the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune starts outside this window. |

Default: 0000 0000B

| **0x048** | **Horizontal Mask Window End** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-0 | VI_HMASK_END [7:0] | Horizontal Mask Window End. When VI_MKWIN_EN =1, this register sets the number of clocks before the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune stops. |

Default: 0000 0000B

| **0x049** | **Vertical Mask Window Begin** | **R/W** |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | VI_VMASK_BEG [7:0] | Vertical Mask Window Begin. When VI_MKWIN_EN =1, this register sets the number of lines after the referenced edge of the VSYNC pulse in which the captured data is '0x00' and auto-tune starts outside this window. |

Default: 0000 0000B

| 0x04A | Vertical Mask Window End | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | VI_VMASK_END [7:0] | Vertical Mask Window End. When VI_MKWIN_EN =1, this register sets the number of lines before the referenced edge of the VSYNC pulse in which the captured data is '0x00' and the auto-tune stops. |

Default: 0000 0000B

## 9.6. Color space conversion Control

**Color Transfer Equation**

$R = Y_{601} + COEFA*(Cr-128)/512$
$G = Y_{601} – COEFB*(Cr-128)/-512 – COEFC*(Cb-128)/-512$
$B = Y_{601} + COEFD*(Cb-128)/-512$

**SDTV**

$R = Y_{601} + 1.371(Cr-128)$
$G = Y_{601} – 0.698(Cr-128) – 0.336(Cb-128)$
$B = Y_{601} + 1.732(Cb-128)$

**HDTV**

$R = Y_{709} + 1.540(Cr-128)$
$G = Y_{709} – 0.459(Cr-128) – 0.183(Cb-128)$
$B = Y_{709} + 1.816(Cb-128)$

**Color Transfer Coefficient**

| 0x04B | Color Transfer Coefficient A -lo | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | COEFA [7:0] | Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023 |

Default: 1011 1110B

| 0x04C | Color Transfer Coefficient A -hi | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 1-0 | COEFA [9:8] | MSB of COEFA |

Default: XXXX XX10B

| 0x04D | Color Transfer Coefficient B -lo | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | COEFB [7:0] | Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023 |

Default: 0110 0101B

| 0x04E | Color Transfer Coefficient B -hi | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 1-0 | COEFB [9:8] | MSB of COEFB |

Default: XXXX XX01B

| 0x04F | | Color Transfer Coefficient C -lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | COEFC [7:0] | Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023 | |

Default: 1010 1100B

| 0x050 | | Color Transfer Coefficient C -hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 1-0 | COEFC [9:8] | MSB of COEFC | |

Default: XXXX XX00B

| 0x051 | | Color Transfer Coefficient D -lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | COEFD [7:0] | Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023 | |

Default: 0111 0111B

| 0x052 | | Color Transfer Coefficient D -hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 1-0 | COEFD [9:8] | MSB of COEFD | |

Default: XXXX XX11B

## 9.7. Video Port Capture Control

**Capture Window Control**

| 0x053 | | Vertical Capture Begin for Odd Field -lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_CAP_VBEGO [7:0] | ODD Field Vertical Capture Begin. VI_CAP_VBEGO indicates how many lines to wait after referenced edge of VSYNC before starting image capture. VI_CAP_VBEGO =3, means waiting 3 lines to begin capture. **This register is double-buffered.** | |

Default: 0000 0000B

| 0x054 | | Vertical Capture Begin for Odd Field -hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | VI_CAP_VBEGO [10:8] | MSB of VI_CAP_BEG. **This register is double-buffered.** | |

Default: XXXX X000B

| 0x055 | | Vertical Capture Begin for Even Field -lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_CAP_VBEGE [7:0] | Even Field Vertical Capture Begin. VI_CAP_VBEGE indicates how many lines to wait after referenced edge of VSYNC before starting image | |

| | | |
|---|---|---|
| | | capture. VI_CAP_VBEGE =3, means waiting 3 lines to begin capture.<br>**This register is double-buffered.** |

Default: 0000 0000B

| 0x056 | Vertical Capture Begin for Even Field -hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 2-0 | VI_CAP_VBEGE [10:8] | MSB of VI_CAP_VBEGE.<br>**This register is double-buffered.** |

Default: XXXX X000B

| 0x057 | Vertical Capture Length -lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | VI_CAP_VLEN [7:0] | Vertical Capture Length. VI_CAP_VLEN indicates how many lines to capture. VI_CAP_VLEN =3, means capturing 3 lines.<br>**This register is double-buffered.** |

Default: 0000 0000B

| 0x058 | Vertical Capture Length -hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 2-0 | VI_CAP_VLEN [10:8] | MSB of VI_CAP_VLEN.<br>**This register is double-buffered.** |

Default: XXXX X000B

| 0x059 | Horizontal Capture Begin -lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | VI_CAP_HBEG [7:0] | Horizontal Capture Begin. VI_CAP_HBEG indicates how many pixels to wait after referenced edge of HSYNC before starting image capture. VI_CAP_HBEG =3, means waiting 3 pixels to begin capture.<br>**This register is double-buffered.** |

Default: 0000 0000B

| 0x05A | Horizontal Capture Begin -hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 3-0 | VI_CAP_HBEG [11:8] | MSB of VI_CAP_HBEG.<br>**This register is double-buffered.** |

Default: XXXX 0000B

| 0x05B | Horizontal Capture Width -lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | VI_CAP_HWID [7:0] | Horizontal Capture Width. VI_CAP_HWID indicates how many pixels to capture. VI_CAP_HWID = 3, means capturing 3 pixels.<br>**This register is double-buffered.** |

Default: 0000 0000B

| 0x05C | Horizontal Capture Width -hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 3-0 | VI_CAP_HWID [11:8] | MSB of VI_CAP_HWID<br>**This register is double-buffered.** |

Default: XXXX 0000B

| 0x05D~0x05F | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: XXXX XXXX B

## 9.8. Back End Image Processing

- Back-end offset control
- Back-end gain control
- Back-end sharpness and smooth control

| 0x060 | | Back-end Horizontal Sharpness | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | | Reserved | |
| 6 | BK_H_ASRP | Graphic horizontal adaptive sharpness adjusting.<br>0 = Disable<br>1 = Enable | |
| 5 | | HPLL test control | |
| 4 | BK_H_SRPSMO | Graphic horizontal back-end smooth and sharpness select.<br>0 = sharpness<br>1 = smooth | |
| 3-0 | BK_H_SRP [3:0] | Graphic horizontal back-end sharpness/smooth adjusting.<br>16 steps | |

Default: XX00 0000B

| 0x061 | | Color Channel Select | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3 | GAIN_DITH_EN | Gain dithering enable | |
| 2 | GAIN_DITH_MODE | Gain dithering mode<br>0 = Static dithering<br>1 = Random dithering | |
| 1-0 | BK_CH_SEL [1:0] | Select color channel for offset and gain adjusting.<br>00 = R/G/B<br>01 = R<br>10 = G<br>11 = B | |

Default: XXXX 0000B

| 0x062 | | Back-end Offset | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BK_OFFSET [7:0] | Back-end offset adjusting.<br>-128~127 in 2's complement<br>Display color = (Original value * GAIN) +OFFSET | |

Default: 0000 0000B

| 0x063 | | Back-end Gain | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BK_GAIN [7:0] | Back-end gains adjusting.<br>0/128~255/128 | |

Default: 1000 0000B

| 0x064 | Interpolation Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-5 | TEXT_EN [2:0] | Select the Text Mode type<br>000 = Normal Mode<br>001 = Level 1 Text Mode<br>010 = Level 2 Text Mode<br>011 = Level 3 Text Mode<br>1xx = Reserved |
| 4-3 | V_INTE_TYPE [1:0] | Select the Vertical interpolation type<br>00 = DSP (2-pixel)<br>01 = Bi-linear (2-pixel)<br>10 = Duplicate (2-pixel)<br>11 = Reserved |
| 2-0 | H_INTE_TYPE [2:0] | Select the Horizontal interpolation type<br>000 = Advanced DSP (4-pixel)<br>001 = Bi-linear (2-pixel)<br>010 = Duplicate (2-pixel)<br>011 = DSP (2-pixel)<br>100 = DSP (4-pixel)<br>101, 110, 111 = Reserved |

Default: 0000 0000B

| 0x065 | Gamma Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | GAMMA_EN | Gamma Table Enable, When GAMMA_EN = 1, the Gamma Table can't read or write by host interface. When GAMMA_EN = 0 the display is bypass the Gamma table.<br>0 = Disable<br>1 = Enable |
| 6 | TBL_8_10B_SEL | Used 8 bit gamma table or 10 bit gamma table for read/write<br>0 = 10 Bit Access<br>1 = 8 Bit Access |

Default: 00XX XXXXB

| 0x066 | Back-end Vertical Sharpness | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-3 | | Reserved |
| 2-0 | BK_V_SRP [2:0] | Graphic vertical back-end sharpness adjusting.<br>8 steps |

Default: XXXX X000B

| 0x067 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

Default: XXXX XXXXB

## 9.9. Noise Reduction Filter Control

| 0x068 | Noise Reduction Filter Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | | Reserved |
| 6 | NR2_EN | Second Noise Reduction enable<br>0 = Disable<br>1 = Enable |
| 5 | NR_ROUND | Noise Reduction round calculation enable<br>0 = Disable<br>1 = Enable |
| 4 | NR_EDGE_DET | Noise Reduction edge detection enable<br>0 = Disable<br>1 = Enable |
| 3 | | Reserved |
| 2-0 | NR_TYPE | Select the Noise Reduction Filter type<br>000 = Normal Mode (NR disable)<br>001 = Mode 1<br>010 = Mode 2<br>011 = Mode 3<br>1xx = Reserved |

Default: XX00 0000B

| 0x069 | Noise Reduction threshold | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-4 | NR_EDGE_THR [3:0] | Edge Threshold of the noise reduction filter adjusting. |
| 3-0 | NR_THR [3:0] | Threshold of the noise reduction filter adjusting. |

Default: 0000 0000B

| 0x06A | Jitter Correction Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-6 | JC_MAX_TYPE | Jitter Correction max type selection<br>00 = 1 frame<br>01 = 2 frame<br>10 = 4 frame<br>11 = Adaptive mode |
| 5 | | Reserved |
| 4 | JC_EN | Jitter Correction Enable<br>0 = Disable<br>1 = Enable |
| 3-0 | JC_LEVEL [3:0] | Jitter Correction Level |

Default: 0000 0001B

| 0x06B | Seconded Noise Reduction threshold | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-4 | | Reserved |

| | | |
|---|---|---|
| 3-0 | NR2_THR [3:0] | Threshold of the seconded noise reduction filter adjusting. |

Default: 0000 0000B

| 0x06C | Reserved | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

Default: 0000 0000B

| 0x06D | Reserved | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

Default: 0000 0000B

| 0x06E | Reserved | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

Default: 0000 0000B

| 0x06F | Reserved | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

Default: 0000 0000B

## 9.10. General Purpose Input Output (GPIO)

| 0x070 | GPIO Port Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 5 | PWM1_EN | PWM1 output enable (open-drain)<br>0 = Disable<br>1 = PWM1 Enable |
| 4 | PWM0_EN | PWM0 output enable (open-drain)<br>0 = Disable<br>1 = PWM0 Enable |
| 3 | VSO_EN | VSYNC output enable (push-pull)<br>0 = Disable<br>1 = VSYNCO Enable |
| 2 | HSO_EN | HSYNC output enable (push-pull)<br>0 = Disable<br>1 = HSYNCO Enable |

Default: XX00 00XXB

| 0x071 | GPIO Output / Input Data | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 5 | | |
| 4 | | |
| 3 | | |
| 2 | | |
| 1 | | |
| 0 | | |

Default: XX00 0000B

| 0x072 | | Bypass Sync Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 4 | BP_HSYNC_EN | This bit is used to Bypass the Hsync from pin to INT_HSO<br>0 = Disable<br>1 = Enable | |
| 3 | | Reserved | |
| 2 | REFCKO_EN | Reference clock output enable<br>0 = Disable<br>1 = Enable | |
| 1 | BP_HSYNC_SEL | When BP_SYNC_EN = "1", this bit is used to select the output source.<br>0 = From the internal normal Hsync (RAW_HS)<br>1 = From the internal SOG Sync (SOG_HS) | |
| 0 | BP_VSYNC_EN | This bit is used to Bypass the sync from pin to INT_VSO<br>0 = Disable<br>1 = Enable | |

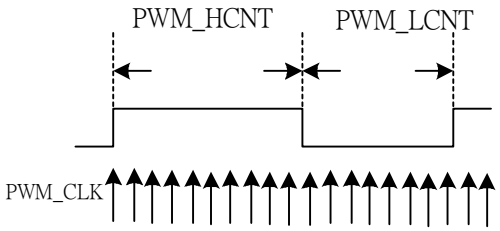
Default: XXXX 0100B

| 0x073 | | GPIO Data Direction | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 5 | | | |
| 4 | | | |
| 3 | | | |
| 2 | | | |
| 1 | | | |
| 0 | | | |

Default: XX00 0000B

## 9.11. PWM Output

- Frequency programmable
- Duty cycle programmable




**When clock source select from reference clock**

$$F_{PWM\_CLK} = F_{REFCLK} / (PWM\_DIV\ 1 \times PWM\_DIV\ 2)$$

**When clock source select from Display Hsync**

$$F_{PWM\_CLK} = F_{DISP\_HS} / (PWM\_DIV\ 1 \times PWM\_DIV\ 2)$$

$$F_{PWM} = \frac{F_{PWM\_CLK}}{(PWM\_HCNT + PWM\_LCNT)}$$

$$Duty = \frac{PWM\_HCNT}{(PWM\_HCNT + PWM\_LCNT)}$$

$$PWM\_HCNT = \frac{Duty \times F_{PWM\_CLK}}{F_{PWM}}$$

$$PWM\_LCNT = \frac{(1 - Duty) \times F_{PWM\_CLK}}{F_{PWM}}$$

| PWM_HCNT | PWM_LCNT | PWM Output |
|---|---|---|
| 0 | 0 | Tri-state |
| 0 | 1~255 | DC '0' |
| 1~255 | 0 | DC '1' |
| 1~255 | 1~255 | PWM pulse |

| 0x074 | | PWM0 Low Period Counter | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | PWM0_LCNT [7:0] | PWM0 pulse low period counter value. Double-buffered. | |

Default: 0000 0000B

| 0x075 | | PWM0 High Period Counter | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | PWM0_HCNT [7:0] | PWM0 pulse high period counter value. Double-buffered. | |

Default: 0000 0000B

| 0x076 | | PWM1 Low Period Counter | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | PWM1_LCNT [7:0] | PWM1 pulse low period counter value. Double-buffered. | |

Default: 0000 0000B

| 0x077 | | PWM1 High Period Counter | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | PWM1_HCNT [7:0] | PWM1 pulse high period counter value. Double-buffered. | |

Default: 0000 0000B

## 9.12. DDC Port Control

- Dual independent input DDC channel
- Pure hardware solution for VESA DDC1/2B
- Selectable 128/256 Bytes EDID-Buffer for hardware DDC port

This block is a 128/256-byte selectable dual-mode DDC port. It is designed for use in applications requiring serial transmission of configuration and control information. Two modes of operation have been implemented

- **Transmit Only Mode for DDC1**
- **Bi-directional Mode for DDC2B**

| **0x078** | | **DDC0 Port Control** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | DDC_EN | DDC0 enable control<br>0 = Disable<br>1 = Enable | |
| 6 | WPT_DDC | DDC0 RAM write-Protect Mode<br>0 = DDC0 RAM-Buffer is R/W Mode<br>1 = DDC0 RAM-Buffer is read only under Write-Protect Mode | |
| 5 | LEN_EDID | DDC0 EDID Data length<br>0 = 128 Bytes<br>1 = 256 Bytes | |
| 4 | MODE_DDC | DDC0 Mode control<br>0 = DDC1<br>H/W ➔ a default state after system reset<br>S/W ➔ clear this bit by S/W to force into DDC1 mode<br>1 = DDC2<br>H/W ➔ automatically set this bit when SCL go-low pulse is detected<br>S/W ➔ set by S/W to force into DDC2B mode | |
| 3 | EN_BACK | Enable Bit for automatically switching back to DDC1 mode if VCLK>128<br>0 = Disable<br>1 = Enable | |
| 2 | INVT_VCLK | The VCLK invert control bit for DDC1 communication<br>0 = the polarity of the VCLK is the same as the of the VSYNC<br>1 = the polarity of the VCLK is inverted with the one of the VSYNC | |
| 1 | CLR_PTR | Clear the contents of Address Pointer of the DDC RAM-Buffer<br>0 = No effect<br>1 = Clear it once after writing an 1 into this bit | |
| 0 | UPD_DDC (R)/ | RAM-Buffer contents updated flag (set by H/W)<br>0 = Not Updated<br>1 = Updated | |
| | CLR_UPD (W) | Clear bit of the UPD_DDC bit<br>0 = No effect<br>1 = Clear the UPD_DDC flag | |

Default: 0100 1000B

| **0x079** | | **DDC0 Port Slave Address Control** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | ADDR_B7 | Slave Address Bit-3~1 of the DDC0-Port<br>➔These 3 lower order bits of the 7-bit slave address can be masked to compare with the written address from the master if the respective VALID bits within DDC_CON register are logic 0<br>✧The default value of the high order bit is %1010 | |
| 6 | ADDR_B6 | | |
| 5 | ADDR_B5 | | |
| 4 | ADDR_B4 | | |
| 3 | ADDR_B3 | | |
| 2 | ADDR_B2 | | |
| 1 | ADDR_B1 | | |
| 0 | | Unused | |

Default: 1010 0000B

| 0x07A | | DDC0 Port Slave Address Mask | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | INT_ UPD_DDC | RAM-Buffer contents updated interrupt enable | |
| 6-4 | | Reserved | |
| 3 | VALID_B3 | Valid/Mask Bit3, 2, 1 of slave address for DDC0-Port Addressing<br>0 = Masked:<br>➔ The respective address bits (ADDR_B3, 2 and 1 at register DDC_ADDR) will be Don't care for DDC0-Port addressing<br>1 = Valid:<br>➔ Otherwise, they will be valid address bits of DDC-Port | |
| 2 | VALID_B2 | | |
| 1 | VALID_B1 | | |
| 0 | | Reserved | |

Default: 0000 0000B

| 0x07B | | DDC1 Port Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | DDC_EN | DDC1 enable control<br>0 = Disable<br>1 = Enable | |
| 6 | WPT_DDC | DDC1 RAM write-Protect Mode<br>0 = DDC0 RAM-Buffer is R/W Mode<br>1 = DDC0 RAM-Buffer is read only under Write-Protect Mode | |
| 5 | LEN_EDID | DDC1 EDID Data length<br>0 = 128 Bytes<br>1 = 256 Bytes | |
| 4 | MODE_DDC | DDC1 Mode control<br>0 = DDC1<br>H/W ➔ a default state after system reset<br>S/W ➔ clear this bit by S/W to force into DDC1 mode<br>1 = DDC2<br>H/W ➔ automatically set this bit when SCL go-low pulse is detected<br>S/W ➔ set by S/W to force into DDC2B mode | |
| 3 | EN_BACK | Enable Bit for automatically switching back to DDC1 mode if VCLK>128<br>0 = Disable<br>1 = Enable | |
| 2 | INVT_VCLK | The VCLK invert control bit for DDC1 communication<br>0 = the polarity of the VCLK is the same as the of the VSYNC<br>1 = the polarity of the VCLK is inverted with the one of the VSYNC | |
| 1 | CLR_PTR | Clear the contents of Address Pointer of the DDC RAM-Buffer<br>0 = No effect<br>1 = Clear it once after writing an 1 into this bit | |
| 0 | UPD_DDC (R)/ | RAM-Buffer contents updated flag (set by H/W)<br>0 = Not Updated<br>1 = Updated | |
| | CLR_UPD (W) | Clear bit of the UPD_DDC bit<br>0 = No effect<br>1 = Clear the UPD_DDC flag | |

Default: 0100 1000B

| 0x07C | | DDC1 Port Slave Address Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |

| | | |
|---|---|---|
| 7 | ADDR_B7 | Slave Address Bit-3~1 of the DDC1-Port<br>➔These 3 lower order bits of the 7-bit slave address can be masked to compare with the written address from the master if the respective VALID bits within DDC_CON register are logic 0<br>✧The default value of the high order bit is %1010 |
| 6 | ADDR_B6 | |
| 5 | ADDR_B5 | |
| 4 | ADDR_B4 | |
| 3 | ADDR_B3 | |
| 2 | ADDR_B2 | |
| 1 | ADDR_B1 | |
| 0 | | Unused |

Default: 1010 0000B

| **0x07D** | **DDC1 Port Slave Address Mask** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7 | INT_ UPD_DDC | RAM-Buffer contents updated interrupt enable |
| 6-4 | | Reserved |
| 3 | VALID_B3 | Valid/Mask Bit3, 2, 1 of slave address for DDC1-Port Addressing<br>0 = Masked:<br>➔ The respective address bits (ADDR_B3, 2 and 1 at register DDC_ADDR) will be Don't care for DDC1-Port addressing<br>1 = Valid:<br>➔ Otherwise, they will be valid address bits of DDC1-Port |
| 2 | VALID_B2 | |
| 1 | VALID_B1 | |
| 0 | | Reserved |

Default: 0000 0000B

| **0x07E** | **PWM Control 1** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7 | PWM1_VS_LOCK | PWM1 counter lock to display vertical sync<br>0 = Roll PWM counter over continuously<br>1 = Load PWM on Display VS (DISP_VS) leading edge |
| 6-5 | PWM1_DIV1 [1:0] | First divider-- PWM1 clock divide of the selected clock by<br>00 = 1; 01 = 2<br>10 = 4; 11 = 8 |
| 4 | PWM1_CLK | PWM1 clock source select<br>0 = Reference Clock<br>1 = Display HS (DISP_HS) |
| 3 | PWM0_VS_LOCK | PWM0 counter lock to display vertical sync<br>0 = Load PWM counter when high period counter<br>1 = Load PWM on Display VS (DISP_VS) leading edge |
| 2-1 | PWM0_DIV1 [1:0] | First divider-- PWM0 clock divide of the selected clock by<br>00 = 1; 01 = 2<br>10 = 4; 11 = 8 |
| 0 | PWM0_CLK | PWM0 clock source select<br>0 = Reference Clock<br>1 = Display HS (DISP_HS) |

Default: 0000 0000B

| **0x07F** | **PWM Control 2** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-4 | | Reserved |

| | | |
|---|---|---|
| 3-2 | PWM1_ DIV2 | Second divider--PWM1 clock divide of the selected clock by<br>00 = 1; 01 = 512<br>10 = 1024; 11 = 2048 |
| 1-0 | PWM0_DIV2 [1:0] | Second divider--PWM0 clock divide of the selected clock by<br>00 = 1; 01 = 512<br>10 = 1024; 11 = 2048 |

Default: 0000 0000B

## 9.13. On Screen Display Registers

**OSD Control**

| **0x080** | **OSD and Window Enable Control** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7 | ROT_EN | Rotation control.<br>0: Normal<br>1: Rotated |
| 6 | FLIP_EN | Flip control<br>0: No flip<br>1: Flip ON |
| 5 | MIR_EN | Mirror control<br>0: No mirror<br>1: Mirror ON |
| 4 | WIN4_EN | Enable Window 4<br>0: Disable<br>1: Enable |
| 3 | WIN3_EN | Enable Window 3<br>0: Disable<br>1: Enable |
| 2 | WIN2_EN | Enable Window 2<br>0: Disable<br>1: Enable |
| 1 | WIN1_EN | Enable Window 1<br>0: Disable<br>1: Enable |
| 0 | OSD_EN | Enable OSD<br>0: Disable<br>1: Enable |

Default: 0000 0000B

| **0x081** | **OSD Frame Horizontal Start - Low byte** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-0 | OSD_HS [7:0] | OSD frame horizontal start low byte [7:0]. Specifies the horizontal starting position of the OSD in pixel units. This register is **double-buffered**. |

Default: 0000 0000B

| **0x082** | **OSD Frame Horizontal Start - High Byte** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-4 | | Reserved |
| 3-0 | OSD_HS [11:8] | OSD frame horizontal start high byte [11:8]. Specifies the horizontal starting position of the OSD in pixel units. This register is **double-buffered**. |

Default: XXXX 0000B

| 0x083 | | OSD Frame Horizontal Width | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | | Reserved | |
| 5-0 | OSD_HW [5:0] | Specifies the width of the OSD in font units.<br>Range: 0~ 63 (OSD display width = 1~64) | |

Default: XX00 0000B

| 0x084 | | OSD Frame Vertical Start Low byte | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_VS [7:0] | OSD frame vertical start low byte [7:0]. Specifies the vertical starting position of the OSD in line units. This register is **double-buffered**. | |

Default: 0000 0000B

| 0x085 | | OSD Frame Vertical Start High byte | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-3 | | Reserved | |
| 2-0 | OSD_VS [10:8] | OSD frame vertical start high byte [10:8]. Specifies the vertical starting position of the OSD in line units. This register is **double-buffered**. | |

Default: XXXX X000B

| 0x086 | | OSD Frame Vertical Height | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-5 | | Reserved | |
| 4-0 | OSD_VH [4:0] | Specifies the height of the OSD in font units.<br>Range: 0~31 (OSD display height = 1~32) | |

Default: XXX0 0000B

| 0x087 | | OSD Shift Row Offset | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 4-0 | OSD_SHIFT_ROW | Specifies the row of the OSD shift offset.<br>Range: 0~31 | |

Default: X000 0000B

| 0x088 | | OSD One Bit Font Address - Low Byte | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | FONT1B_ADDR [7:0] | OSD one bit per pixel programmable font start address high byte [7:0].<br>Specifies the start address for the On-Chip programmable font.<br>Default for this 12 bit register = 1000 (dec) | |

Default: 1110 1000B

| 0x089 | | OSD One bit Font Address - High Byte | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | FONT1B_ADDR [11:8] | OSD one bit per pixel programmable font start address high byte [11:8].<br>Specifies the start address for the On-Chip programmable font<br>Default for this 12 bit register = 1000 (dec) | |

Default: XXXX 0011B

| 0x08A | OSD Two Bit Font Address - Low Byte | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | FONT2B_ADDR [7:0] | OSD two bit per pixel programmable font start address high byte [7:0].<br>Specifies the start address for the On-Chip programmable font.<br>Default for this 12 bit register = 2656 (dec) |

Default: 0110 0000B

| 0x08B | OSD Two Bit Font Address - High Byte | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 3-0 | FONT2B_ADDR [11:8] | OSD two bit per pixel programmable font start address high byte [11:8].<br>Specifies the start address for the On-Chip programmable font<br>Default for this 12 bit register = 2656 (dec) |

Default: XXXX 1010B

| 0x08C | OSD Four Bit Font Address - Low Byte | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | FONT4B_ADDR [7:0] | OSD four bit per pixel programmable font start address high byte [7:0].<br>Specifies the start address for the On-Chip programmable font.<br>Default for this 12 bit register = 3808 (dec) |

Default: 1110 0000B

| 0x08D | OSD Four Bit Font Address - High Byte | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 3-0 | FONT4B_ADDR [11:8] | OSD four bit per pixel programmable font start address high byte [11:8].<br>Specifies the start address for the On-Chip programmable font<br>Default for this 12 bit register = 3808 (dec) |

Default: XXXX 1110B

**OSD Fade in/out Control**

| 0x08E | OSD Fade-in / Fade-out Step | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-4 | FAD_V_STEP [3:0] | OSD Vertical side Fade-in / Fade-out Step (4 pixel/step)<br>0~15 step |
| 3-0 | FAD_H_STEP [3:0] | OSD Horizontal side Fade-in / Fade-out Step (4 pixel/step)<br>0~15 step |

Default: 0000 0000B

| 0x08F | OSD Fade-in / Fade-out Frequency | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7 | FAD_EN | Fade-in / Fade-out function enable.<br>0: Fade-in / Fade-out disable<br>1: Fade-in / Fade-out enable |
| 6-4 | FAD_VFREQ [2:0] | OSD Fade-in / Fade-out Vertical Frequency for every step |
| 3-0 | FAD_HFREQ [3:0] | OSD Fade-in / Fade-out Horizontal Frequency for every step |

Default: 0000 0000B

**OSD Zoom Control**

| 0x090 | OSD Zoom Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|

| | | |
|---|---|---|
| 7-4 | | Reserved |
| 3 | VROW_ZMEN | Vertical Row Zoom Enable; Vertical zoom for all characters in one row defined in Reg 0x09A ~ 0x09D.<br>0: Disable<br>1: Enable. |
| 2 | HROW_ZMEN | Horizontal Row Zoom Enable; Horizontal zoom for all characters in one row defined in Reg 0x096 ~ 0x099.<br>0: Disable<br>1: Enable. |
| 1 | VGLOB_ZMEN | Vertical Global Zoom Enable; Vertical zoom for all characters in OSD frame.<br>0: Disable<br>1: Enable. |
| 0 | HGLOB_ZMEN | Horizontal Global Zoom Enable; Horizontal zoom for all characters in OSD frame.<br>0: Disable<br>1: Enable. |

Default: XXXX 0000B

| **0x091** | | **OSD Font Horizontal Global Zoom Pattern - Low Byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HZM_PATN [7:0] | Least significant 8 bits (7:0) of the horizontal zoom pattern.<br>This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range. | |

Default: 0000 0000B

| **0x092** | | **OSD Font Horizontal/Vertical Global Zoom Pattern - High Byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-6 | | Reserved | |
| 5-4 | VZM_PATN [17:16] | Most significant 2 bits (17:16) of the vertical zoom pattern.<br>This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range. | |
| 3-0 | HZM_PATN [11:8] | Most significant 4 bits (11:8) of the horizontal zoom pattern.<br>This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range. | |

Default: XX00 0000B

| **0x093** | | **OSD Font Vertical Global Zoom Pattern - Low Byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VZM_PATN [7:0] | Least significant 8 bits (7:0) of the vertical zoom pattern.<br>This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range. | |

Default: 0000 0000B

| **0x094** | | **OSD Font Vertical Global Zoom Pattern - Mid Byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VZM_PATN [15:8] | Bits (15:8) of the vertical zoom pattern.<br>This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range. | |

Default: 0000 0000B

| 0x095 | | OSD Font Global Zoom Range | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-6 | VGLOB_ZMRNG1 [1:0] | Vertical Global Zoom Pattern (Reg 0x092 ~ 0x094) '1' Zoom Range<br>00: No Zoom<br>01: Vertical Zoom Pattern '1' bits are duplicated once<br>10: Vertical Zoom Pattern '1' bits are duplicated twice<br>11: Vertical Zoom Pattern '1' bits are duplicated three times | |
| 5-4 | HGLOB_ZMRNG1 [1:0] | Horizontal Global Zoom Pattern (Reg 0x091 ~ 0x092) '1' Zoom Range<br>00: No Zoom<br>01: Horizontal Zoom Pattern '1' bits are duplicated once<br>10: Horizontal Zoom Pattern '1' bits are duplicated twice<br>11: Horizontal Zoom Pattern '1' bits are duplicated three times | |
| 3-2 | VGLOB_ZMRNG0 [1:0] | Vertical Global Zoom Pattern (Reg 0x092 ~ 0x094) '0' Zoom Range<br>00: No Zoom<br>01: Vertical Zoom Pattern '0' bits are duplicated once<br>10: Vertical Zoom Pattern '0' bits are duplicated twice.<br>11: Vertical Zoom Pattern '0' bits are duplicated three times. | |
| 1-0 | HGLOB_ZMRNG0 [1:0] | Horizontal Global Zoom Pattern (Reg 0x091 ~ 0x092) '0' Zoom Range<br>00: No Zoom<br>01: Horizontal Zoom Pattern '0' bits are duplicated once<br>10: Horizontal Zoom Pattern '0' bits are duplicated twice<br>11: Horizontal Zoom Pattern '0' bits are duplicated three times | |

Default: 0000 0000B

| 0x096 | | Horizontal Row Zoom Control Row 7 - 0 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HROW_ZMPN [7:0] | Horizontal Row Zoom Pattern 7-0<br>Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'. | |

Default: 0000 0000B

| 0x097 | | Horizontal Row Zoom Control Row 15 - 8 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HROW_ZMPN [15:8] | Horizontal Row Zoom Pattern 15-8<br>Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'. | |

Default: 0000 0000B

| 0x098 | | Horizontal Row Zoom Control Row 23 - 16 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HROW_ZMPN [23:16] | Horizontal Row Zoom Pattern 23-16<br>Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'. | |

Default: 0000 0000B

| 0x099 | | Horizontal Row Zoom Control Row 31 - 24 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HROW_ZMPN [31:24] | Horizontal Row Zoom Pattern 31-24<br>Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'. | |

Default: 0000 0000B

| 0x09A | | Vertical Row Zoom Control Row 7 - 0 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VROW_ZMPN [7:0] | Vertical Row Zoom Pattern 7-0<br>Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'. | |

Default: 0000 0000B

| 0x09B | | Vertical Row Zoom Control Row 15 - 8 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VROW_ZMPN [15:8] | Vertical Row Zoom Pattern 15-8<br>Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'. | |

Default: 0000 0000B

| 0x09C | | Vertical Row Zoom Control Row 23 - 16 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VROW_ZMPN [23:16] | Vertical Row Zoom Pattern 23-16<br>Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'. | |

Default: 0000 0000B

| 0x09D | | Vertical Row Zoom Control Row 31 - 24 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VROW_ZMPN [31:24] | Vertical Row Zoom Pattern 31-24<br>Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'. | |

Default: 0000 0000B

| 0x09E | | OSD Font Row Zoom Range | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | | Reserved | |
| 3-2 | VROW_ZMRNG [1:0] | Vertical Row Zoom Range; The rows assigned by Vertical Row Zoom Control registers will be zoomed up.<br>00: Vertical Zoom 1x for all fonts in the row<br>01: Vertical Zoom 2x for all fonts in the row<br>10: Vertical Zoom 3x for all fonts in the row<br>11: Vertical Zoom 4x for all fonts in the row | |
| 1-0 | HROW_ZMRNG [1:0] | Horizontal Row Zoom Range; The rows assigned by Horizontal Row Zoom Control registers will be zoomed up.<br>00: Horizontal Zoom 1x for all fonts in the row<br>01: Horizontal Zoom 2x for all fonts in the row<br>10: Horizontal Zoom 3x for all fonts in the row<br>11: Horizontal Zoom 4x for all fonts in the row | |

Default: XXXX 0000B

| 0x09F | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| | | | |

Default: 0000 0000B

**OSD Translucent and Blinking Control**

| 0x0A0 | | OSD Blink Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | | Reserved | |
| 6 | OSD_BLINK | Blink<br>1=OSD frame blink enable, don't care the attribute bit 0.<br>0=Blink control from font attribute bit 0. | |
| 5 | BS_BLINK | Mask Border/Shadow at Blink<br>1=Character border/shadow will not blink with the foreground of the character.<br>0= Character border/shadow will blink with the foreground of the character. | |
| 4-2 | BLINK_FREQ [2:0] | Blink Frequency<br>000: Character foreground's blinking period is 4 frames.<br>001: Character foreground's blinking period is 8 frames.<br>010: Character foreground's blinking period is 16 frames.<br>011: Character foreground's blinking period is 32 frames.<br>100: Character foreground's blinking period is 64 frames. | |
| 1-0 | BLINK_RATE [1:0] | Blink Rate<br>00: Character foreground is turned 25% on / 75% off.<br>01: Character foreground is turned 50% on / 50% off.<br>10: Character foreground is turned 75% on / 25% off.<br>11: reserved. | |

Default: X000 0001B

| 0x0A1 | | OSD Character Translucent Level | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| | | | |
| 5-3 | TP_LEVEL_TWO [2:0] | When the attribute BG_Index is set to "0001", these 3-bits set the translucent level of the character background color. Translucent level refers to the percentage of color composition that is OSD.<br>"111" = 0% "110" = 12.25%<br>"101" = 25% "100" = 37.5%<br>"011" = 50% "010" = 62.5%<br>"001" = 75% "000" = 87.5% | |
| 2-0 | TP_LEVEL_ONE [2:0] | When the attribute BG_Index is set to "0000" ~ "1111" except "0001", these 3-bits set the translucent level of the character background color. Translucent level refers to the percentage of color composition that is OSD.<br>"111" = 0% "110" = 12.25%<br>"101" = 25% "100" = 37.5%<br>"011" = 50% "010" = 62.5%<br>"001" = 75% "000" = 87.5% | |

Default: XX00 0000B

**OSD Spacing Control**

| 0x0A2 | | OSD Space | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | V_FS_SEL | Vertical Font size selection | |

| | | |
|---|---|---|
| | | 0: 18 font size for Vertical<br>1: 16 font size for Vertical |
| 6 | H_FS_SEL | Horizontal Font size selection<br>0: 12 font size selected for Horizontal<br>1: 10 font size selected for Horizontal |
| 5-3 | VSPACE [2:0] | OSD vertical space. These 3 bits define the vertical scan pixel of background color added to above and below of each character.<br>Range: 0~7 |
| 2-0 | HSPACE [2:0] | OSD horizontal space. These 3 bits define the horizontal scan pixel of background color added to left and right of each character.<br>Range: 0~7 |

Default: 0000 0000B

| **0x0A3~0x0A4** | **Reserved** | R/W |
|---|---|---|
| Bits | Name | Description |
| | | |

Default: 0000 0000B

**OSD Window Control**

| **0x0A5** | **OSD Window Select** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7 | WIN8_EN | Enable Window 8<br>0: Disable<br>1: Enable |
| 6 | WIN7_EN | Enable Window 7<br>0: Disable<br>1: Enable |
| 5 | WIN6_EN | Enable Window 6<br>0: Disable<br>1: Enable |
| 4 | WIN5_EN | Enable Window 5<br>0: Disable<br>1: Enable |
| 3 | | Reserved |
| 2-0 | WIN_SEL [2:0] | This register is used to select which window is to be accessed or modified. It is programmed prior to accessing the registers Reg 0x0A6h ~ 0x0AFh<br>“000” = Window1 “001” = Window2<br>“010” = Window3 “011” = Window4<br>“100” = Window5 “101” = Window6<br>“110” = Window7 “111” = Window8 |

Default: 0000 X000B

| **0x0A6** | **OSD Window Horizontal Start** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-6 | | Reserved |
| 5-0 | WIN_HS [5:0] | Horizontal starting position relative to the OSD for the selected window. The unit is in font.<br>Range: 0~63 |

Default: XX00 0000B

| 0x0A7 | | OSD Window Horizontal End | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-6 | | Reserved | |
| 5-0 | WIN_HE [5:0] | Horizontal ending position relative to the OSD for the selected window. The unit is in font.<br>The OSD Window Horizontal Width = (WIN_HE+1) - WIN_HS<br>Range: 0~63 | |

Default: XX00 0000B

| 0x0A8 | | OSD Window Vertical Start | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 4-0 | WIN_VS [4:0] | Vertical starting position relative to the OSD for the selected window. The unit is in font.<br>Range: 0~31 | |

Default: XXX0 0000B

| 0x0A9 | | OSD Window Vertical End | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-5 | | Reserved | |
| 4-0 | WIN_VE [4:0] | Vertical ending position relative to the OSD for the selected window. The unit is in font.<br>The OSD Window 1 Vertical Height = (WIN1_VE+1) - WIN1_VS<br>Range: 0~31 | |

Default: XXX0 0000B

| 0x0AA | | OSD Window Attribute | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | WIN_BLEN | Window bevel enable<br>Bevel size is specified in WIN_BL_HWID [2:0] and WIN_BL_VHEI[2:0] | |
| 6-5 | WIN_BL_TYPE | Window bevel type<br>00: Type 1<br>01: Type 2<br>10: Type 3<br>11: Type 4 | |
| 4 | WIN_MIX | Window translucent enable for the selected window<br>0 - Normal<br>1 - Translucent ((1- TP_LEVEL_ONE) * Display + (TP_LEVEL_ONE) * OSD_BG) | |
| 3-2 | WIN_SDSZ [1:0] | Shadow Size for the selected window when window shadow enable<br>00: 2 pixels in width and 2 lines in height.<br>01: 4 pixels in width and 4 lines in height.<br>10: 6 pixels in width and 6 lines in height.<br>11: 8 pixels in width and 8 lines in height. | |
| 1 | WIN_SDEN | Window Shadow Enable for the selected window<br>Shadow size is specified in bits 3:2.<br>1= Shows a shadow for Window.<br>0= No shadow | |
| 0 | | Reserved | |

Default: 0000 000XB

| 0x0AB | | OSD Window Color | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | WIN_CL [7:0] | Color index for the selected OSD Window. This color will cover the character background color when Window is enabled. | |

Default: 0000 0000B

| 0x0AC | | OSD Window Shadow Color | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | WIN_SDCL [7:0] | Color index for all eight window's shadow | |

Default: 0000 0000B

| 0x0AD | | OSD Window Bevel Width | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | | Reserved | |
| 2-0 | WIN_BL_VWID [2:0] | Specifies the width of the window bevel units.<br>Range: 1~8 | |

Default: 0000 0000B

| 0x0AE | | OSD Window Bevel Right Color | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | WIN_BL_RCL [7:0] | Color index for all eight window's right side bevel | |

Default: 0000 0000B

| 0x0AF | | OSD Window Bevel Left Color | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | WIN_BL_LCL [7:0] | Color index for all eight window's left side bevel | |

Default: 0000 0000B

**OSD Border And Shadow Control**

| 0x0B0 | | OSD Shadow Control Row 7 - 0 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_SCR [7:0] | Character Row Shadow Enable for 7-0. Each bit controls each row correspondingly. Used only in one bit per pixel font.<br>1= Enable shadow for a row. | |

Default: 0000 0000B

| 0x0B1 | | OSD Shadow Control Row 15 - 8 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_SCR [15:8] | Character Row Shadow Enable for 15-8. Each bit controls each row correspondingly. Used only in one bit per pixel font.<br>1= Enable shadow for a row. | |

Default: 0000 0000B

| 0x0B2 | | OSD Shadow Control Row 23 - 16 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_SCR | Character Row Shadow Enable for 23-16. Each bit controls each row | |

| | | |
|---|---|---|
| | [23:16] | correspondingly. Used only in one bit per pixel font.<br>1= Enable shadow for a row. |

Default: 0000 0000B

| 0x0B3 | | OSD Shadow Control Row 31 - 24 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_SCR [31:24] | Character Row Shadow Enable for 31-24. Each bit controls each row correspondingly. Used only in one bit per pixel font.<br>1= Enable shadow for a row. | |

Default: 0000 0000B

| 0x0B4 | | OSD Border Control Row 7 - 0 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_BCR [7:0] | Character Row Border Enable for 7-0. Each bit controls each row correspondingly. Used only in one bit per pixel font.<br>1= Enable border for a row. | |

Default: 0000 0000B

| 0x0B5 | | OSD Border Control Row 15-8 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_BCR [15:8] | Character Row Border Enable for 15-8. Each bit controls each row correspondingly. Used only in one bit per pixel font.<br>1= Enable border for a row. | |

Default: 0000 0000B

| 0x0B6 | | OSD Border Control Row 23-16 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_BCR [23:16] | Character Row Border Enable for 23-16. Each bit controls each row correspondingly. Used only in one bit per pixel font.<br>1= Enable border for a row. | |

Default: 0000 0000B

| 0x0B7 | | OSD Border Control Row 31-24 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_BCR [31:24] | Character Row Border Enable for 31-24. Each bit controls each row correspondingly. Used only in one bit per pixel font.<br>1= Enable border for a row. | |

Default: 0000 0000B

| 0x0B8 | | OSD Border & Shadow Color Row 1 - 0 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR1 [3:0] | Character Border/Shadow Color Index For Row 1. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR0 [3:0] | Character Border/Shadow Color Index For Row 0. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0B9 | | OSD Border & Shadow Color Row 3 - 2 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR3 | Character Border/Shadow Color Index For Row 3. Used only in one bit per | |

| | | |
|---|---|---|
| | [3:0] | pixel font. |
| 3-0 | OSD_BSCR2 [3:0] | Character Border/Shadow Color Index For Row 2. Used only in one bit per pixel font. |

Default: 0000 0000B

| 0x0BA | | OSD Border & Shadow Color Row 5 - 4 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR5 [3:0] | Character Border/Shadow Color Index For Row 5. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR4 [3:0] | Character Border/Shadow Color Index For Row 4. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0BB | | OSD Border & Shadow Color Row 7- 6 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR7 [3:0] | Character Border/Shadow Color Index For Row 7. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR6 [3:0] | Character Border/Shadow Color Index For Row 6. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0BC | | OSD Border & Shadow Color Row 9 - 8 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR9 [3:0] | Character Border/Shadow Color Index For Row 9. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR8 [3:0] | Character Border/Shadow Color Index For Row 8. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0BD | | OSD Border & Shadow Color Row 11 - 10 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR11 [3:0] | Character Border/Shadow Color Index For Row 11. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR10 [3:0] | Character Border/Shadow Color Index For Row 10. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0BE | | OSD Border & Shadow Color Row 13 - 12 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR13 [3:0] | Character Border/Shadow Color Index For Row 13. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR12 [3:0] | Character Border/Shadow Color Index For Row 12. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0BF | | OSD Border & Shadow Color Row 15 - 14 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR15 [3:0] | Character Border/Shadow Color Index For Row 15. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR14 | Character Border/Shadow Color Index For Row 14. Used only in one bit per | |

| | | |
|---|---|---|
| | [3:0] | pixel font. |

Default: 0000 0000B

| 0x0C0 | | OSD Border & Shadow Color Row 17 - 16 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR17 [3:0] | Character Border/Shadow Color Index For Row 17. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR16 [3:0] | Character Border/Shadow Color Index For Row 16. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0C1 | | OSD Border & Shadow Color Row 19 - 18 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR19 [3:0] | Character Border/Shadow Color Index For Row 19. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR18 [3:0] | Character Border/Shadow Color Index For Row 18. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0C2H | | OSD Border & Shadow Color Row 21 - 20 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR21 [3:0] | Character Border/Shadow Color Index For Row 21. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR20 [3:0] | Character Border/Shadow Color Index For Row 20. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0C3 | | OSD Border & Shadow Color Row 23- 22 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR23 [3:0] | Character Border/Shadow Color Index For Row 23. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR22 [3:0] | Character Border/Shadow Color Index For Row 22. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0C4 | | OSD Border & Shadow Color Row 25 - 24 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR25 [3:0] | Character Border/Shadow Color Index For Row 25. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR24 [3:0] | Character Border/Shadow Color Index For Row 24. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0C5 | | OSD Border & Shadow Color Row 27 – 26 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR27 [3:0] | Character Border/Shadow Color Index For Row 27. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR26 [3:0] | Character Border/Shadow Color Index For Row 26. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0C6 | | OSD Border & Shadow Color Row 29 – 28 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR29 [3:0] | Character Border/Shadow Color Index For Row 29. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR28 [3:0] | Character Border/Shadow Color Index For Row 28. Used only in one bit per pixel font. | |

Default: 0000 0000B

| 0x0C7 | | OSD Border & Shadow Color Row 31 - 30 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | OSD_BSCR31 [3:0] | Character Border/Shadow Color Index For Row 31. Used only in one bit per pixel font. | |
| 3-0 | OSD_BSCR30 [3:0] | Character Border/Shadow Color Index For Row 30. Used only in one bit per pixel font. | |

Default: 0000 0000B

**OSD Splitting Control**

| 0x0C8 | | OSD Horizontal Splitting Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | H_SPL_EN | Horizontal Splitting Enable<br>0: Disable<br>1: Enable | |
| 6-0 | SPL_HP [6:0] | Splitting horizontal begin position relative to the OSD frame for the selected window. The unit is in 4 pixels.<br>Range: 0~127 | |

Default: 0000 0000B

| 0x0C9 | | OSD Horizontal Splitting width Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | SPL_HW [7:0] | Splitting horizontal width relative to the OSD frame. The unit is in 4 pixels.<br>Range: 0~255 | |

Default: 0000 0000B

| 0x0CA | | OSD Vertical Splitting Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | V_SPL_EN | Vertical Splitting Enable<br>0: Disable<br>1: Enable | |
| 6 | | Reserved | |
| 5-0 | SPL_VP [5:0] | Splitting vertical begin position relative to the OSD frame. The unit is in 4 lines.<br>Range: 0~64 | |

Default: 0000 0000B

| 0x0CB | | OSD Vertical Splitting Height Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | SPL_VH [7:0] | Splitting vertical height relative to the OSD frame. The unit is in 4 lines.<br>Range: 0~255 | |

Default: 0000 0000B

**OSD Attribute Control and OSD Fast Clear Control**

| 0x0CC | | OSD Attribute LSB | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_ATTR [7:0] | OSD Attribute LSB. The register OSD_ATTR [15:0] is use for fast clear and update code from host and attribute from Register. This value is appended with the character font code. When update OSD SRAM code from host and “attribute from Reg 0x0CC ~ 0x0CD is selected in Reg 0x0E0 [7:4]. If fast clear is enable, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute). | |

Default: 0000 0000B

| 0x0CD | | OSD Attribute MSB | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | OSD_ATTR [15:8] | OSD attribute MSB. The register OSD_ATTR [15:0] is use for fast clear and update code from host and attribute from Register. This value is appended with the character font code. When update OSD SRAM code from host and “attribute from Reg 0x0CC ~ 0x0CD is selected in Reg 0x0E0 [7:4]. If fast clear is enable, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute). | |

Default: 0000 0000B

| 0x0CE | | OSD SRAM Code Value For Fast Clear | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | CODE_FC [7:0] | SRAM code for fast clear. | |

Default: 0000 0000B

| 0x0CF | | Fast Clear and Fade Mode Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-6 | FADE_MODE | Fade-in/Fade-out mode select<br>00:Left-Top corner<br>01:Right-Top corner<br>10:Left-Bottom corner<br>11:Right-Bottom corner | |
| 5 | BG_MIX_EN | Background translucent enables. | |
| 4 | FG_MIX_EN | Foreground translucent enables. | |
| 3 | BS_MIX_EN | Border/Shadow translucent enable. | |
| 2 | WIN_MIX_EN | Windows translucent enable. | |
| 1 | FC_MASK | Fast Clear area mask<br>0: SRAM on OSD frame<br>1: SRAM on 0x0000 to One bit Font Address | |
| 0 | FC_EN (W)/ FC_RDY (R) | Fast Clear Enable, When enable this bit, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute).<br>1: Enable the fast clear. If fast clear is finished, this bit FC_RDY will be clear to ‘0’.<br>0: No Effect | |

Default: 0000 0000B

## 9.14. Source Hsync Digital PLL Control

| 0x0D0 | | HS DDS PLL Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | HSDDS_DEBUG_MODE | | |
| 6 | VER_DOUB_BYPASS | Vertical double buffer bypass<br>0: Normal<br>1: Bypass | |
| 5 | DBL_EN | Double buffer Load Data at VSYNC Blanking<br>0: Disable<br>1: Enable | |
| 4 | | Reserved | |
| 3 | HSDDS_RST | HS DDS Reset<br>0: Normal<br>1: Reset | |
| 2 | OCLK_DIV | Oscillator Clock divide<br>0: Normal<br>1: Divide 2 | |
| 1 | HSDDS_UNLOCK_CHK | HS PLL unlock check<br>0: Disable<br>1: Enable | |
| 0 | DDS_EN | Reserved | |

Default: 000X 0000B

| 0x0D1 | | HS Frequency Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 6-4 | HSDDS_LOOP_FILTER [2:0] | HS DDS loop filter control | |
| 3 | HSDDS_DIV_CTRL | HS DDS Divide control<br>0: Enable<br>1: Disable | |
| 2 | | Reserved | |
| 1-0 | HPLL_FREQ_RANGE [1:0] | HS DDS output frequency range control<br>00: 100~200MHz<br>01: 50~100MHz<br>10: 25~50MHz<br>11: 12.5~25MHz | |

Default:X001 0000B

| 0x0D2 | | HS PLL Frequency Control Ratio – lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HSDDS_RATIO [7:0] | HS PLL frequency control ration | |

Default: 0000 0000B

| 0x0D3 | | HS PLL Frequency Control Ratio - mi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HSDDS_RATIO [15:8] | HS PLL frequency control ration | |

Default: 0000 0000B

| 0x0D4 | HS PLL Frequency Control Ratio – hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 5-0 | HSDDS_RATIO [21:16] | HS PLL frequency control ration |

Default: 0000 1010B

| 0x0D5 | HS PLL phase lock control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-5 | | Reserved |
| 4 | | Reserved |
| 3 | HS_INV | HSYNC Invert<br>0: Normal<br>1: Inverted |
| 2 | HPLL_OP_LOOP | HS PLL open loop control<br>0: Disable<br>1: Enable |
| 1 | HS_QUICK_UNLOCK_CHK | HS PLL quick unlock check<br>0: Disable<br>1: Enable |
| 0 | HPLL_EN | HS PLL DDS enable<br>0: Disable<br>1: Enable |

Default: 1000 0011B

| 0x0D6 | HS PLL control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | HPLL_LOCK_EN | HS PLL phase lock enable |
| 6-5 | HPLL_PLOOP_FIT [1:0] | HS PLL phase lock error correction ratio |
| 4-3 | HPLL_FLOOP_FIT0 [1:0] | HS PLL frequency lock mode long time adjust level select<br>00: 16<br>01: 32<br>10: 64<br>11: 128 |
| 2-0 | HPLL_FLOOP_FIT1 [2:0] | HS PLL phase lock mode long time adjust duration select<br>000: 1 001: 2<br>010: 4 011: 8<br>100: 16 101: 32<br>110: 64 111:128 |

Default: 0011 1111B

| 0x0D7 | HS PLL divider - lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | HSDDS_DIVIDER [7:0] | Clock divides value in the feedback loop of the HS PLL. The HS PLL reference is the input Hsync signal. |

Default: 1001 0111B

| 0x0D8 | HS PLL divider - hi | R/W |
|---|---|---|
| Bits | Name | Description |

| | | |
|---|---|---|
| 3-0 | HSDDS_ DIVIDER [11:8] | The low byte [7:0] of HS PLL divider value. The register is **double-buffered**.<br>Divider = HSDDS_ DIVIDER <11:0> + 1 |

Default: XXXX 0110B

| **0x0D9** | **HS PLL phase control 1** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-6 | CLK_DLY_SEL | Select clock channel with clock delay adjusting.<br>00 = R<br>01 = G<br>10 = B<br>11 = Reserved |
| 5-0 | HS_PHASE_STEP [5:0] | HS PLL 64 step phase adjust |

Default: 0000 0000B

| **0x0DA** | **HS PLL Phase control 2** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-6 | | Reserved |
| 5 | ADC_CKI_INV | |
| 4 | ADC_CKD_INV | |
| 3-0 | ADC_CK_DELAY[3:0] | To ADC Clock delay control |

Default: 0000 0000B

| **0x0DB** | **HS PLL Line count Select** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-5 | | Reserved |
| 4-0 | HS_LINE_CNT_SEL [4:0] | Horizontal Sync Line Count Select<br>00000: 1 Line<br>00001: 2 Line<br>00010: 4 Line<br>00100: 8 Line<br>01000: 16 Line<br>10000: 32 Line |

Default: 0000 0100B

| **0x0DC** | **HS_DDS DPLL Output Control** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7-4 | ADC_CK_DUTY [3:0] | To ADC clock duty control |
| 3 | TMDS_CK_EN | Clock input to TMDS PLL enable<br>0: Disable<br>1: Enable |
| 2 | HSDDS_COAST_EN | HS PLL coast enable<br>0: Disable<br>1: Enable |
| 1 | CAP_CKO_INV | Capture clock output polarity invert<br>0: Normal<br>1: Inverted |
| 0 | EXT_CKIN_EN | External clock input enable |

| | | |
|---|---|---|
| | | 0: Disable<br>1: Enable |

Default: 0000 0000B

| 0x0DD | HS DPLL Frequency Read back– lo | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | HS_CNT_RESULT [7:0] | HS DPLL Frequency read back [7:0] |

Default: 0000 0000B

| 0x0DE | HS DPLL Frequency Read back - mi | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | HS_CNT_RESULT [15:8] | HS DPLL Frequency read back [15:8] |

Default: 0000 0000B

| 0x0DF | HS DPLL Frequency Read back – hi | R |
|---|---|---|
| Bits | Name | Description |
| 5-0 | HS_CNT_RESULT [21:16] | HS DPLL Frequency read back [21:16] |

Default: 0000 0000B

## 9.15. Index Port Access Control

| 0x0E0 | Index Access Port | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-4 | TBL_SEL<br>INDEX_ADDR [7:0]<br>INDEX_ADDR [7:0]<br>INDEX_ADDR [7:0]<br>INDEX_ADDR [7:0]<br><br>INDEX_ADDR [11:0]<br>INDEX_ADDR [11:0]<br>INDEX_ADDR [11:0]<br>INDEX_ADDR [11:0]<br>INDEX_ADDR [11:0]<br>INDEX_ADDR [11:0]<br><br>INDEX_ADDR [9:0]<br>INDEX_ADDR [7:0]<br>INDEX_ADDR [7:0]<br>INDEX_ADDR [7:0]<br>INDEX_ADDR [7:0]<br>INDEX_ADDR [7:0] | Table Select<br>0000: Red Gamma Table (Read/Write) (10 bits/word)<br>0001: Green Gamma Table (Read/Write) (10 bits/word)<br>0010: Blue Gamma Table (Read/Write) (10 bits/word)<br>0011: R/G/B Gamma Tables modified simultaneously (Write only) (10 bits/word)<br>0100: OSD SRAM code only (Read/Write) (8 bits/word)<br>0101: OSD SRAM attribute MSB (Read/Write) (8 bits/word)<br>0110: OSD SRAM attribute LSB (Read/Write) (8 bits/word)<br>0111: OSD SRAM attribute (Read/Write) (16 bits/word)<br>1000: OSD SRAM code and attribute (Read/Write) (24 bits/word)<br>1001: OSD SRAM code from host and attribute from Reg 0x0CC ~ 0x0CD (Read/Write) (8 bits/word)<br>1010: OSD Programmable 1 Bit Color Font (Read/Write) (24 bits/word)<br>1011: OSD Programmable 2 Bit Color Font (Read/Write) (24 bits/word)<br>1100: OSD Programmable 4 Bit Color Font (Read/Write) (24 bits/word)<br>1101: OSD Palette (Read/Write) (16 bits/word)<br>1110: DDC0 RAM-Buffer (Read/Write)(8 bits/word)<br>1111: DDC1 RAM-Buffer (Read/Write)(8 bits/word) |
| 3 | PORT_RW | Port Read/Write<br>0: Write<br>1: Read |
| D2-0 | | Reserve |

Default: 0000 0XXXB

| 0x0E1 | | Index Address Port - Low Byte | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | INDEX_ADDR [7:0] | Table Address – low bits | |

Default: 0000 0000B

| 0x0E2 | | Index Address Port - High Byte | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | INDEX_ADDR [15:8] | Table Address – upper bits | |

Default: 0000 0000B

| 0x0E3 | | Index Data Port | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | PORT_DATA [7:0] | Data port for the SRAM, Palette, and Programmable Font. | |

Default: 0000 0000B

Note: 1. If The Index Port's access is over 8 bit data length, the host interface will transfer or receive data from LSB to MSB.

## 9.16. Misc. Access Control

| 0x0E5 | | Host Interface Type Status | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-3 | | Reserve | |
| 2-1 | I2C_ADDR | I2C Address Bit [2:1] | |
| 0 | BUSTYPE | Host Interface Select<br>0: Parallel bus access<br>1: I2C bus access | |

Default: 0000 0001B

| 0x0E6 | | Register update Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | Reserve | |

Default: 0000 0000B

| 0x0E7~0x0EF | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| | | | |

Default: 0000 0000B

## 9.17. Display Digital PLL Control

| 0x0F0 | | Display DDS PLL Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | DDDS_DEBUG_MODE | | |
| 6-4 | | | |
| 3 | DDDS_RST | Display DDS Reset<br>0: Normal<br>1: Reset | |

| | | |
|---|---|---|
| 2 | | |
| 1 | DDDS_UNLOCK_CHK | Display PLL unlock check<br>0: Disable<br>1: Enable |
| 0 | DDDS_EN | Display DDS enable<br>0: Disable<br>1: Enable |

Default: 0000 0001B

| 0x0F1 | | Display Frequency Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 6-4 | DDDS_LOOP_FILTER [2:0] | Display DDS loop filter control | |
| 3-2 | | Reserved | |
| 1-0 | DPLL_FREQ_DIV [1:0] | Display DDS output frequency divider<br>00: Divide 1 (80~180MHz)<br>01: Divide 2 (40~80MHz)<br>10: Divide 4 (20~40MHz)<br>11: Divide 8 (10~20MHz) | |

Default: 0001 0000B

| 0x0F2 | | Display PLL Frequency Control Ratio – lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DDDS_RATIO [7:0] | Display DDS frequency control ration | |

Default: 0000 0000B

| 0x0F3 | | Display PLL Frequency Control Ratio - mi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DDDS_RATIO [15:8] | Display DDS frequency control ration | |

Default: 0000 0000B

| 0x0F4 | | Display PLL Frequency Control Ratio – hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 5-0 | DDDS_RATIO [21:16] | Display DDS frequency control ration | |

Default: 0000 1010B

| 0x0F5 | | SSC Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | SSC_MOD_FREQ | Display PLL spread spectrum modulation frequency control<br>“111” = REFCLK/4 “110” = REFCLK/8<br>“101” = REFCLK/16 “100” = REFCLK/32<br>“011” = REFCLK/64 “010” = REFCLK/128<br>“001” = REFCLK/256 “000” = REFCLK/512 | |
| 3-1 | SSC_RATIO | DDDS PLL spread spectrum ratio<br>“111” = 1/8 “110” = 1/16<br>“101” = 1/32 “100” = 1/64<br>“011” = 1/128 “010” = 1/256 | |

| | | |
|---|---|---|
| | | “001” = 1/512 “000” = 1/1024 |
| 1 | SSC_EN | DDS PLL spread spectrum enable<br>0: Disable<br>1: Enable |

Default: 0000 1010B

| 0x0F6~0x0F7 | Reserved | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| | | |

Default: 0000 0000B

## 9.18. Graphic Input Gauge

| 0x0F8 | Gauge Control | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7 | GAUGE_EN | To Gauge the distribution of input data. When GAUGE_EN set “1”, the function is enable, then if the gauge is finished this bit is cleared to “0”.<br>0 = Disable<br>1 = Enable |
| 6-5 | | Reserved |
| 4-3 | GAUGE_SEL | Gauge Source Select<br>00: Blue Channel<br>01: Green Channel<br>10: Red Channel<br>11: Reserved |
| 2-0 | GAUGE_STEP [7:0] | The step of gauge Data<br>000: 1 Step 100: 16 Step<br>001: 2 Step 101: 32 Step<br>010: 4 Step 110: Reserved<br>011: 8 Step 111: Reserved |

Default: 0X00 0000B

| 0x0F9 | Gauge Result Read Back Area Select | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-3 | | Reserved |
| 2-0 | GAUGE_AREA | The Gauge Result Read back area select<br>0~7 |

Default: XXXX X000B

| 0x0FA | Gauge Offset | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GAUGE_OFFSET | The level of Y/R/G/B Input when Gauge function is enable |

Default: XXX0 0000B

| 0x0FB | Gauge Result - lo | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GAUGE_RESULT [7:0] | The gauge result of input data in capture window |

Default:

| 0x0FC | Gauge Result - mi | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GAUGE_RESULT [15:8] | The gauge result of input data in capture window |

Default:

| 0x0FD | Gauge Result - hi | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GAUGE_RESULT [23:16] | The gauge result of input data in capture window |

Default:

| 0x0FE | Reserved | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| | | |

Default: 0000 0000B

## 9.19. Product ID

| 0x100 | Product ID | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-4 | REV_NO | IC revision number |
| 3-0 | CHIP_ID | Chip ID = 0110 |

## 9.20. Power Control

| 0x101 | Power Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7 | | Reserved |
| 6 | PU_LVDSA | LVDS A Port power up control.<br>0 = Power down<br>1 = Power up |
| 5 | WARM_RST | Chip Warm Reset. When WARM_RST=1, all state machines will be reset other than the all of register's value.<br>0 = Normal<br>1 = Reset |
| 4 | | Reserved |
| 3 | GCLK_OFF | Graphic Port Clock Off. When GCLK_OFF=1, Graphic Port clock is disabled to conserve power. This bit is reset only by external reset pin. |
| 2 | VCLK_OFF | Video Port Clock Off. When VCLK_OFF=1, Video Port clock is disabled to conserve power. This bit is reset only by external reset pin. |
| 1 | | Reserved |
| 0 | DCLK_OFF | Display Clock Off. When DCLK_OFF=1, display clock is disabled to conserve power. This bit is reset only by external reset pin. |

Default: 0000 11X1B

| 0x102 | Power Down Control 2 | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7 | | Reserved |
| 6 | PU_PLL | ADCPLL Power up frequency PLL.<br>0 = Power down |

| | | |
|---|---|---|
| | | 1 = Power up |
| 5 | PU_HPLL (hpll_en) | HPLL Power up control.<br>0 = Power down<br>1 = Power up |
| 4 | PU_TSEN | ADCPLL Power up on chip temperature sensor.<br>0 = Power down<br>1 = Power up |
| 3 | PU_ADC | ADC Power up control.<br>0 = Power down<br>1 = Power up |
| 2 | | |
| 1 | PU_TMDS | TMDS PD power up mode. When PU_TMDS = '0', TMDS circuit will go into power down state.<br>0 = Power down<br>1 = Power up |
| 0 | | Reserved |

Default: 1101 1000B

| **0x103~0x105** | **Reserved** | R/W |
|---|---|---|
| Bits | Name | Description |
| | | |

Default: 0000 0000B

## 9.21. Auto Tune

**Graphic Auto Tune Control**

| **0x106** | **Graphic Auto Tune Control** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 6 | GI_AUTO_MASK | Gain and Phase Detection Area masking when GI_GAINPHS_AREA = "1"<br>0 = Detecting area is whole frame<br>1 = Detecting area is defined by mask window registers. |
| 5 | GI_GAINPHS_AREA | Gain and Phase Detection Area Define Enable.<br>0 = Detecting area is over one frame except the area defined by mask window registers.<br>1 = Detecting area is defined by capture registers. |
| 4 | GI_POS_DE | Enable Position Detection depending on DE signal when TMDS is enabled. If GI_POS_DE =1, 0xFF data is input to RGB channel for position detection instead of data from graphic port when DE is '1'. |
| 3-2 | GI_GAINPHS_SEL [1:0] | Graphic Input Gain and Phase Detection Type Select.<br>00 = Phase Tune 1<br>01 = Phase Tune 2<br>10 = Min RGB Gain<br>11 = Max RGB Gain |
| 1 | GI_GAINPHS_EN/ GI_GAINPHS_RDY | Graphic Input Gain and Phase Detection Enable. When GI_GAINPHS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'.<br>0 = Disable<br>1 = Enable |
| 0 | GI_POS_EN/ | Graphic Input Active Window Position Detection Enable. When |

| | | |
|---|---|---|
| | GI_POS_RDY | GI_POS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'.<br>0 = Disable.<br>1 = Enable |

Default: X001 1100B

**Graphic Auto Position**

| 0x107 | | Auto Position Black Threshold | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_POS_THR [7:0] | Graphic data lager then GI_POS_THR will be considered to be non-black pixel for position detecting. | |

Default: 0000 1111B

| 0x108 | | Auto Position Vertical Begin for Odd Field –lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_POS_VBEGO [7:0] | Active Window Vertical Begin for Odd Field. GI_POS_VBEGO= 3 means there are 3 blanking lines. | |

| 0x109 | | Auto Position Vertical Begin for Odd Field –hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | GI_POS_VBEGO [10:8] | MSB of GI_POS_VBEGO | |

| 0x10A | | Auto Position Vertical Begin for Even Field –lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_POS_VBEGE [7:0] | Active Window Vertical Begin for Even Field. GI_POS_VBEGE= 3 means there are 3 blanking lines. | |

| 0x10B | | Auto Position Vertical Begin for Even Field –hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | GI_POS_VBEGE [10:8] | MSB of GI_POS_VBEGE | |

| 0x10C | | Auto Position Vertical Length –lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | GI_POS_VLEN [7:0] | The active window vertical length. GI_POS_VLEN = 3 means there are 3 active lines. | |

| 0x10D | | Auto Position Vertical Length –hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | GI_POS_VLEN [10:8] | MSB of GI_POS_VLEN | |

| 0x10E | | Auto Position Horizontal Begin –lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_POS_HBEG [7:0] | The active window horizontal begin. GI_POS_HBEG = 3 means there are 3 blanking pixels. | |

| 0x10F | | Auto Position Horizontal Begin –hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | GI_POS_HBEG [11:8] | MSB of GI_POS_HBEG | |

| 0x110 | | Auto Position Horizontal Width –lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | GI_POS_HWID [7:0] | The active window horizontal width. GI_POS_HWID = 3 means there are 3 active pixels. | |

| 0x111 | | Auto Position Horizontal Width –hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | GI_POS_HWID [11:8] | MSB of GI_POS_HWID | |

**Graphic Auto Phase and Gain**

| 0x112 | | Auto Phase Bit Mask | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | GI_PHS_MASK [2:0] | Decide how many LSB bits will be masked out, and then the difference between adjacent pixels will be added to the sum of difference accumulator. | |

Default: XXXX X100B

| 0x113 | | Auto Phase Sum of Difference –lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_PHS_SDIFF [7:0] | Auto Phase Sum of Difference (LSB). GI_PHS_SDIFF specifies how the phase locking quality in ADCPLL block. | |
| | R_MINMAX [7:0] | The minimum or maximum value of red channel data in one frame. | |

| 0x114 | | Auto Phase Sum of Difference – 2’nd | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_PHS_SDIFF [15:8] | Second byte of GI_PHS_SDIFF | |
| | G_MINMAX [7:0] | The minimum or maximum value of green channel data in one frame. | |

| 0x115 | | Auto Phase Sum of Difference – 3’rd | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_PHS_SDIFF [23:16] | Third byte of GI_PHS_SDIFF | |
| | B_MINMAX [7:0] | The minimum or maximum value of blue channel data in one frame. | |

| 0x116 | Auto Phase Sum of Difference -hi | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GI_PHS_SDIFF [31:24] | MSB of GI_PHS_SDIFF |

**Graphic Auto Clock**

| 0x117 | Auto Clock Reference Width -lo | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | GI_CLK_REF [7:0] | Auto Clock Reference Width. This register provides the reference value for calibrating the frequency of sampling clock in ADCPLL block. |

Default: 0000 0000B

| 0x118 | Auto Clock Reference Width -hi | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 3-0 | GI_CLK_REF [11:8] | MSB of AUTO_CLK_REF |

Default: XXXX 0000B

| 0x119 | Auto Clock Detecting Result | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-6 | GI_CLK_COMP [1:0] | Auto Clock Comparing Relation. GI_CLK_COMP specifies the comparing relation between GI_POS_HWID and GI_CLK_REF<br>00: GI_POS_HWID = GI_CLK_REF<br>01: GI_POS_HWID < GI_CLK_REF<br>10: GI_POS_HWID > GI_CLK_REF<br>11: Reserved |
| 5-0 | GI_CLK_DIFF [5:0] | Difference of \|GI_POS_HWID - GI_CLK_REF\|<br>The difference value is clamped to 0x3F if difference ≥ 0x3F |

| 0x11A | | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | Reserved |

**Video Auto Tune Control**

| 0x11B | Video Auto Tune Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 5 | VI_AUTO_MASK | Gain Detection Area masking when VI_GAIN_AREA = “1”<br>0 = Detecting area is whole frame<br>1 = Detecting area is defined by mask window registers. |
| 4 | VI_AUTO_HREF | Video auto tune according to YUV_HREF signal<br>0 = Disable<br>1 = Enable |
| 3 | VI_GAIN_AREA | Gain Detection Area Define Enable.<br>0 = Detecting area is over one frame except the area defined by mask window registers.<br>1 = Detecting area is defined by capture registers. |
| 2 | VI_GAIN_SEL | Video Input Gain Type Select<br>0 = Min Y Gain |

| | | |
|---|---|---|
| | | 1 = Max Y Gain |
| 1 | VI_GAIN_EN/ VI_GAIN_RDY | Video Input Y Min/Max Data Detection Enable. When VI_MINMAX_EN = 1, detection will start from next VSYNC.<br>When detection is finished, this bit is cleared to '0'.<br>0 = Disable<br>1 = Enable |
| 0 | VI_POS_EN/ VI_POS_RDY | Video Input Active Window Position Detection Enable. When VI_POS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'.<br>0 = Disable<br>1 = Enable |

Default: XX00 0000B

**Video Auto Position**

| **0x11C** | | **Auto Position Black Threshold** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_POS_THR [7:0] | Video data lager than VI_POS_THR will be considered to be non-black pixel for position detecting. | |

Default: 0000 1111B

| **0x11D** | | **Auto Position Vertical Total -lo** | **R** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_VTOTAL [7:0] | Vertical Period Total. VI_VTOTAL =99 means total 99 lines. | |

| **0x11E** | | **Auto Position Vertical Total -hi** | **R** |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | VI_VTOTAL [10:8] | MSB of VI_VTOTAL. | |

| **0x11F** | | **Auto Position Vertical Begin for Odd Field -lo** | **R** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_POS_VBEGO [7:0] | Active Window Vertical Begin for Odd Field. VI_POS_VBEGO =9 means 9 blanking lines. | |

| **0x120** | | **Auto Position Vertical Begin for Odd Field -hi** | **R** |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | VI_POS_VBEGO [10:8] | MSB of VI_POS_VBEGO. | |

| **0x121** | | **Auto Position Vertical Begin for Even Field -lo** | **R** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_POS_VBEGE [7:0] | Active Window Vertical Begin for Even Field. VI_POS_VBEGE =9 means 9 blanking lines. | |

| **0x122H** | | **Auto Position Vertical Begin for Even Field -hi** | **R** |
|---|---|---|---|
| Bits | Name | Description | |

| | | |
|---|---|---|
| 2-0 | VI_POS_VBEGE [10:8] | MSB of VI_POS_VBEGE. |

| 0x123 | | Auto Position Vertical Length -lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7- 0 | VI_POS_VLEN [7:0] | Active Window Vertical Length. VI_POS_VLEN =99 means 99 active lines. | |

| 0x124 | | Auto Position Vertical Length -hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | VI_POS_VLEN [10:8] | MSB of VI_POS_VLEN. | |

Default:

| 0x125 | | Auto Position Horizontal Total -lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_HTOTAL [7:0] | Horizontal Period Total. VI_HTOTAL=99, means total 99 pixels. | |

Default:

| 0x126 | | Auto Position Horizontal Total -hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | VI_HTOTAL [11:8] | MSB of VI_HTOTAL. | |

Default:

| 0x127 | | Auto Position Horizontal Begin -lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_POS_HBEG [7:0] | Active Window Horizontal Begin. VI_POS_HBEG =3 means 3 blanking pixels. | |

Default:

| 0x128 | | Auto Position Horizontal Begin -hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | VI_POS_HBEG [11:8] | MSB of VI_POS_HBEG | |

Default:

| 0x129 | | Auto Position Horizontal Width -lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VI_POS_HWID [7:0] | Active Window Horizontal Width. VI_POS_HWID =99 means 99 active pixels. | |

Default:

| 0x12A | | Auto Position Horizontal Width -hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | VI_POS_HWID [11:8] | MSB of VI_POS_HWID | |

**Video Auto Gain**

| 0x12B | Video Min/Max Y Value | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | Y_MINMAX [7:0] | The minimum or maximum value of Y channel data in one frame. |

| 0x12C~0x12F | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | Reserved |

## 9.22. Bright Frame Display Registers

**Bright Frame Control**

Note--When both Bright Frames are enabled and if two windows are overlapped frame2 has higher priority than frame 1.

| 0x130 | Bright Frame Enable Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-5 | | |
| 4 | BRIGHT_REF_CTL | Bright Frame Active reference<br>0: Front (Capture)<br>1: Post (Display) |
| 3-2 | | Reserved |
| 1 | BRIGHT_FRM2_EN | Enable Bright Frame 2<br>0: Disable<br>1: Enable |
| 0 | BRIGHT_FRM1_EN | Enable Bright Frame 1<br>0: Disable<br>1: Enable |

Default: XXXX XX00B

| 0x131 | Bright Frame access index Select | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-1 | | Reserved |
| 0 | BRIGHT_FRM_SEL [0] | This register is used to select which frame is to be accessed or modified. It is programmed prior to accessing the registers Reg 0x132 ~ 0x13B<br>“0” = Bright Frame 1 “1” = Bright Frame 2 |

Default: XXXX XXX0B

| 0x132 | Bright Frame Horizontal Start - Low byte | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | BRIGHT_FRM_HS [7:0] | Bright Frame horizontal start low byte [7:0]. Specifies the horizontal starting position of the Bright Frame in pixel units. This register is **double-buffered**. |

Default: 0000 0000B

| 0x133 | Bright Frame Horizontal Start - High Byte | R/W |
|---|---|---|
| Bits | Name | Description |

| | | |
|---|---|---|
| 7-4 | | Reserved |
| 3-0 | BRIGHT_FRM_HS [11:8] | Bright Frame horizontal start high byte [11:8]. Specifies the horizontal starting position of the Bright Frame in pixel units. This register is **double-buffered**. |

Default: XXXX 0000B

| **0x134** | | **Bright Frame Horizontal Width - Low byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BRIGHT_FRM_HW [7:0] | Bright Frame horizontal Width low byte [7:0]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**. | |

Default: 0000 0000B

| **0x135** | | **Bright Frame Horizontal Width – High byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | | Reserved | |
| 3-0 | BRIGHT_FRM_HW [11:8] | Bright Frame horizontal Width low byte [11:8]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**. | |

Default: XXXX 0000B

| **0x136** | | **Bright Frame Vertical Start - Low byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BRIGHT_FRM_VS [7:0] | Bright Frame vertical start low byte [7:0]. Specifies the vertical starting position of the Bright Frame in pixel units. This register is **double-buffered**. | |

Default: 0000 0000B

| **0x137** | | **Bright Frame Vertical Start - High Byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | | Reserved | |
| 3-0 | BRIGHT_FRM_VS [10:8] | Bright Frame vertical start high byte [10:8]. Specifies the vertical starting position of the Bright Frame in pixel units. This register is **double-buffered**. | |

Default: XXXX 0000B

| **0x138** | | **Bright Frame Vertical Height - Low byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BRIGHT_FRM_VH [7:0] | Bright Frame vertical Width low byte [7:0]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**. | |

Default: 0000 0000B

| **0x139** | | **Bright Frame Vertical Height – High byte** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | | Reserved | |
| 2-0 | BRIGHT_FRM_VH [10:8] | Bright Frame vertical Width low byte [10:8]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**. | |

Default: XXXX X000B

| **0x13A** | | **Bright Frame Gain Control** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BRIGHT_FRM_GAIN | Bright Frame gains adjusting | |

Default: 1000 0000B

| 0x13B | | Bright Frame Offset Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | BRIGHT_FRM_OFFSET | Bright Frame offsets adjusting | |

Default: 0000 0000B

| 0x13C~0x13E | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| | | | |

Default: 0000 0000B

## 9.23. DVI Input Control 2

| 0x13F | | DVI Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| 0x140 | | DVI Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| 0x141 | | DVI Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| 0x142 | | DVI Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| 0x143 | | DVI Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | TMDS_PLL_PD | TMDS PLL power down control | |
| 6 | TMDS_VCO_5X | TMDS PLL VCO 5X mode | |
| 5-4 | TMDS_LCPC | TMDS PLL lower charge pump current | |
| 3-1 | TMDS_VCO_SV | Control reference swing voltage of TMDS PLL VCO | |
| 0 | PMOS_RES_EN | PMOS resistor enable | |

Default: 0000 0000B

| 0x144 | | DVI Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-1 | | | |
| 0 | TMDS_IPDS_PD | Power down control of three channel impedances | |

Default: 0000 0000B

| 0x145 | | DVI Control | R/W |
|---|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

Default: 0000 0000B

| 0x146 | DVI Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

Default: 0000 0000B

| 0x147 | DVI Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

Default: 0000 0000B

| 0x148 ~ 0x149 | Reserved | R/W |
|---|---|---|

| 7-0 | | Reserved |
|---|---|---|

Default: 0000 0000B

## 9.24. Display Port Control

- Display timing control
- Single pixel or dual pixel output
- Output signals drive current and slew rate control
- Phase delay adjustment for accessing clock to external LCD
- Dithering function supports 24-bit quality for 18-bit panel
- Mute display control

**Display Video Special mode Control**

| 0x14C | Reserved | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | |

| 0x14D | Reserved | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 3-0 | | |

| 0x14E | Reserved | R/W |
|---|---|---|

| 7-0 | | Reserved |
|---|---|---|

Default: 0000 0000B

| 0x14F | Reserved | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | | Reserved |

Default: XXXX 0000B

**Display General Control**

| 0x150 | Display Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|

| | | |
|---|---|---|
| 7 | DP_BIT_SHF | When display bus is 6-bit/color, this bit enable will shift the data RA[7:2], GA[7:2], BA[7:2] to RA[5:0], GA[5:0], BA[5:0] and RB[7:2], GB[7:2], BB[7:2] to RB[5:0], GB[5:0], BB[5:0]. When display bus is 8-bit/color, this bit enable will rotate the data RA[7:0], GA[7:0], BA[7:0] and RB[7:0], GB[7:0], BB[7:0] to right 2 bits<br>0 = Normal<br>1 = Shift / Rotate |
| 6 | | Reserved |
| 5 | | Reserved |
| 4 | | Reserved |
| 3 | DP_COLDEP | Display Color Depth<br>0 = 8-bit/color<br>1 = 6-bit/color |
| 2 | DP_BUSWID | Display Bus Width<br>0 = Double pixel 48-bit<br>1 = Single pixel 24-bit |
| 1 | DP_DE | Panel supports DE mode<br>0 = Panel supports Sync mode, display Hs/Vs signal is at normal state<br>1 = Panel supports DE mode, display Hs/Vs signal will be pulled low |
| 0 | DP_EN | Display Enable<br>0 = Disable. Tri-state control lines and data lines.<br>1 = Enable |

Default: 011X 0000B

| **0x151** | | **Reserved** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| **0x152** | | **Reserved** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| **0x153** | | **Reserved** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | | | |

Default: XXXX 0000B

| **0x154** | | **Display Mute and Color Control** | **R/W** |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | DP_PATT [3:0] | Select built-in display pattern<br>Pattern number = 0~15<br><br>If PATT_BK = Bank 0<br>0000 = Gamma Correction pattern<br>0001 = Dot Moiré<br>0010 = Vertical Line Moire (1B1W)<br>0011 = Vertical Line Moire (2B1W)<br>0100 = Vertical Line Moire (2B2W) | |

| | | |
|---|---|---|
| | | 0101 = 256 V_Gray Bar<br>0110 = 256 H_Gray Bar<br>0111 = Horizontal Line Moire (1B1W)<br>1000 = Horizontal Line Moire (2B1W)<br>1001 = Horizontal Line Moire (2B2W)<br>1010 = Chat Pattern<br>1011 = White Pattern<br>11xx = Rectangular pattern, outline width is defined by xx bits.<br>00 = 1 pixel<br>01 = 3 pixels<br>10 = 5 pixels<br>11 = 7 pixels<br><br>If PATT_BK = Bank 1<br>0000 = Black pattern<br>0001~1111 = Reserved |
| 3 | PATT_BK | Built-in pattern bank Select<br>0 = Bank 0<br>1 = Bank 1 |
| 2 | CBAR_EN | Paste a Cross Bar on the built-in display pattern and the Bar's gray level is controlled via CBAR_FG[7:0] register (0x15A)<br>0 = Disable<br>1 = Enable |
| 1-0 | DP_MUTE [1:0] | Display Mute Mode Select<br>00 = Normal display, RGB channel output controlled via DP_RGB<br>01 = Mute input with output built-in display pattern, pattern color decided by DP_RGB registers. (Display free-run)<br>10 = Mute input with output OSD and background color, background color decided by DP_BG_R/G/B registers. (Display free-run)<br>11 = Pull low all display signals including data, clock and control lines |

Default: 0000 0000B

| **0x155** | **Display Drive Control** | **R/W** |
|---|---|---|
| Bits | Name | Description |
| 7 | DCLK_SLEW | Select panel interface CLOCK slew rate<br>0: Fast<br>1: Slow |
| 6-4 | DCLK_DRV [2:0] | Select panel interface CLOCK drive strength<br>000: 2mA 100: 10mA<br>001: 4mA 101: 12mA<br>010: 6mA 110: 14mA<br>011: 8mA 111: 16mA |
| 3 | DOUT_SLEW | Select panel interface DATA slew rate<br>0: Fast<br>1: Slow |
| 2-0 | DOUT_DRV [2:0] | Select panel interface DATA drive strength<br>000: 2mA 100: 10mA<br>001: 4mA 101: 12mA<br>010: 6mA 110: 14mA<br>011: 8mA 111: 16mA |

Default: 0100 0011B

| 0x156 | | Display Drive and Polarity Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | DDE_POL | Display DE<br>1 = Active High<br>0 = Active Low | |
| 6 | DCLK_POL | Display Clock<br>0 = Normal<br>1 = Inverted | |
| 5 | DHS_POL | Display Hsync<br>1 = Active High<br>0 = Active Low | |
| 4 | DVS_POL | Display Vsync<br>1 = Active High<br>0 = Active Low | |
| 3 | DCTRL_SLEW | Select panel interface HS/VS/DE slew rate<br>0 = Fast<br>1 = Slow | |
| 2-0 | DCTRL_DRV [2:0] | Select panel interface HS/VS/DE drive strength<br>000 = 2mA 100 = 10mA<br>001 = 4mA 101 = 12mA<br>010 = 6mA 110 = 14mA<br>011= 8mA 111 = 16mA | |

Default: 1011 0010B

| 0x157 | | Display Clock and Data Delay Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | DOUT_STAG | When dual-pixel/clock display output is enabled, staggering output format is supported to reduce the ground bounce that affects EMI.<br>0 = Normal<br>1 = Stagger | |
| 6-5 | DCLK_SYNC_SEL | Display clock synchronous mode select<br>00 = Display clock free-run<br>01 = Display clock is synchronized to input(default by TCON enable)<br>10 = Display clock free-run and DISP_DE synchronized to DISP_CLK<br>11 = Reserved | |
| 4-0 | DCLK_DLY [4:0] | Select panel interface CLOCK delay time. (0.5nS/step)<br>0~32 step | |

Default: 0010 0000B

| 0x158 | | Display Dithering Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | | Delay data transition time from 4 frame to 16 frame | |
| 6 | | Separate G-channel data to do dithering function | |
| 5-4 | DITH_MODE [1:0] | Dithering mode select | |
| 3 | | Reserved | |
| 2 | DITH_8BIT | Rounded 10 bit gamma data output to 8 bit for dithering<br>0 = Disable | |

| | | |
|---|---|---|
| | | 1 = Enable 8 Bit dithering |
| 1 | DITH_TURBO | |
| 0 | DITH_EN | Dithering enable. When DITH_EN =0, the LSB bits of display data will be truncated if display color depth is less than internal data resolution.<br>0 = Disable<br>1 = Enable |

Default: 0000 0000B

| 0x159 | Display Channel Select | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | INT_FAST_EN | Mute mode with Free Run timing when graphic input sync fail<br>0: Disable<br>1: Enable |
| 6-4 | | Reserved |
| 3 | MUTE_FR_EN | Mute mode with Free Run timing Enable<br>0: Disable<br>1: Enable |
| 2-0 | DP_RGB [2:0] | Select RGB channel for display<br>000 = RGB normal display<br>001 = R channel only<br>010 = G channel only<br>011 = B channel only<br>100 = R & G channels<br>101 = R & B channels<br>110 = G & B channels<br>111 = RGB inverted display |

Default: 00XX X000B

| 0x15A | Cross Bar Gray Level | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | CBAR_FG [7:0] | Select the foreground gray level of Cross Bar for burn-in display pattern.<br>R=G=B= 0~255 |

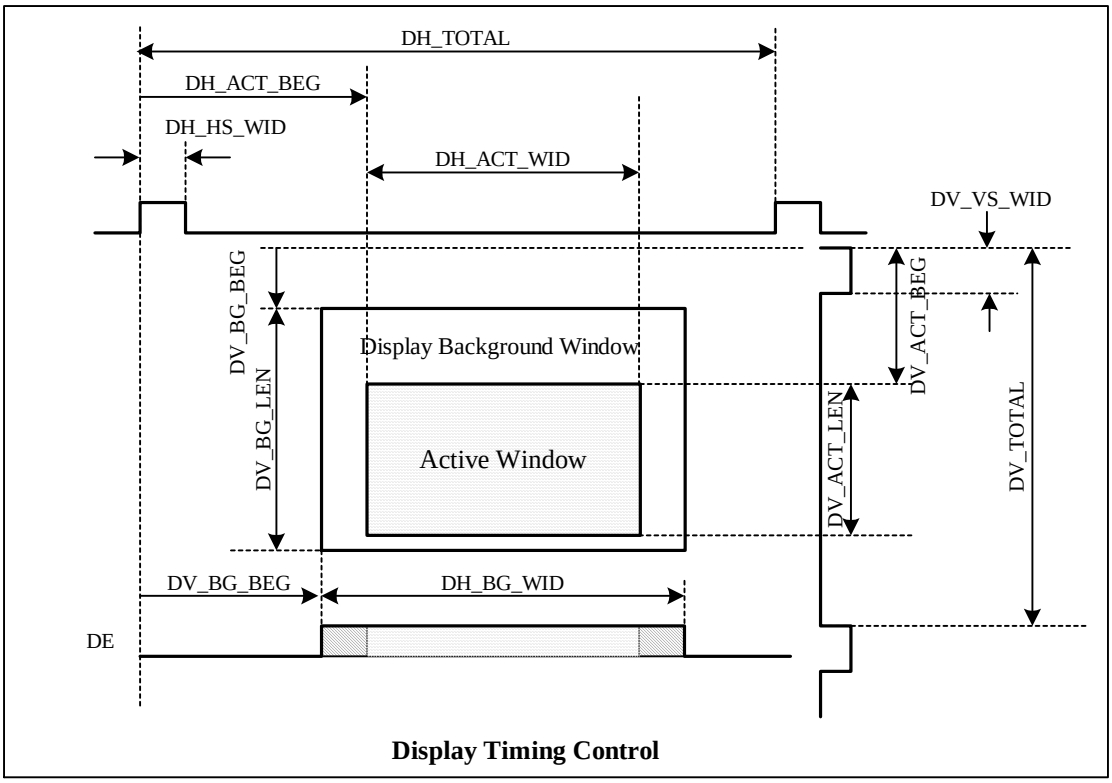



**Figure 9.24-1 Display Timing**

**Display Sync Timing Control**

| 0x15B | | Display Vertical Total –lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DV_TOTAL [7:0] | Display Vertical Total Lines.<br>DV_TOTAL = 3 means there are 4 total lines. | |

Default: 0000 0000B

| 0x15C | | Display Vertical Total –hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | DV_TOTAL [10:8] | MSB of DV_TOTAL | |

Default: XXXX X000B

| 0x15D | | Display VSYNC Pulse Width | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DV_VS_WID [7:0] | Display VSYNC Pulse Width. DV_VS_WID =3, means pulse width is 3 lines wide. | |

Default: 0000 0000B

| 0x15E | | Display Horizontal Total –lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DH_TOTAL [7:0] | Display Horizontal Total Pixels.<br>DH_TOTAL = 3 means there are 4 total pixels. | |

Default: 0000 0000B

| 0x15F | Display Horizontal Total –hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 3-0 | DH_TOTAL [11:8] | MSB of DH_TOTAL |

Default: XXXX 0000B

| 0x160 | Display HSYNC Pulse Width | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | DH_HS_WID [7:0] | Display HSYNC Pulse Width. DH_HS_WID =3, means pulse width is 3 pixels wide. |

Default: 0000 0000B

| 0x161H | | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | Reserved |

**Display Background Window Control**

| 0x162 | Display Background Window Vertical Begin –lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | DV_BG_BEG [7:0] | Display Background Window Vertical Begin. DV_BG_BEG indicates how many lines to wait after DVSYNC leading edge before starting image display. DV_BG_BEG =3, means waiting 3 lines to begin display. |

Default: 0000 0000B

| 0x163 | Display Background Window Vertical Begin –hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 2-0 | DV_BG_BEG [10:8] | MSB of DV_BG_BEG |

Default: XXXX X000B

| 0x164 | Display Background Window Vertical Length –lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | DV_BG_LEN [7:0] | Display Background Window Vertical Length. DV_BG_LEN indicates how many lines to display. DV_BG_LEN =3, means displaying 3 lines. |

Default: 0000 0000B

| 0x165 | Display Background Window Vertical Length –hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 2-0 | DV_BG_LEN [10:8] | MSB of DV_BG_LEN |

Default: XXXX X000B

| 0x166 | Display Background Window Horizontal Begin –lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | DH_BG_BEG [7:0] | Display Background Window Horizontal Begin. DH_BG_BEG indicates how many pixels to wait after DHSYNC leading edge before starting image display. DH_BG_BEG =3, means waiting 3 pixels to begin display. |

Default: 0000 0000B

| 0x167 | | Display Background Window Horizontal Begin –hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | DH_BG_BEG [11:8] | MSB of DH_BG_BEG | |

Default: XXXX 0000B

| 0x168 | | Display Background Window Horizontal Width –lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DH_BG_WID [7:0] | Display Background Window Horizontal Width. DV_BG_WID indicates how many pixels to display. DV_BG_WID =3, means displaying 3 pixels. | |

Default: 0000 0000B

| 0x169 | | Display Background Window Horizontal Width –hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | DH_BG_WID [11:8] | MSB of DH_BG_WID | |

Default: XXXX 0000B

| 0x16A | | | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-5 | | Reserved | |
| 4 | DP_PORT_SWAP | A /B Port Swap Control<br>0: Normal<br>1: A/B Port Swap | |
| 3 | DP_BYTE_SWAPB | Display Bus Port B Byte Swap Control<br>0: Normal<br>1: B Port R/B Channel Byte Swap | |
| 2 | DP_BYTE_SWAPA | Display Bus Port A Byte Swap Control<br>0: Normal<br>1: A Port R/B Channel Byte Swap | |
| 1 | DP_BIT_SWAPB | Display Bus Port B Bit Swap Control<br>0: Normal<br>1: B Port Bit Swap | |
| 0 | DP_BIT_SWAPA | Display Bus Port A Bit Swap Control<br>0: Normal<br>1: Port A Bit Swap (RGB bit7~bit0 in 8 bit Mode, bit5~bit0 in 6 bit Mode) | |

Default: XXX0 0000B

**Display Background Color Control**

| 0x16B | | Display Background Color - Red | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DP_BG_R [7:0] | Display Background Window Red Color. | |

Default: 0000 0000B

| 0x16C | | Display Background Color - Green | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | DP_BG_G [7:0] | Display Background Window Green Color. | |

Default: 0000 0000B

| 0x16D | Display Background Color - Blue | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | DP_BG_B [7:0] | Display Background Window Blue Color. |

Default: 0000 0000B

**Graphic Display Active Window Control**

| 0x16E | Graphic Display Window Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | | Reserved |
| 6 | GD_PRIO | When Graphic Display and Video Display are both enabled, the priority decides which one has higher priority to display for image overlap area.<br>0 = Graphic<br>1 = Video |
| 5 | GD_FRM_INV | Select the frame signal polarity to display for alternate sampling mode<br>0 = Normal<br>1 = Invert |
| 4 | GD_DEALT_SP | Spatial de-alternating mode enable<br>0 = Disable<br>1 = Enable |
| 3 | GD_DEALT | Display de-alternating function enable<br>0 = Disable<br>1 = Enable |
| 2-1 | GD_FLD [1:0] | Select the field to display for interlaced graphic input<br>00 = Display both odd and even field mode<br>01 = Display only odd field mode<br>10 = Display only even field mode<br>11 = Spatial Interpolation mode |
| 0 | GD_EN | Graphic Display Window Enable<br>0 = Disable<br>1 = Enable |

Default: X000 0110B

| 0x16F | Graphic Display Active Window Vertical Begin –lo | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | GDV_ACT_BEG [7:0] | Graphic Display Active Window Vertical Begin. GDV_ACT_BEG indicates how many lines to wait after DVSYNC leading edge before starting graphic image display. GDV_BG_BEG =3, means waiting 3 lines to begin display. |

Default: 0000 0000B

| 0x170 | Graphic Display Active Window Vertical Begin –hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 2-0 | GDV_ACT_BEG [10:8] | MSB of GDV_ACT_BEG |

Default: XXXX X000B

| 0x171 | Graphic Display Active Window Vertical Length –lo | R/W |
|---|---|---|
| Bits | Name | Description |

| | | |
|---|---|---|
| 7-0 | GDV_ACT_LEN [7:0] | Graphic Display Active Window Vertical Length. GDV_ACT_LEN indicates how many lines to display. GDV_ACT_LEN =3, means displaying 3 lines. |

Default: 0000 0000B

| 0x172 | | Graphic Display Active Window Vertical Length –hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | GDV_ACT_LEN [10:8] | MSB of GDV_ACT_LEN | |

Default: XXXX X000B

| 0x173 | | Graphic Display Active Window Horizontal Begin –lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GDH_ACT_BEG [7:0] | Graphic Display Active Window Horizontal Begin. GDH_ACT_BEG indicates how many pixels to wait after DHSYNC leading edge before starting graphic image display. GDH_ACT_BEG =3, means waiting 3 pixels to begin display. | |

Default: 0000 0000B

| 0x174 | | Graphic Display Active Window Horizontal Begin –hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | GDH_ACT_BEG [11:8] | MSB of GDH_ACT_BEG | |

Default: XXXX 0000B

| 0x175 | | Graphic Display Active Window Horizontal Width –lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GDH_ACT_WID [7:0] | Graphic Display Active Window Horizontal Width. GDH_ACT_WID indicates how many pixels to display. GDH_ACT_WID =3, means displaying 3pixels. | |

Default: 0000 0000B

| 0x176 | | Graphic Display Active Window Horizontal Width –hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | GDH_ACT_WID [11:8] | MSB of GDH_ACT_WID | |

Default: XXXX 0000B

| 0x177 | | Reserved | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

| 0x178 | | Reserved | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-4 | | | |
| 3-0 | | | |

**Free Run Htotal Control**

| 0x179 | | Free Run Horizontal Total –lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |

| | | |
|---|---|---|
| 7-0 | FRH_TOTAL [7:0] | Free Run Horizontal Total Pixels.<br>DH_TOTAL = 3 means there are 4 total pixels. |

Default: 0000 0000B

| 0x17A | Free Run Horizontal Total –hi | R/W |
|---|---|---|
| Bits | Name | Description |
| 3-0 | FRH_TOTAL [11:8] | MSB of DH_TOTAL |

Default: XXXX 0000B

| 0x17B~0x181 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

Default: 0000 0000B

**Auto Control H-total Read Back**

| 0x182 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

| 0x183 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 3-0 | | |

**Residual Display HSYNC Control**

| 0x184 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

| 0x185 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 3-0 | | |

| 0x186 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| 4 | | |
| 3-2 | | |
| 1 | | |
| 0 | | |

Default: XXX0 0000B

| 0x187 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| | | |

Default: 0000 0000B

| 0x188 | | VCR Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 4 | SC_MUTE_DIS | Scaler mute disable | |
| 3-1 | | | |
| 0 | VCR_EN | VCR input mode enable control<br>0 = Disable<br>1 = Enable | |

Default: 0000 0000B

| 0x189 | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| 0x18A | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | | | |

Default: XXXX 0000B

| 0x18B | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | | | |

Default: 0000 0000B

| 0x18C | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 3-0 | | | |

Default: XXXX 0000B

| 0x18D | | Residual DHS Average Increment | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 5 | | | |
| 4 | DHS_H_PORCH_SEL | Residual Display HSYNC Area Select<br>0 = Front Porch<br>1 = Back Porch | |
| 3-2 | DHS_TOTAL_SELECT [1:0] | Force Htotal control<br>00 = default auto Htotal<br>01 = force odd Htotal<br>10 = force even Htotal | |
| 1-0 | DHS_DIST_LEN [1:0] | When DHS_DIST = 10, this register indicates the increment value for average.<br>00 = 1-pixel<br>01 = 2-pixel<br>10 = 3-pixel<br>11 = 4-pixel | |

Default: XXX0 0000B

**FIFO Over/Under-flow Interrupt**

| 0x18E | FIFO Interrupt Flag | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 1 | INT_FFOV | FIFO over-flow interrupt flag |
| 0 | INT_FFUN | FIFO under-flow interrupt flag |

| 0x18E | FIFO Interrupt Flag Clear | W |
|---|---|---|
| Bits | Name | Description |
| 1 | CLR_FFOV | Writing '1' will clear INT_FFOV flag |
| 0 | CLR_FFUN | Writing '1' will clear INT_FFUN flag |

Default: XXXX XX00B

| 0x18F | FIFO Interrupt Enable | R/W |
|---|---|---|
| Bits | Name | Description |
| 1 | INT_FFOV_EN | FIFO over-flow interrupt enable |
| 0 | INT_FFUN_EN | FIFO under-flow interrupt enable |

Default: XXXX XX00B

| 0x190 | FIFO Control 1 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-5 | | |
| 4 | FIFO_TEST | |
| 3 | | |
| 2 | GR_VD_CLK_POL | 0 = Normal<br>1 = Inverted |
| 1 | GR_UP_CLK_POL | 0 = Normal<br>1 = Inverted |
| 0 | GR_BK_CLK_POL | 0 = Normal<br>1 = Inverted |

Default: 0000 0000B

| 0x191 | FIFO Control 2 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | BP_VI | Bypass the VI data and power down the clock |
| 6 | BP_HI | Bypass the HI data and power down the clock |
| 5 | BP_SRGB | Bypass the SRGB data and power down the clock |
| 4 | BP_VC | Bypass the VC data and power down the clock |
| 3 | BP_HC | Bypass the HC data and power down the clock |
| 2 | GR_AUTO_CLK | FIFO reference clock control auto select enable<br>0 = Disable<br>1 = Enable |
| 1-0 | GR_FIFO_CLK_SEL [1:0] | FIFO reference clock control source select<br>00 = Graphic clock<br>01 = Video clock<br>10 =<br>11 = |

Default: 0000 0100B

| 0x192 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

| 0x193 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 7-4 | | Reserved |
| 3-0 | | |

| 0x194 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 7-0 | | |

| 0x195 | Reserved | R |
|---|---|---|
| Bits | Name | Description |
| 7-4 | | Reserved |
| 3-0 | | |

## 9.25. Sync Processor

- H/V sync frequency counter & polarity detection
- H/V sync frequency change detection
- Composite/separate auto-switch
- Interlaced/progressive input detection
- Programmable free-run H/V frequency
- Status change interrupt

**Graphic Sync Processor Control**

| 0x196 | Graphic SYNC Processor Control 1 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | DVI_SYNC_SEL | Select the SYNC input source when DVI interface is enabled.<br>0 = From DVI DE signal<br>1 = From DVI HS/VS signal |
| 6 | GI_ADCHS_INV | Invert the ADC_HS polarity<br>0 = Normal<br>1 = Invert |
| 5-4 | GI_HS_SRC [1:0] | Select the HSYNC input source to sync processor and core logic.<br>00 = ADC_HS -> sync processor and core logic<br>01 = RAW_HS -> sync processor and core logic<br>10 = RAW_HS -> sync processor and ADC_HS -> core logic<br>11 = SOG_HS-> sync processor and core logic |
| 3-2 | GI_VCNT_BIT [1:0] | Select the bit number of GI_VCNT.<br>00 = 11-bit. Overflow freq = 27.32Hz<br>01 = 12-bit. Overflow freq = 13.66Hz<br>1X = 13-bit. Overflow freq = 6.83Hz |

| | | |
|---|---|---|
| 1-0 | GI_SYNC_TYPE [1:0] | Graphic sync type select.<br>00 = Separate SYNC<br>01 = Composite SYNC<br>1X = Auto detection and switch |

Default: 00010110B

| 0x197 | Graphic SYNC Processor Control 2 | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | COAST_EN | COAST output enable for ADCPLL free run<br>0 = Disable<br>1 = Enable |
| 6 | SYNC_OUT_SEL [0] | Internal SYNC signal selection |
| 5 | GI_VRUN_EN | VSYNC output free run enable<br>0 = Disable<br>1 = Enable |
| 4 | GI_HRUN_EN | HSYNC output free run enable<br>0 = Disable<br>1 = Enable |
| 3 | GI_VSO_POL | VSYNC output polarity control<br>0 = Active low<br>1 = Active high |
| 2 | GI_HSO_POL | HSYNC output polarity control<br>0 = Active low<br>1 = Active high |
| 1 | GI_VSO_EN | VSYNC output enable<br>0 = Disable<br>1 = Enable |
| 0 | GI_HSO_EN | HSYNC output enable<br>0 = Disable<br>1 = Enable |

Default: 1000 1111B

**Interlace Detector Control**

| 0x198 | Graphic Field Decision Window | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-4 | GI_FLD_WINEDN [3:0] | Define the end position of graphic field decision window. |
| 3-0 | GI_FLD_WINBEG [3:0] | The G_HS period is divided into 16 segments; a field decision window is defined by GI_FLD_WINBEG and GI_FLD_WINEND. GI_FLD_WINBEG defines the window begin position, and GI_FLD_WINEND defines the end position. If the G_VS reference edge locates inside the window, it means ODD field. |

Default: 0100 1100B

| 0x199 | Graphic SYNC Processor Control 3 | R/W |
|---|---|---|
| Bits | Name | Description |
| 6 | SYNC_OUT_SEL [1] | Internal SYNC signal selection<br>0 = Disable<br>1 = Enable |

| | | |
|---|---|---|
| 5 | HSYNC_CNT_MOD | Hsync period counter measurement mode.<br>0 = Counter mode<br>1 = Time mode |
| 4-2 | | Reserved |
| 1 | GI_FLD_EDGE | Select the reference edge of VSYNC in Graphic Field Detector<br>0 = Leading edge<br>1 = Trailing edge |
| 0 | GI_FLD_INV | Invert the polarity of Graphic Field Detector output signal<br>0 = Normal<br>1 = Invert |

Default: 00XX XX00B

**Sync Status**

| **0x19A** | **Graphic Sync Processor Status** | **R** |
|---|---|---|
| Bits | Name | Description |
| 7 | GI_VCNT_OV | GI_VCNT overflow flag<br>0 = Non-overflow<br>1 = Overflow |
| 6 | GI_HCNT_OV | GI_HCNT overflow flag<br>0 = Non-overflow<br>1 = Overflow |
| 5 | GI_CSPRE | Composite SYNC present flag<br>0 = Non-present<br>1 = Present |
| 4 | GI_VPRE | VSYNC present flag<br>0 = Non-present<br>1 = Present |
| 3 | GI_HPRE | HSYNC present flag<br>0 = Non-present<br>1 = Present |
| 2 | GI_INTE | Interlace input detected flag<br>0 = Progressive input<br>1 = Interlaced input |
| 1 | GI_VPOL | VSYNC polarity<br>0 = Active low<br>1 = Active high |
| 0 | GI_HPOL | HSYNC polarity<br>0 = Active low<br>1 = Active high |

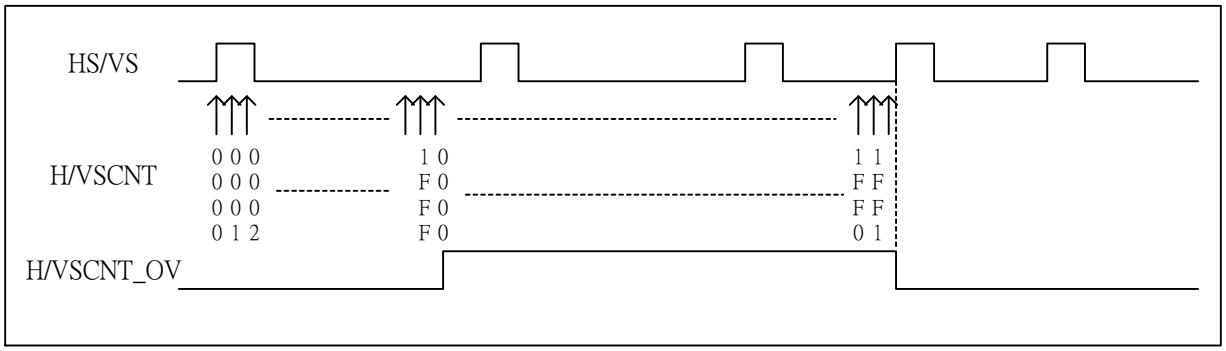



**Figure 9.25-1**

**H/V Sync Counter**

| 0x19B | | Graphic HSYNC Counter -lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_HCNT [7:0] | Hsync period counter. GI_HCNT is the number of clock (=REFCLK/4) in the period of 32x HSYNC.<br>Hfreq = (REFCLK x 32)/(4 x GI_HCNT) Hz | |

| 0x19C | | Graphic HSYNC Counter -hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 4-0 | GI_HCNT [12:8] | MSB of GI_HCNT | |

| 0x19D | | Graphic VSYNC Counter -lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_VCNT [7:0] | Vsync period counter. GI_VCNT is a 12-bit counter; counter value is the number of clock (=REFCLK/256) between two VSYNC pulses.<br>Vfreq = REFCLK/(256 x GI_VCNT) | |

| 0x19E | | Graphic VSYNC Counter -hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 4-0 | GI_VCNT [12:8] | MSB of GI_VCNT. | |

**H/V Free Run Divider**

| 0x19F | | HSO Free Run Divider -lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HFREE_DIV [7:0] | HSYNC output free-run divider value. HSYNC pulse width = 15x REFCLK<br>Hfreq (free-run) = REFCLK/(HFREE_DIV+1)<br>0~511 | |

Default: 0010 0111B

| 0x1A0 | | HSO Free Run Divider -hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 0 | HFREE_DIV [8] | MSB of HFREE_DIV | |

Default: XXXX XXXX1B

| 0x1A1 | | VSO Free Run Divider -lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | VFREE_DIV [7:0] | VSYNC output free-run divider value. VSYNC pulse width = 3x HFREE<br>Vfreq (free-run) = Hfreq (free-run)/ (VFREE_DIV+1)<br>0~2048 | |

Default: 0010 0110B

| 0x1A2 | | VSO Free Run Divider -hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | VFREE_DIV [10:8] | MSB of VFREE_DIV | |

Default: XXXX X011B

**H/V Present Threshold**

| 0x1A3 | | HSYNC Present Low Count Threshold | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 6-0 | HPRE_THR_LO [6:0] | Hsync non-present counter threshold<br>1 (0H)~127 (7EH)<br>Not-present when Hfreq < REFCLK / (4 x 8192 x HPRE_THR_LO) Hz | |

Default: X010 1101B

| 0x1A4 | | HSYNC Present High Count Threshold | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 6-0 | HPRE_THR_HI [6:0] | Hsync present counter threshold<br>1 (0H)~127 (7EH)<br>Present when Hfreq > REFCLK / (4 x 8x HPRE_THR_HI) Hz | |

Default: X010 1100B

| 0x1A5 | | VSYNC Present Low Count Threshold | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 6-0 | VPRE_THR_LO [6:0] | Vsync non-present counter threshold<br>1 (0H)~127 (7EH)<br>Not-present when Vfreq < REFCLK / (4 x 8192 x VPRE_THR_LO) Hz | |

Default: X010 1100B

| 0x1A6 | | VSYNC Present High Count Threshold | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 6-0 | VPRE_THR_HI [6:0] | Vsync present counter threshold<br>1 (0H)~127 (7EH)<br>Present when Vfreq > REFCLK / (4 x 2048x VPRE_THR_HI) Hz | |

Default: X010 1100B

**H/V Frequency Change Threshold**

| 0x1A7 | | HSYNC Freq Change Threshold | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | HCNT_THR [7:0] | HSYNC counter value change threshold for mode change detection.<br>1~256 | |

Default: 0000 0000B

| 0x1A8 | | VSYNC Freq Change Threshold | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-5 | H_CHANG_CNT | The INT_HFREQ will occur if the times out of HSYNC frequency change time are more than CHANG_CNT setting.<br>000~111: 1, 4, 8, ~ 28 times | |
| 4-0 | VCNT_THR [4:0] | VSYNC counter value change threshold for mode change detection.<br>1~32 | |

Default: 0000 0000B

**Interrupt Control**

| 0x1A9 | | SYNC Interrupt Enable 1 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | INT_INV | Invert the polarity of IRQn output signal<br>0 = Normal<br>1 = Invert | |
| 5 | INT_VFREQ_EN | VSYNC frequency change interrupt enable<br>0 = Disable<br>1 = Enable | |
| 4 | INT_HFREQ_EN | HSYNC frequency change interrupt enable<br>0 = Disable<br>1 = Enable | |
| 3 | INT_VPOL_EN | VSYNC polarity change interrupt enable<br>0 = Disable<br>1 = Enable | |
| 2 | INT_HPOL_EN | HSYNC polarity change interrupt enable<br>0 = Disable<br>1 = Enable | |
| 1 | INT_VEDGE_EN | VSYNC rising edge occur interrupt enable<br>0 = Disable<br>1 = Enable | |
| 0 | INT_HEDGE_EN | HSYNC rising edge occur interrupt enable<br>0 = Disable<br>1 = Enable | |

Default: 0000 0000B

| 0x1AA | | SYNC Interrupt Enable 2 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 4 | INT_DVIPRE_EN | DVI SYNC present or non-present interrupt enable<br>0 = Disable<br>1 = Enable | |
| 3 | INT_ISPRE_EN | Interlaced SYNC present or non-present interrupt enable<br>0 = Disable<br>1 = Enable | |
| 2 | INT_CSPRE_EN | Composite SYNC present or non-present interrupt enable<br>0 = Disable<br>1 = Enable | |
| 1 | INT_VPRE_EN | VSYNC present or non-present interrupt enable<br>0 = Disable<br>1 = Enable | |
| 0 | INT_HPRE_EN | HSYNC present or non-present interrupt enable | |

| | | |
|---|---|---|
| | | 0 = Disable<br>1 = Enable |

Default: XXX0 0000B

| 0x1AB | | SYNC Interrupt Flag 1 | R |
|---|---|---|---|
| Bits | Name | Description | |
| 5 | INT_VFREQ | VSYNC frequency change interrupt | |
| 4 | INT_HFREQ | HSYNC frequency change interrupt | |
| 3 | INT_VPOL | VSYNC polarity change interrupt | |
| 2 | INT_HPOL | HSYNC polarity change interrupt | |
| 1 | INT_VEDGE | VSYNC rising edge occur interrupt | |
| 0 | INT_HEDGE | HSYNC rising edge occur interrupt | |

Default: 0000 0000B

| 0x1AC | | SYNC Interrupt Flag 2 | R |
|---|---|---|---|
| Bits | Name | Description | |
| 4 | INT_DVIPRE | DVI SYNC present or non-present interrupt | |
| 3 | INT_ISPRE | Interlaced SYNC present or non-present interrupt | |
| 2 | INT_CSPRE | Composite SYNC present or non-present interrupt | |
| 1 | INT_VPRE | VSYNC present or non-present interrupt | |
| 0 | INT_HPRE | HSYNC present or non-present interrupt | |

Default: XXX0 0000B

| 0x1AB | | SYNC Interrupt Flag 1 Clear | W |
|---|---|---|---|
| Bits | Name | Description | |
| 5 | CLR_VFREQ | Writing ‘1’ will clear INT_VFREQ flag | |
| 4 | CLR_HFREQ | Writing ‘1’ will clear INT_HFREQ flag | |
| 3 | CLR_VPOL | Writing ‘1’ will clear INT_VPOL flag | |
| 2 | CLR_HPOL | Writing ‘1’ will clear INT_HPOL flag | |
| 1 | CLR_VEDGE | Writing ‘1’ will clear INT_VEDGE flag | |
| 0 | CLR_HEDGE | Writing ‘1’ will clear INT_HEDGE flag | |

Default: 0000 0000B

| 0x1AC | | SYNC Interrupt Flag 2 Clear | W |
|---|---|---|---|
| Bits | Name | Description | |
| 4 | CLR_DVIPRE | Writing ‘1’ will clear INT_DVIPRE flag | |
| 3 | CLR_ISPRE | Writing ‘1’ will clear INT_ISPRE flag | |
| 2 | CLR_CSPRE | Writing ‘1’ will clear INT_CSPRE flag | |
| 1 | CLR_VPRE | Writing ‘1’ will clear INT_VPRE flag | |
| 0 | CLR_HPRE | Writing ‘1’ will clear INT_HPRE flag | |

Default: XXX0 0000B

| 0x1AD | | DVI Sync Status | R |
|---|---|---|---|
| Bits | Name | Description | |
| 0 | DVI_SCDT | DVI Sync Detect. (Read Only)<br>0 = When DE is inactively, indicating the link is down<br>1 = When DE is actively toggling indicating that the link is alive.<br>The SCDT output itself, however, remains in the active mode at all times. | |

**Video Sync Processor Control**

| 0x1AE | Video Sync Processor Status | R |
|---|---|---|
| Bits | Name | Description |
| 2 | VI_INTE | Interlace input detected flag<br>0 = Progressive input<br>1 = Interlaced input |
| 1 | VI_VPOL | VSYNC polarity<br>0 = Active low<br>1 = Active high |
| 0 | VI_HPOL | HSYNC polarity<br>0 = Active low<br>1 = Active high |

| 0x1AF | Video Field Decision Window | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-4 | VI_FLD_WINEDN [3:0] | Define the end position of video field decision window. |
| 3-0 | VI_FLD_WINBEG [3:0] | The V_HS period is divided into 16 segments; a field decision window is defined by VI_FLD_WINBEG and VI_FLD_WINEND. VI_FLD_WINBEG defines the window begin position, and VI_FLD_WINEND defines the end position. If the V_VS reference edge locates inside the window, it means ODD field. |

Default: 0100 1100B

| 0x1B0 | Field Polarity Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 1 | VI_FLD_EDGE | Select the reference edge of VSYNC in Video Field Detector<br>0 = Leading edge<br>1 = Trailing edge |
| 0 | VI_FLD_INV | Invert the polarity of Video Field Detector output signal or external EXFLD input signal.<br>0 = Normal<br>1 = Invert |

Default: XXXX XX00B

| 0x1B1 | Hsync Pulse width counter | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | GI_HS_WID [7:0] | Hsync pulse width counter. GI_HS_WID is the number of REFCLK in the period of HSYNC.<br>Hpswid = (1/REFCLK x GI_HS_WID) |

Default: 0000 0000B

| 0x1B2 | Vsync Pulse width counter | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | GI_VS_WID [7:0] | Vsync pulse width counter. GI_VS_WID is the number of clock in the period of HSYNC. |

Default: 0000 0000B

| 0x1B3 | | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | PRE_COAST | Sets the number of Hsync periods that coast becomes active prior to Vsync. |

Default: 0000 0000B

| 0x1B4 | | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | POS_COAST | Sets the number of Hsync periods that coast stays active following Vsync. |

Default: 0000 0000B

| 0x1B5 | | Graphic VTotal Counter-lo | R |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | GI_VTOTAL [7:0] | Vertical total counter. GI_VTOTAL is an 11-bit counter, counter value is the number of Hsync between two VSYNC pulses. | |

Default: 0000 0000B

| 0x1B6 | | Graphic VTotal Counter-hi | R |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | GI_VTOTAL [10:8] | MSB of GI_VTOTAL | |

Default: 0000 0000B

| 0x1B7 | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| | | | |

Default: 0000 0000B

## 9.26. LVDS Output Control

| 0x1B8 | | LVDS Output Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 5-3 | LVDS_LEVEL [2:0] | Fine tune LVDS output differential voltage<br>000: Standard output 200 mVp-p<br>001: Output 250 mVp-p<br>010: Output 300 mVp-p<br>011: Output 350 mVp-p<br>100: Output 400 mVp-p<br>101~111: Reserved | |
| 2-1 | LVDS_ICO [1:0] | Charge pump current<br>00 : 100uA<br>01 : 200uA<br>10 : 400uA<br>11 : 800uA | |
| 0 | LVDS_RFB | Data strobe edge selection<br>0 = falling edge strobe<br>1 = rising edge strobe | |

Default: 0000 0000B

| 0x1B9 | | Display Output Interface Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |

| | | |
|---|---|---|
| 7-6 | | Reserved |
| 5 | DIS_OUT_CTL | Display Output interface type control status (Read only)<br>0 = Register control Disable<br>1 = Register control enable |
| 4 | DIS_OUT_TYPE | Display Output interface type status (Read only)<br>0 = RSDS output<br>1 = LVDS output |
| 3-1 | | Reserved |
| 0 | TCON_EN | Timing controller enable<br>0 = Disable<br>1 = Enable |

Default: 0000 0000B

| 0x1BA~1BF | | R/W |
|---|---|---|
| Bits | Name | Description |
| | | |

Default: 0000 0000B

| 0x1C0~1C6 | | R/W |
|---|---|---|
| Bits | Name | Description |
| | | |

Default: 0000 0000B

## 9.27. Data Tracking Control

| 0x1C7 | Data Tracking Control | R/W |
|---|---|---|
| Bits | Name | Description |
| 7 | DIT_TRACK4_EN | Dithering data output tracking enable<br>0: Disable<br>1: Enable |
| 6 | GAM_TRACK3_EN | Gamma data output tracking enable<br>0: Disable<br>1: Enable |
| 5 | OSD_TRACK2_EN | OSD data output tracking enable<br>0: Disable<br>1: Enable |
| 4 | GO_TRACK1_EN | Gain/Offset data output tracking enable<br>0: Disable<br>1: Enable |
| 3-1 | | Reserved |
| 0 | DATA_TRACK1_EN | Scaler tracking enable One<br>0: Disable<br>1: Enable |

Default: 0000 0000B

| 0x1C8~1CB | Data Tracking Mask | R/W |
|---|---|---|
| Bits | Name | Description |
| 7-0 | DATA_MASK [7:0] | |

Default: 0000 0000B

| 0x1CC~1CF | | | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| | | | |

Default: 0000 0000B

## 9.28. sRGB Control

| 0x1D0 | | sRGB Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-6 | | Reserved | |
| 5 | SRGB_DITH_EN | SRGB dithering enable | |
| 4 | RANDOM_DITH_EN | Random dithering enable | |
| 3 | SRGB_FORCE_UPD | Force update sRGB<br>0: Disable<br>1: Force update the sRGB Coefficient to H/W | |
| 2-1 | SRGB_BK_SEL | Select sRGB converting tristimulus values bank<br>00 = R<br>01 = G<br>10 = B<br>11 = Reserved | |
| 0 | SRGB_En | sRGB Enable<br>0: Disable<br>1: Enable | |

Default: XXXX 1000B

| 0x1D1 | | sRGB Transfer Coefficient R Channel – lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | SRGB_COEF_R [7:0] | sRGB Transfer R channel coefficient LSB<br>-1024 ~ 1023 | |

Default: 0000 0000B

| 0x1D2 | | sRGB Transfer Coefficient R Channel – hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | SRGB_COEF_R [10:8] | MSB of SRGB_COEF_R | |

Default: 0000 0000B

| 0x1D3 | | sRGB Transfer Coefficient G Channel – lo | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7-0 | SRGB_COEF_G [7:0] | sRGB Transfer GIN coefficient LSB<br>-1024 ~ 1023 | |

Default: 0000 0000B

| 0x1D4 | | sRGB Transfer Coefficient G Channel – hi | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 2-0 | SRGB_COEF_G [10:8] | MSB of SRGB_COEF_G | |

Default: 0000 0000B

| 0x1D5 | | sRGB Transfer Coefficient B Channel – lo | R/W |
|---|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | SRGB_COEF_B [7:0] | sRGB Transfer BIN coefficient LSB<br>-1024 ~ 1023 |

Default: 0000 0000B

| 0x1D6 | sRGB Transfer Coefficient B Channel – hi | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 2-0 | SRGB_COEF_B [10:8] | MSB of SRGB_COEF_B |

Default: 0000 0000B

| 0x1D7 | sRGB Transfer Coefficient B Channel – hi | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 2-0 | SRGB_COEF_OFFSET [7:0] | The offset coefficient of sRGB matrix |

Default: 0000 0000B

| 0x1D8 | sRGB | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-4 | | Reserved |
| 3-2 | DITH_10 | “10” dithering type |
| 1-0 | DITH_01 | “01” dithering type |

Default: 0000 0000B

| 0x1D9~1DB | | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| | | |

Default: 0000 0000B

| 0x1DC | Scaler Misc. Odd Read Back and Control | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | MISC_O_RD [7:0] | Misc. odd read back low byte |

| 0x1DD | Scaler Misc. Odd Read Back and Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7 | MISC_O_EN | Misc. odd control enable<br>0 = Disable<br>1 = Enable |
| 3-0 | MISC_O_RD [11:8] | Misc. odd read back low byte |

| 0x1DE | Scaler Misc. Even Read Back and Control | R |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7-0 | MISC_E_RD [7:0] | Misc. even read back low byte |

| 0x1DF | Scaler Misc. Even Read Back and Control | R/W |
|---|---|---|

| Bits | Name | Description |
|---|---|---|
| 7 | MISC_E_EN | Misc. even control enable<br>0 = Disable<br>1 = Enable |
| 3-0 | MISC_E_RD [11:8] | Misc. even read back low byte |

## 9.29. Register Page Control

| 0x0FF / 0x1FF / 0x2FF | Accessing Register Page Enable | R/W |
|---|---|---|
| Bits | Name | Description |
| D7-2 | | Reserve |
| D1-0 | REG_PAGE_SEL | Register Page Enable<br>00: Enable register Page0.<br>01: Enable register Page1.<br>10: Enable register Page2.<br>11: Reserved |

Default: XXXX XX00B

## 9.30. Test Mode

| 0x1E0H | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserve | |

Default :0000 0000B

| 0x1E1H | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserve | |

Default :0000 0000B

| 0x1E2 | | Test Mode Control 1 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7 | | Reserve | |

Default：0000 0000B

| 0x1E3 | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7 | | Reserve | |
| D6 | | Reserve | |
| D5 | | Reserve | |
| D4 | | Reserve | |
| D3 | | Reserve | |
| D2 | | Reserve | |
| D1 | | Reserve | |
| D0 | | Reserve | |

Default：XX00 0X00B

| 0x1E4 | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7 | | Reserve | |
| D6 | | Reserve | |
| D5-4 | | Reserve | |
| D3 | | Reserve | |
| D2-1 | | Reserve | |
| D0 | | Reserve | |

Default：0000 0000B

| 0x1E5 | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7 | | Reserve | |
| D6 | | Reserve | |
| D5 | | Reserve | |
| D4 | | Reserve | |
| D3 | | Reserve | |
| D2 | | Reserve | |
| D1 | | Reserve | |
| D0 | | Reserve | |

Default：00XX 000B

| 0x1E6 | | ADC test mode Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| 7 | | Reserved | |
| 6 | SYNC_HS_SEL | Hsync2 selection<br>1: Hsync from sync process<br>0: Hsync from SOGI path | |
| 5 | | Reserved | |
| 4 | | Reserved | |
| 3-0 | | Reserved | |
| 0 | RSTB | Reset ADC data to low | |

Default：X000 XXX1B

| 0x1E7 | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserve | |

Default：0100 XXXXB

| 0x1E8~1EA | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserved | |

Default：XXXX XXXXB

| 0x1EB | | ADC Comparator Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-2 | | Reserve | |
| D1-0 | Icomp[1:0] | ADC comparator current control<br>00: 100 %<br>01: 114 %<br>10: 133 %<br>11: 80 % | |

Default：0000 0000B

| 0x1EC | | ADC Test 1 Control | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | Test1[7:0] | Test 1 Control | |

Default：0000 0000B

| 0x1ED | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserve | |

Default：0000 0000B

| 0x1EE | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserve | |

Default：0000 0000B

| 0x1EF | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| D7 | HPLL_CK_TEST | HPLL clock reconstructed and phase-aligned by TMDS PLL |
| D6-0 | | Reserved |

Default：0000 0000B

| 0x1F0 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| D7-0 | | Reserve |

Default：0000 0000B

| 0x1F1 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| D7-6 | | Reserved |
| D5-4 | | Reserve |
| D3-2 | | Reserve |
| D1-0 | | Reserve |

Default：XX11 1111B

| 0x1F2 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| D7-0 | | Reserve |

Default：0000 000xB

| 0x1F3 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| D7-2 | | Reserved |
| D1 | | Reserve |
| D0 | | Reserve |

Default：0000 0011B

| 0x1F4 | Reserved | R/W |
|---|---|---|
| Bits | Name | Description |
| D7-0 | | Reserve |

Default：1000 0010B

| 0x1F5 | LVDS control 1 | R/W |
|---|---|---|
| Bits | Name | Description |
| D7 | Reg_125L | |
| D6 | Reg_125R | |
| D5 | EN_125 | |
| D4 | PULL_LOW | Display output power down buffer control<br>0: Tri-state output<br>1: pull low output |
| D3 | TEST | |
| D2-0 | T_S2 [2:0] | |

Default：0000 0000B

| 0x1F6 | | LVDS control 2 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-6 | T_MON [1:0] | | |
| D5-3 | T_S0 [2:0] | | |
| D2-0 | T_S1 [2:0] | | |

Default：0000 0000B

| 0x1F7 | | LVDS control 3 | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7 | PD_LV1 | LV1 power control<br>0: Power down<br>1: Power up | |
| D6 | PD_LV2 | LV2 power control<br>0: Power down<br>1: Power up | |
| D5-0 | | Reserve | |

Default：0000 0000B

| 0x1F8 | | Reserved | R/W |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserve | |

Default：0000 0000B

| 0x1F9 | | Reserved | R |
|---|---|---|---|
| Bits | Name | Description | |
| D7-0 | | Reserve | |

Default：0000 0000B

| 0x1FC | | Reserved | R |
|---|---|---|---|
| Bits | Name | Description | |
| D7-5 | | Reserved | |
| D4 | | Reserve | |
| D3 | | Reserve | |
| D2 | | Reserve | |
| D1 | | Reserve | |
| D0 | | Reserve | |

Default：XXX0 0000B

| 0x1FB | | LVDS PLL divider control | R |
|---|---|---|---|
| Bits | Name | Description | |
| D7-5 | | Reserved | |
| D4 | | Reserve | |
| D3 | | Reserve | |
| D2-1 | LVDS_PLL_DIV [1:0] | LVDS PLL frequency range<br>00: 80~180MHz | |

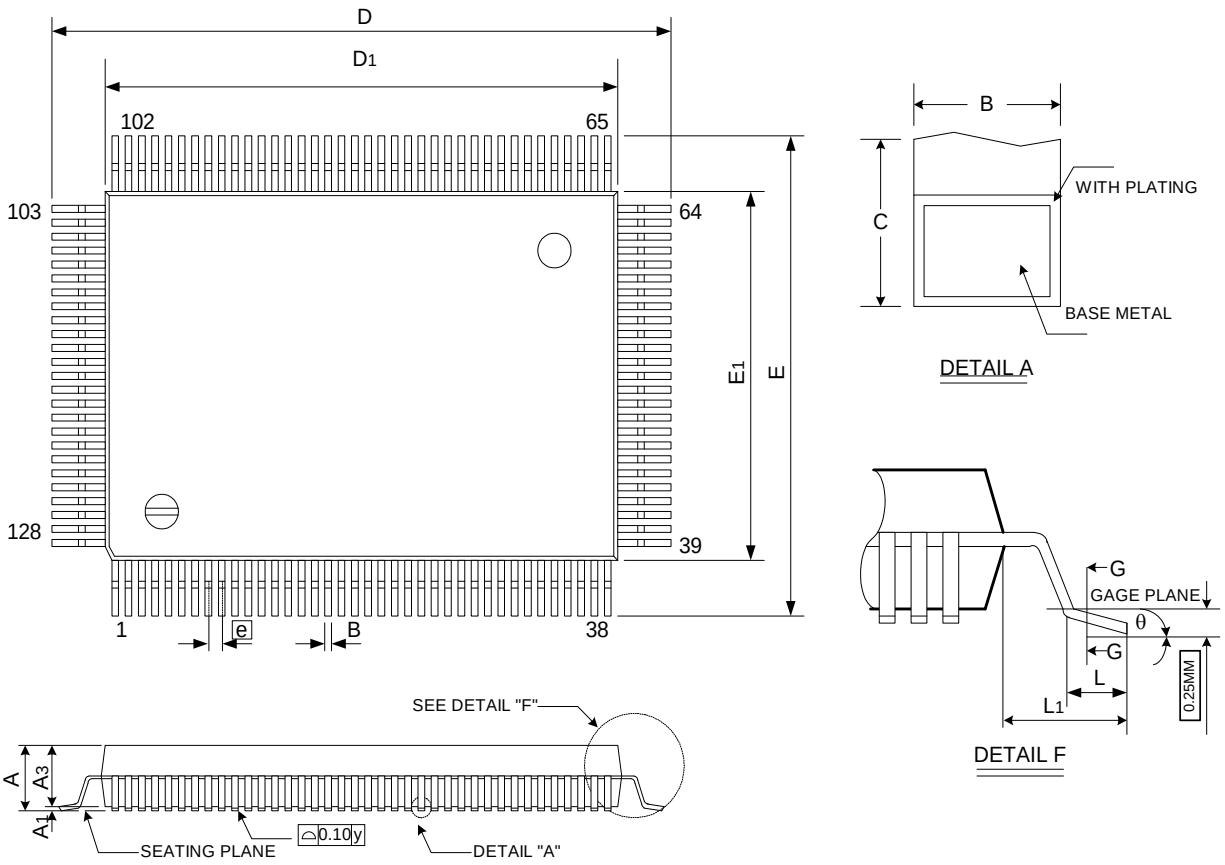
| | | |
|---|---|---|
| | | 01: 40~80MHz<br>10: 20~40MHz<br>11: 10~20MHz |
| D0 | LVDS_CLK_2X | Reserve |

Default：XXXX X000B

# 10. Ordering Information

| Order Code | Application | Package | Note |
|---|---|---|---|
| NT68563EF | SXGA with LVDS transmitter Panel interface | QFP 128L | |
| NT68563XF | XGA with LVDS transmitter Panel interface | QFP 128L | |
| NT68563EFG | SXGA with LVDS transmitter Panel interface | QFP 128L | Green Product<br>( Pb-free) |
| NT68563XFG | XGA with LVDS transmitter Panel interface | QFP 128L | Green Product<br>( Pb-free) |

# 11. Package Information




**QFP 128L Outline Dimensions** **unit: inches/mm**

| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | -- | -- | 0.134 | -- | -- | 3.40 |
| A**1** | 0.010 | -- | -- | 0.25 | -- | -- |
| A**2** | 0.107 | 0.112 | 0.117 | 2.73 | 2.85 | 2.97 |
| B | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| C | 0.004 | -- | 0.008 | 0.09 | -- | 0.20 |
| D | 0.906 | 0.913 | 0.921 | 23.00 | 23.20 | 23.40 |
| D1 | 0.783 | 0.787 | 0.791 | 19.90 | 20.00 | 20.10 |
| E | 0.669 | 0.667 | 0.685 | 17.00 | 17.20 | 17.40 |
| E1 | 0.547 | 0.551 | 0.555 | 13.90 | 14.00 | 14.10 |
| e | 0.020 BSC | | | 0.5 BSC | | |
| L | 0.029 | 0.035 | 0.041 | 0.73 | 0.88 | 1.03 |
| L1 | 0.063 BSC | | | 1.60 BSC | | |
| Y | -- | -- | 0.004 | -- | -- | 0.10 |
| θ | 0° | -- | 7° | 0° | -- | 7° |

**Notes:** 1.Dimensions D & E do not include resin fins.
2.Dimensions F, G**D** & G**E** are for PC Board surface mount pad pitch design reference only