NOVATEK
聯 詠 科 技

Data Sheet

NT7701

160 Output LCD Segment/Common Driver

V2.2

Revision History

NT7701 Specification Revision History		
Version	**Content**	**Date**
1.0	Release	Oct. 2000
2.0	1. Chip size modify (Due to scribe-line modify, change7720μm x 1030μm to 7664μm x 986μm, Page 27) 2. Gold bump size modify (Page 31)	Jul. 2002
2.1	Alignment mark pad location correct (Page 29) ALK_L: -3438(X), -323(Y) change to –3577(X), -320(Y) ALK_R: 3438(X), -323(Y) change to 3577(X), -320(Y)	Dec. 2002
2.2	1. Delete TCP drawing information and Tray information (Page 1, 3, 32~35) 2. Correct Connection Examples of dual mode for Common Drivers (Page 21) 3. Add Application Circuit & ITO Layout Notice 4. Modify Stand-by Current for Common mode from 50μA to 5μA (Page 23~24) 5. Modify Input Leakage Current for Common mode from 10μA to 1μA (page 24) 6. Add Cautions	Oct. 2005

Features

(Segment mode)
- Shift Clock frequency:
  14 MHz (Max.) (VDD = 5V±10%)
  8 MHz (Max.) (VDD = 2.5V~4.5V)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selected with a mode (MD) pin
- Automatic transfer function with an enable signal
- Automatic counting function, when in the chip select mode causes the internal clock to be stopped by automatically counting 160 bits of input data.

(Common mode)
- Shift clock frequency: 4.0MHz (Max.)
- Built-in 160-bits bi-directional shift register (divisible into 80-bits x 2)
- Available in a single mode (160-bits shift register) or in a dual mode (80-bits shift register x 2)
  - Y1 → Y160 Single mode
  - Y160 → Y1 Single mode
  - Y1 → Y80, Y81 → Y160 Dual mode
  - Y160 → Y81, Y80 → Y1 Dual mode

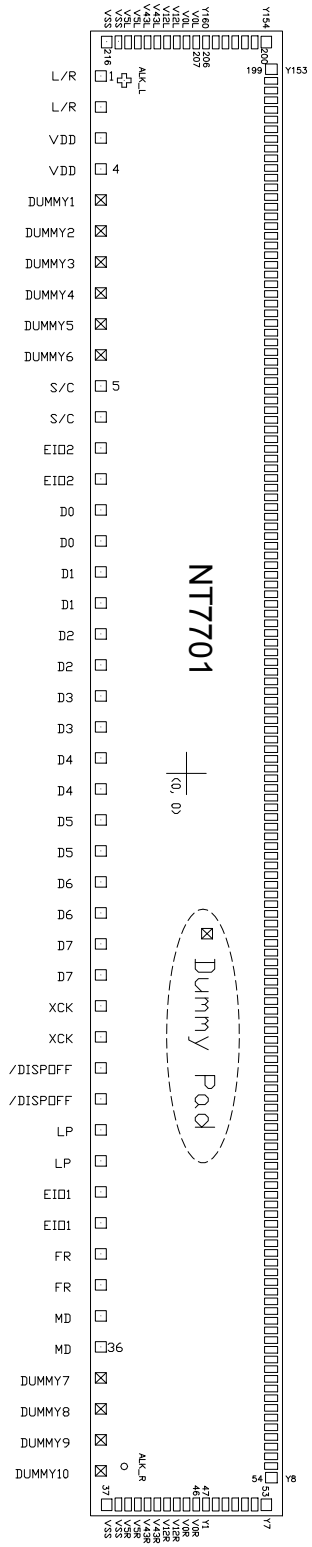
  The above 4 shift directions are pin-selectable

(Both segment mode and common mode)
- Supply voltage for LCD drive: 15.0 to 30.0V
- Number of LCD driver outputs: 160
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5V
- CMOS process
- Not designed or rated as radiation hardened

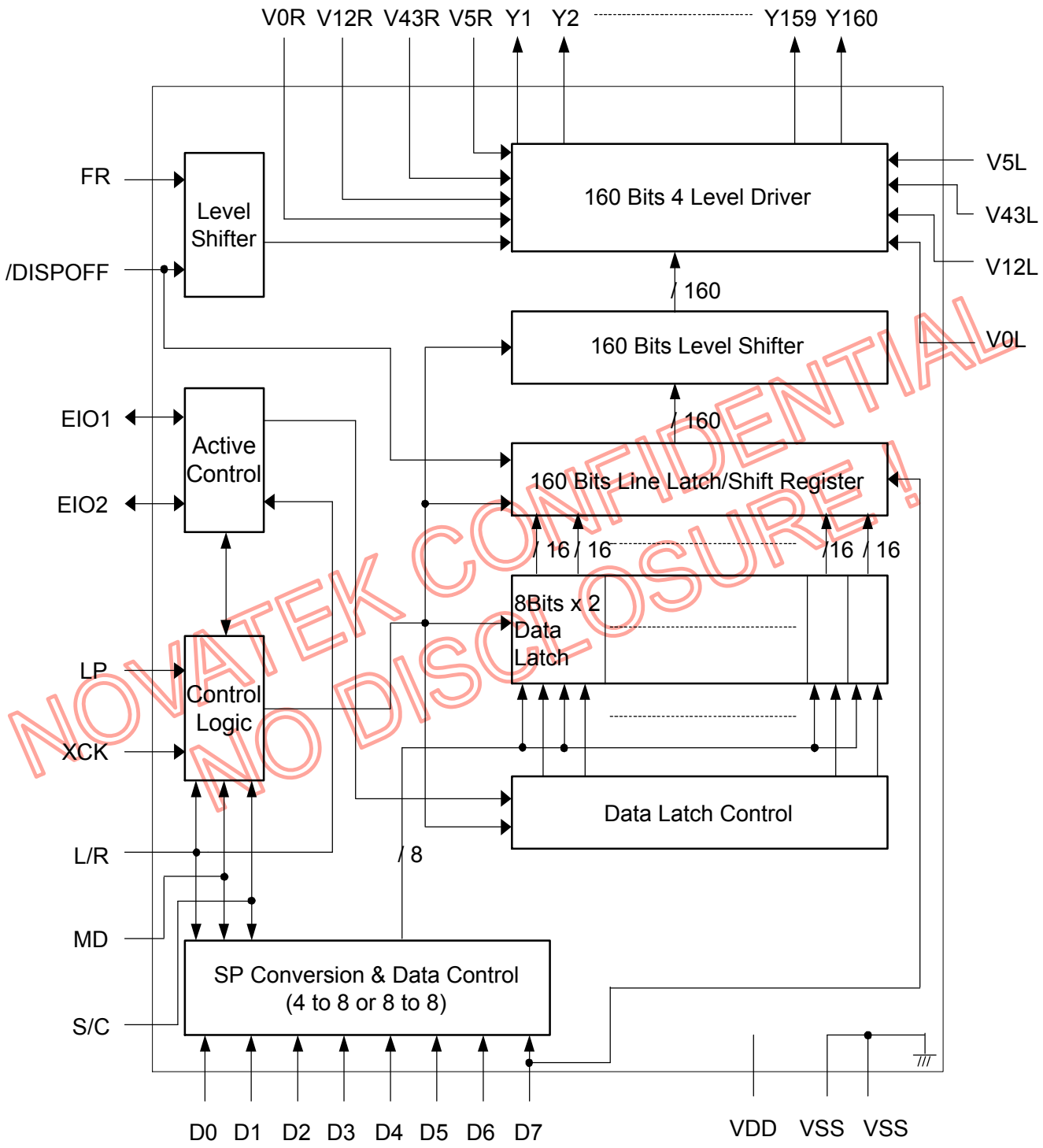
General Description

The NT7701 is a 160-bit output segment/common driver LSI suitable for driving the large-scale dot matrix LCD panels used by PDA's, personal computers and workstations for example. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The NT7701 is good as both a segment driver and a common driver, and a low power consuming, high-precision LCD panel display can be assembled using the NT7701. In the segment mode, the data input is selected 4bit parallel input mode or as 8bit parallel input mode by a mode (MD) pin. In common mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

Pad Configuration



Block Diagram



Pad Descriptions

Pad No.	Designation	I/O	Description
1, 2	L/R	I	Display data shift direction selection.
3, 4	VDD	P	Power supply for the logic system (+2.5 to +5.5V).
5, 6	S/C	I	Segment mode/common mode selection.
7, 8	EIO2	I/O	Input/output for chip selection or data of the shift register.
9 ~ 22	D0 ~ D6	I	Display data input for segment mode.
23, 24	D7	I	Display data input for Segment mode/ Dual mode data input.
25, 26	XCK	I	Display data shift clock input for segment mode.
27, 28	/DISPOFF	I	Control input for deselect output level.
29, 30	LP	I	Latch pulse input/shift clock input for the shift register.
31, 32	EIO1	I	Input/output for chip select or data of the shift register.
33, 34	FR	I/O	AC-converting signal input for LCD driver waveform.
35, 36	MD	I	Mode selection input.
37, 38	VSS	P	Ground (0V), these two pads must be connected to each other.
39, 40	V5R	I	Power supply for LCD driver.
41, 42	V43R	P	Power supply for LCD driver.
43, 44	V12R	P	Power supply for LCD driver.
45, 46	V0R	P	Power supply for LCD driver.
47 ~ 206	Y1 ~ Y160	P	LCD driver output.
207, 208	V0L	P	Power supply for LCD driver.
209, 210	V12L	O	Power supply for LCD driver.
211, 212	V43L	P	Power supply for LCD driver.
213, 214	V5L	P	Power supply for LCD driver.
215, 216	VSS	P	Ground (0V), these two pads must be connected to each other.

Functional Descriptions

Block Description

Active Control

In the case of the segment mode, controls the selection or deselection of the chip. Following an LP signal input, and after the select signal is input, a select signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.

In common mode, controls the input/output data of bi-directional pins.

SP Conversion & Data Control

In segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

Data Latch Control

In the case of the segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

Data Latch

In the case of the segment mode, it latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch controlling 160 bits of data are read in 20 sets of 8 bits.

Line Latch / Shift Register

In the case of the segment mode, all 160 bits that have been read into the data latch are latched on to the falling edge of the LP signal and output to the level shift block simultaneously.

In the case of the common mode, shifts data from the data input pin on to the falling edge of the LP signal.

Level Shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

4-Level Driver

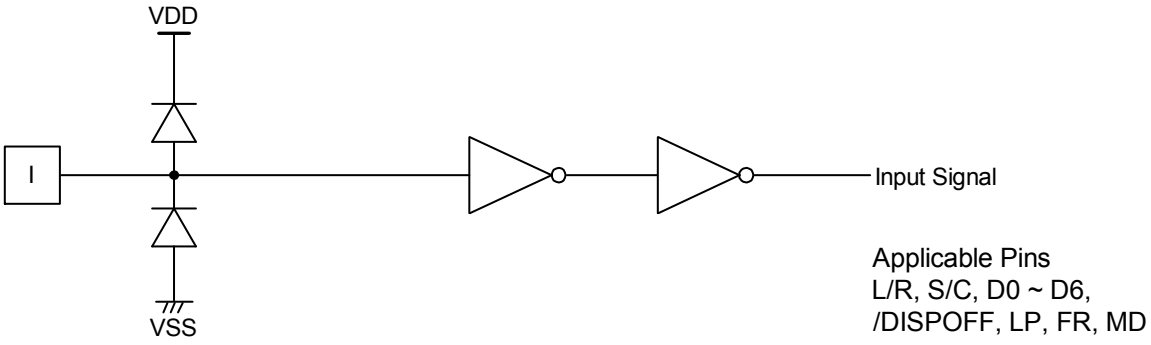
It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V0, V12, V43, V5) based on the S/C, FR and /DISPOFF signals.

Control Logic

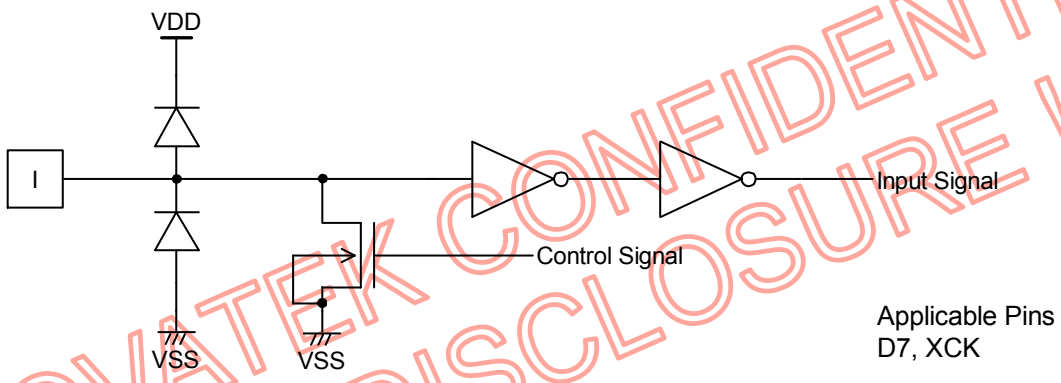
It controls the operation of each block. In the case of the segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected.

In common mode, it controls the direction of the data shift.

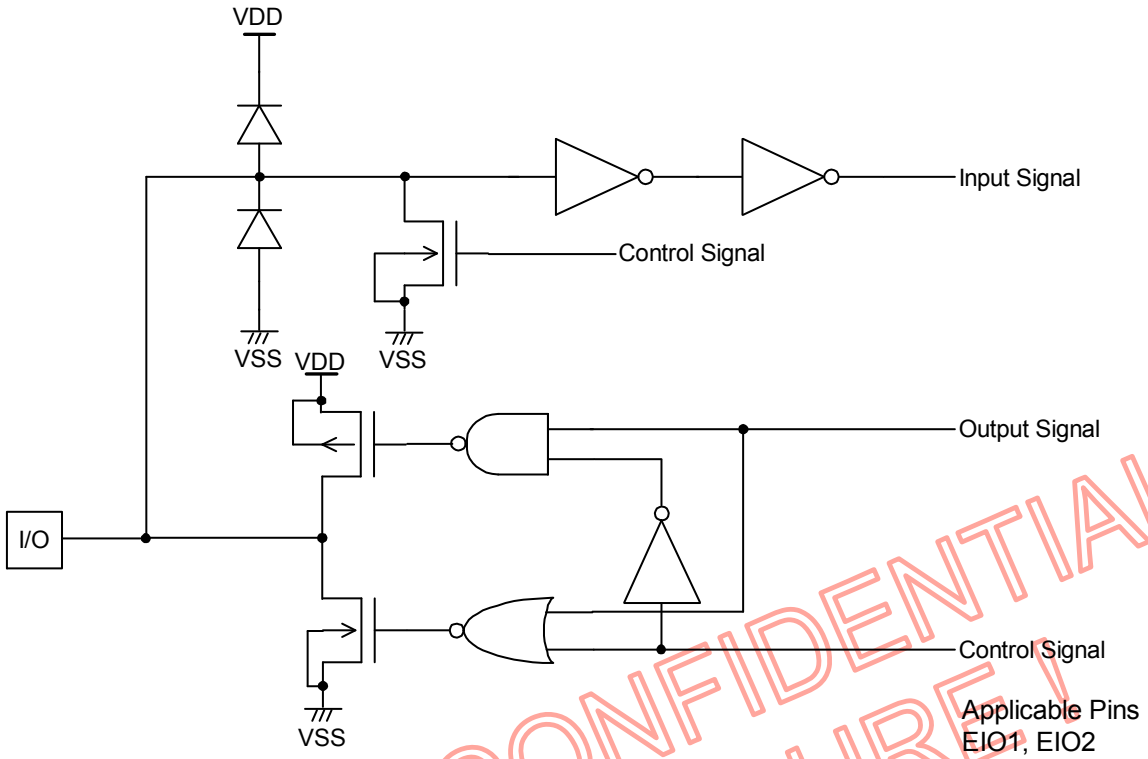
Input / Output Circuits



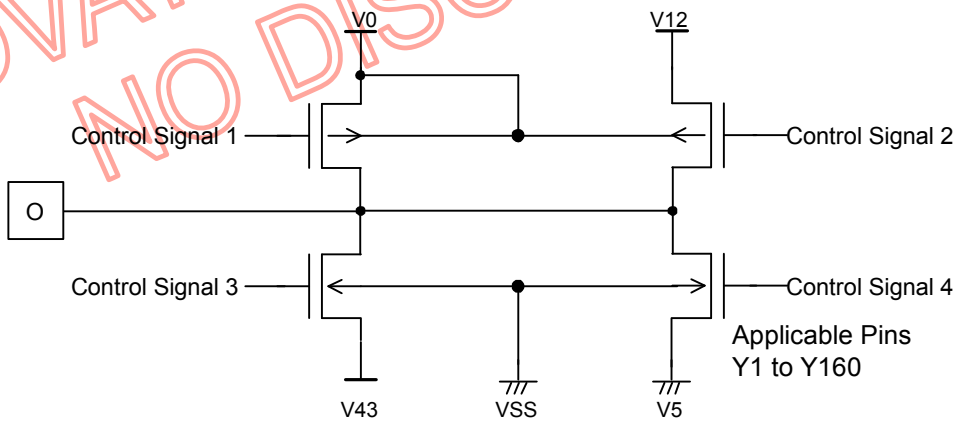
Input Circuit (1)



Input Circuit (2)



Input / Output Circuit



LCD Driver Output circuit

Pad Function

Segment mode

Symbol	Function
VDD	Logic system power supply pin connects to +2.5 to +5.5V.
VSS	Ground pin connects to 0V.
V0R, V0L V12R, V12L V43R, V43L V5R, V5L	Power supply pin for LCD driver voltage bias. • Normally, the bias voltage used is set by a resistor divider. • Ensure that the voltages are set such that VSS ≤ V5 < V43 < V12 < V0. • To further reduce the differences between the output waveforms of the LCD driver output pins Y1 to Y160, externally connect ViR and ViL (i = 0, 12, 43, 5).
D0 ~ D7	Input pin for display data. • In 4-bit parallel input mode, input data into the 4 pins D0 ~ D3. Connect D4 ~ D7 to VSS or VDD. • In 8-bit parallel input mode, input data into the 8 pins D0 ~ D7.
XCK	Clock input pin for taking display data. • Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data. • Data is latched on the falling edge of the clock pulse.
L/R	Direction selection pin for reading display data. • When set to VSS level “L”, data is read sequentially from Y160 to Y1. • When set to VDD level “H”, data is read sequentially from Y1 to Y160.
/DISPOFF	Control input pin for output deselect level. • The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD driver circuit. • When set to “L”, the LCD driver output pins Y1 to Y160 are set to level V5. • While /DISPOFF is set to “L”, the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs deselect level (V12 or V43), then outputs the contents of the data latch on to the next falling edge of the LP. At that time, if /DISPOFF removal time can not regulate what is shown AC characteristics, can not output the reading data correctly.
FR	AC signal input for LCD driving waveform. • The input signal is level-shifted from the logic voltage level to the driver voltage level, and controls the LCD driver circuit. • Normally inputs a frame inversion signal. The LCD driver output pin’s output voltage level can be set to the line latch output signal and the FR signal.
MD	Mode selection pin. • When set to VSS level “L”, 4-bit parallel input mode is set. • When set to VDD level “H”, 8-bit parallel input mode is set.

Segment mode (continuous)

Symbol	Function
S/C	Segment mode / common mode selection pin. • When set to VDD level “H”, segment mode is set. • When set to VSS level “L”, common mode is set.
EIO1, EIO2	Input/output pin for chip selection. • When L/R input is at VSS level “L”, EIO1 is set for output, and EIO2 is set for input. • When L/R input is at VDD level “H”, EIO1 is set for input, and EIO2 is set for output. • During output, it is set to “H” while LP*(/XCK) is “H” and after 160-bits of data have been read, it is set to “L” for one cycle (from falling edge to falling edge of XCK), after which it returns to “H”. • During input, after the LP signal is input, the chip is selected while EI is set to “L”. After 160-bits of data have been read, the chip is deselected.
Y1 ~ Y160	LCD driver output pins • These correspond directly to each bit of the data latch, and one level (V0, V12, V43, or V5) is selected and the output.

Common mode

Symbol	Function
VDD	Logic system power supply pin connects to +2.5 to +5.5V.
VSS	Ground pin connects to 0V.
V0R, V0L V12R, V12L V43R, V43L V5R, V5L	Power supply pin for LCD driver voltage bias. • Normally, the bias voltage used is set by a resistor divider. • Ensure that the voltages are set such that VSS ≤ V5 < V43 < V12 < V0. • To further reduce the differences between the output waveforms of the LCD driver output pins Y1 to Y160, externally connect ViR and ViL (i = 0, 12, 43, 5).
EIO1	Bi-directional shift register shift data input/output pin. • Is an Output pin when L/R is at VSS level “L” and an input pin when L/R is at VDD level “H”. • When EIO1 is used as an input pin, it will be pulled-down internally. • When EIO1 is used as an output pin, it won’t be pulled-down internally.
EIO2	Bi-directional shift register shift data input/output pin. • Is an Input pin when L/R is at VSS level “L” and an output pin when L/R is at VDD level “H”. • When EIO2 is used as an input pin, it will be pulled-down internally. • When EIO2 is used as an output pin, it won’t be pulled-down internally.
LP	Bi-directional shift register shift clock pulse input pin. • Data is shifted on the falling edge of the clock pulse.
L/R	Bi-directional shift register shift direction selection pin. • Data is shifted from Y160 to Y1 when it is set to VSS level “L”, and data is shifted from Y1 to Y160 when it is set to VDD level “H”.
/DISPOFF	Control input pin for output deselect level. • The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls the LCD driver circuit. • When set to “L”, the LCD driver output pins Y1 to Y160 are set to level V5. • While /DISPOFF is set to “L”, the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs deselect level (V12 or V43), then outputs the contents of the data latch onto the next falling edge of the LP. At that time, if /DISPOFF removal time can not regulate what is shown AC characteristics, can not output the reading data correctly.
FR	AC signal input for LCD driving waveform. • The input signal is level-shifted from the logic voltage level to the driver voltage level, and controls LCD driver circuit. • Normally inputs a frame inversion signal. The LCD driver output pin’s output voltage level can be set to the line latch output signal and the FR signal.
MD	Mode selection pin. • When set to VSS level “L”, single mode operation is selected. When set to VDD level “H”, dual mode operation is selected.

Common mode (continuous)

Symbol	Function
D7	Dual Mode data input pin. • According to the data shift direction of the data shift register, data can be input starting from the 161st bit. When the chip is used as dual mode, D7 will be pulled-down internally. When the chip is used as a single mode, D7 won't be pulled-down internally.
S/C	Segment mode / common mode selection pin. • When set to VSS level "L", common mode is set.
D0 ~ D6	Not used. • Connect D0 ~ D6 to VSS or VDD, to avoid floating.
XCK	Not used. • XCK is pull-down in common mode, so connect to VSS or open.
Y1 ~ Y160	LCD driver output pins. • These correspond directly to each bit of the data latch, and one level (V0, V12, V43, or V5) is selected and the output.

LCD Driver Output Voltage Level

The relationship amongst the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

Segment Mode

FR	Latch Data	/DISPOFF	Driver Output Voltage Level (Y1 ~ Y160)
L	L	H	V43
L	H	H	V5
H	L	H	V12
H	H	H	V0
X	X	L	V5

Here, VSS ≤ V5 < V43 < V12 < V0, H: VDD (+2.5 to +5.5V), L: VSS (0V), X: Don't care

Common Mode

FR	Latch Data	/DISPOFF	Driver Output Voltage Level (Y1 ~ Y160)
L	L	H	V43
L	H	H	V0
H	L	H	V12
H	H	H	V5
X	X	L	V5

Here, VSS ≤ V5 < V43 < V12 < V0, H: VDD (+2.5 to +5.5V), L: VSS (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage, which is assigned by specification for each power pin. At that time "Don't care" should be fixed to "H" or "L", to avoid floating.

Relationship between the Display Data and Driver Output Pins

Segment Mode

(a) 4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					1st	2nd	3rd	~	38th	39th	40th
L	L	Output	Input	D0	Y157	Y153	Y149	~	Y9	Y5	Y1
				D1	Y158	Y154	Y150	~	Y10	Y6	Y2
				D2	Y159	Y155	Y151	~	Y11	Y7	Y3
				D3	Y160	Y156	Y152	~	Y12	Y8	Y4
L	H	Input	Output	D0	Y4	Y8	Y12	~	Y152	Y156	Y160
				D1	Y3	Y7	Y11	~	Y151	Y155	Y159
				D2	Y2	Y6	Y10	~	Y150	Y154	Y158
				D3	Y1	Y5	Y9	~	Y149	Y153	Y157

(b) 8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					1st	2nd	3rd	~	18th	19th	20th
H	L	Output	Input	D0	Y153	Y145	Y137	~	Y17	Y9	Y1
				D1	Y154	Y146	Y138	~	Y18	Y10	Y2
				D2	Y155	Y147	Y139	~	Y19	Y11	Y3
				D3	Y156	Y148	Y140	~	Y20	Y12	Y4
				D4	Y157	Y149	Y141	~	Y21	Y13	Y5
				D5	Y158	Y150	Y142	~	Y22	Y14	Y6
				D6	Y159	Y151	Y143	~	Y23	Y15	Y7
				D7	Y160	Y152	Y144	~	Y24	Y16	Y8
H	H	Input	Output	D0	Y8	Y16	Y24	~	Y144	Y152	Y160
				D1	Y7	Y15	Y23	~	Y143	Y151	Y159
				D2	Y6	Y14	Y22	~	Y142	Y150	Y158
				D3	Y5	Y13	Y21	~	Y141	Y149	Y157
				D4	Y4	Y12	Y20	~	Y140	Y148	Y156
				D5	Y3	Y11	Y19	~	Y139	Y147	Y155
				D6	Y2	Y10	Y18	~	Y138	Y146	Y154
				D7	Y1	Y9	Y17	~	Y137	Y145	Y153

Common Mode

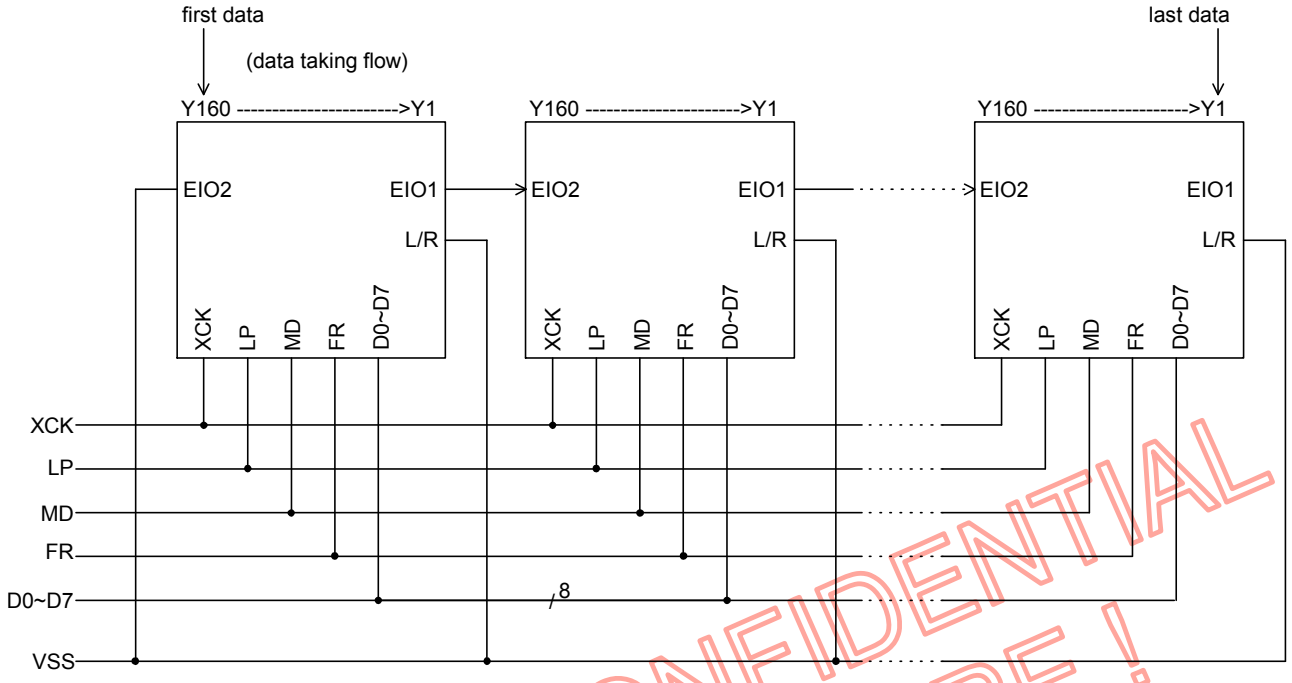
MD	L/R	Data Transfer Direction	EIO1	EIO2	D7
L (Single)	L (shift to left)	Y160 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y160	Input	Output	X
H (Dual)	L (shift to left)	Y160 to Y81 Y80 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y80 Y81 to Y160	Input	Output	Input

Here, L: VSS (0V), H: VDD (+2.5V to +5.5V), X: Don't care

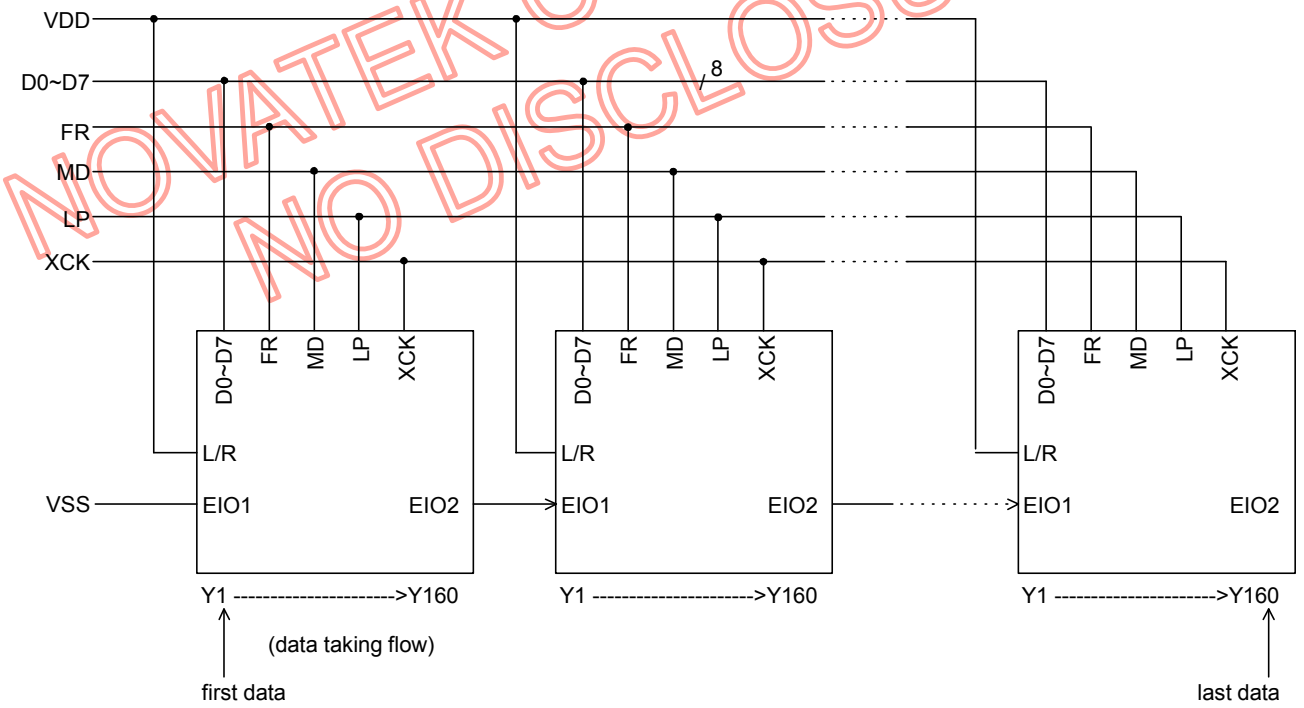
Note: “Don't care” should be fixed to “H” or “L”, to avoid floating.

Connection Examples of Segment Drivers

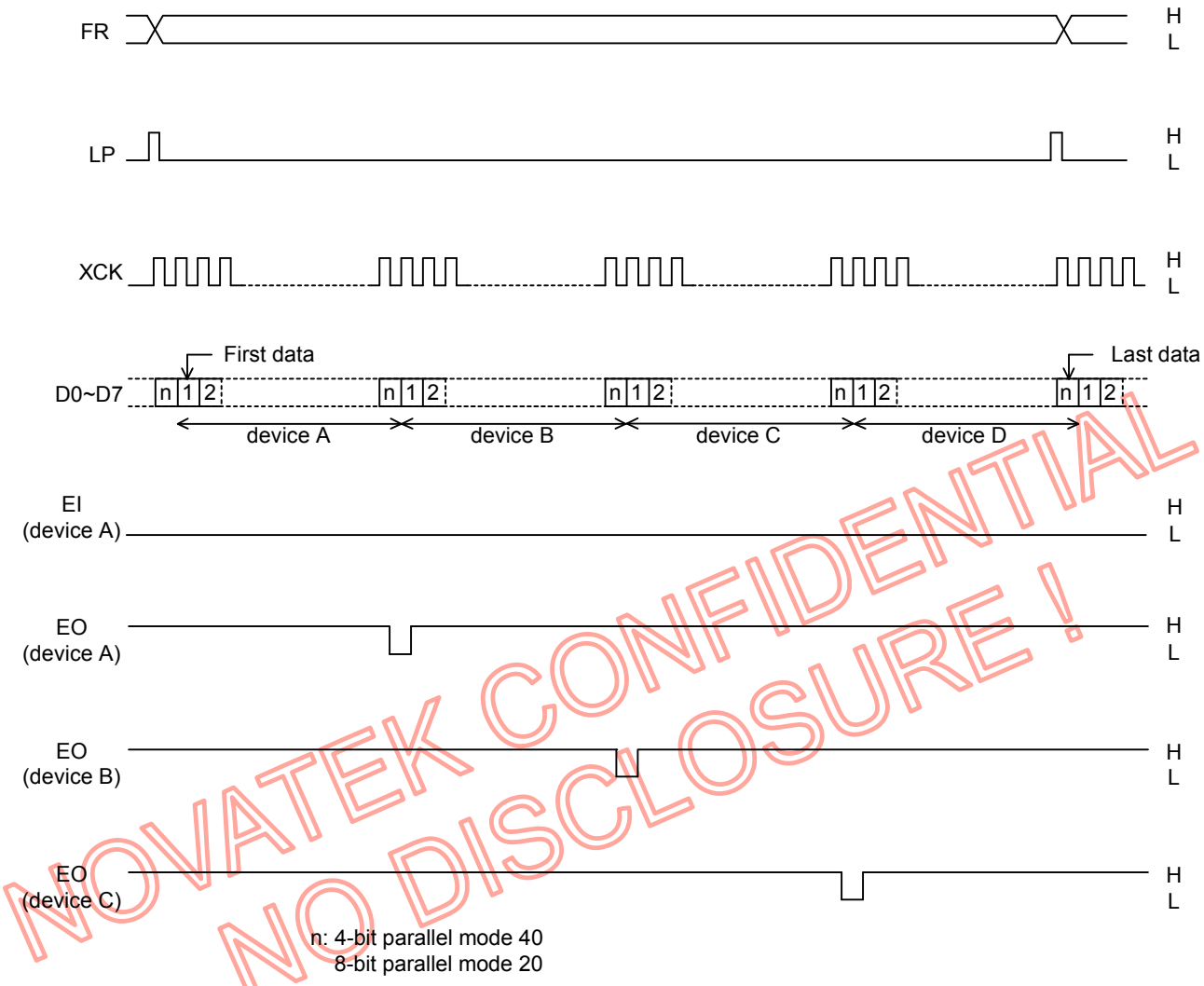
Case of L/R = “L”



Case of L/R = “H”

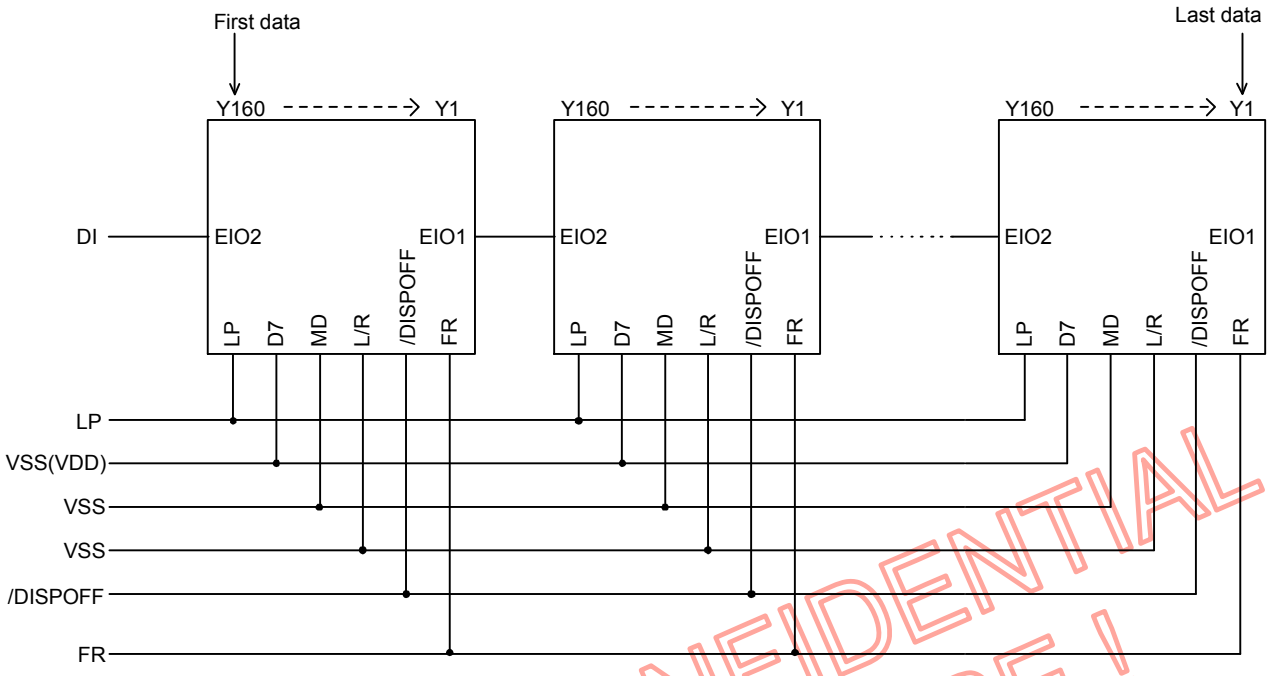


Timing Waveform of 4-Device Cascade Connection of Segment Drivers



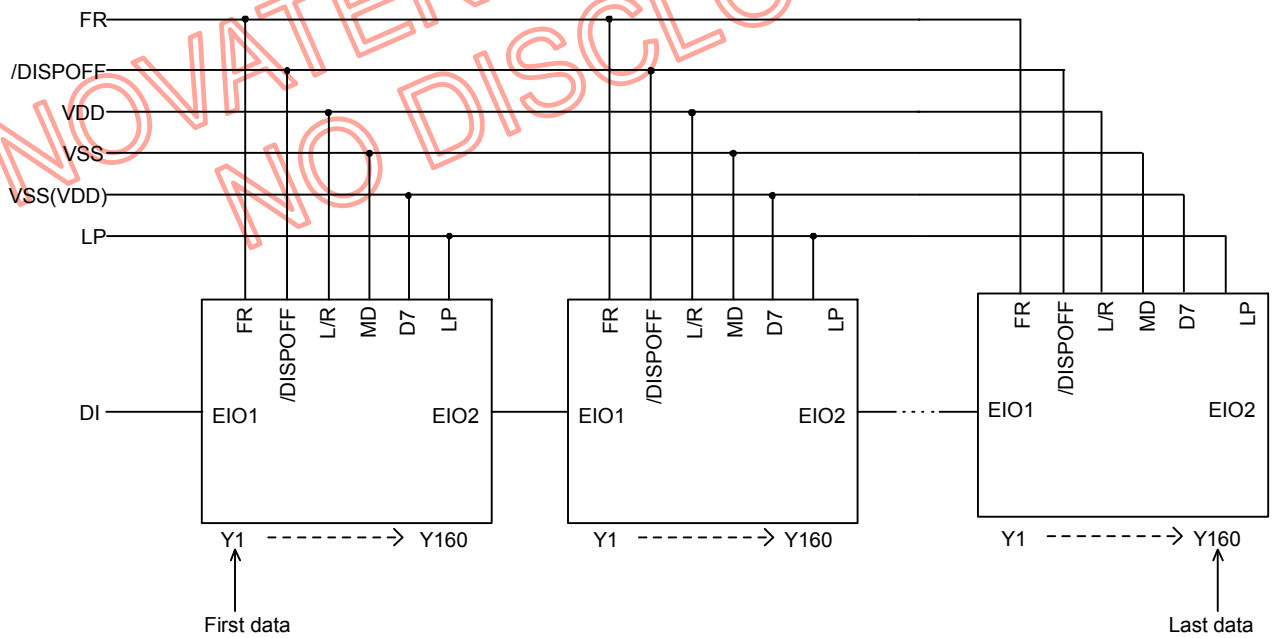
Connection Examples for Common Drivers

Case of L/R = “L”



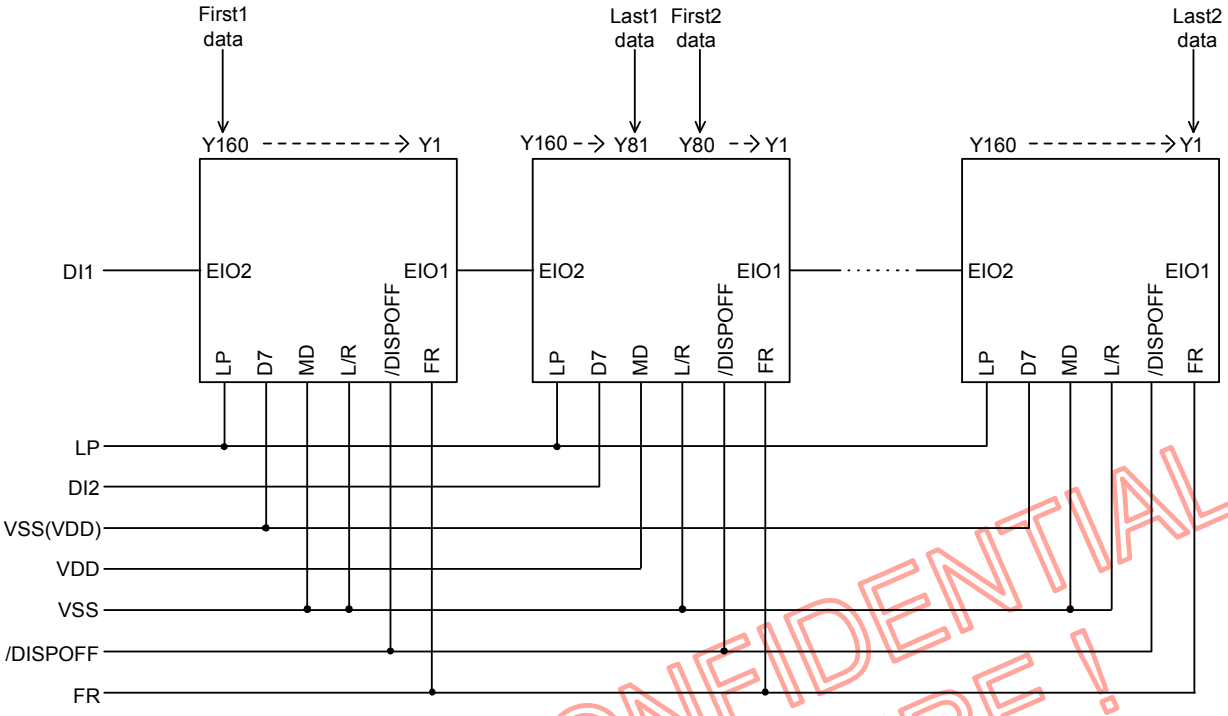
Single Mode (Shifting towards the left)

Case of L/R = “H”



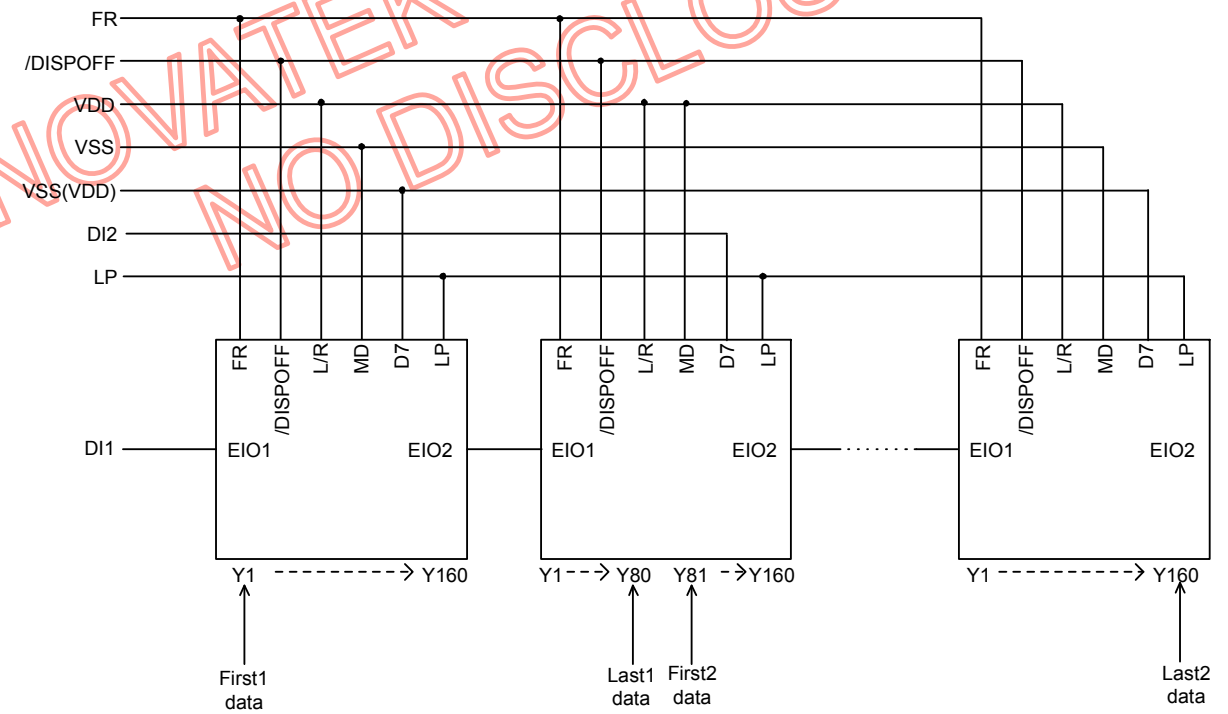
Single Mode (Shifting towards the right)

Case of L/R = “L”



Dual mode (Shifting towards the left)

Case of L/R = “H”



Dual mode (Shifting towards the right)

Precaution

Be careful when connecting or disconnecting the power.

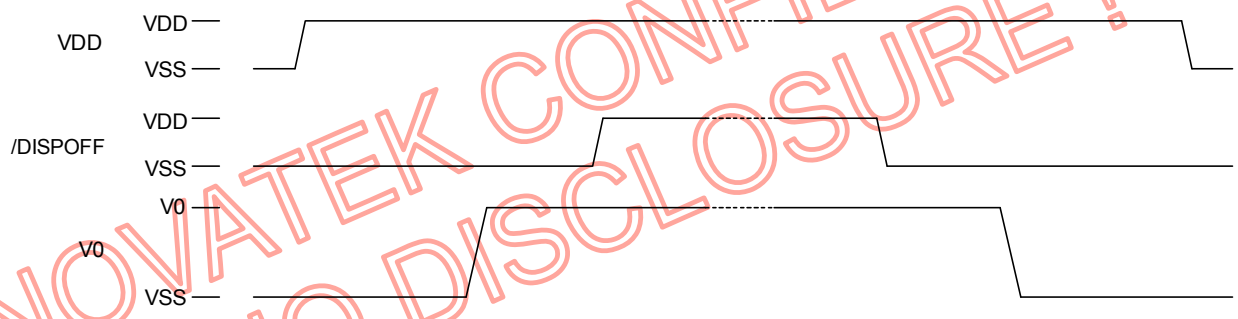
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur, if voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50 ~ 100 Ω) or fuse to the LCD driver power V0 of the system as a current limiting device. Also, set a suitable value for the resistor in consideration of the LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore connect the LCD driver power supply after resetting the logic condition of this LSI inside on /DISPOFF function. After that, the /DISPOFF cancels the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level VSS on the /DISPOFF function. After that, disconnect the logic system power after disconnecting the LCD driver power.

When connecting the power supply, follow the recommended sequence shown.



Absolute Maximum Rating

DC Supply Voltage VDD ..... -0.3V to 7.0V
DC Supply Voltage V0 ..... -0.3V to +30.0V
Input Voltage (Vin) ..... -0.3V to VDD +0.3V
Operating Ambient Temperature ..... -30°C to +85°C
Storage Temperature ..... -45°C to +125°C

*Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics

Segment Mode (VSS=V5=0V, VDD=2.5~5.5V, V0=15~30V, Ta = -30 to +85°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
VDD	Operating Voltage	2.5	-	5.5	V		
V0	Operating Voltage	15	-	30	V		
VIH	Input high voltage	0.8 X VDD	-	-	V	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins	
VIL	Input low voltage	-	-	0.2 X VDD	V		
VOH	Output high voltage	VDD - 0.4	-	-	V	EIO1, EIO2 pins, IOH = -0.4mA	
VOL	Output low voltage	-	-	+0.4	V	EIO1, EIO2 pins, IOL = +0.4mA	
IIH	Input leakage current 1	-	-	+1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VDD	
IIL	Input leakage current 2	-	-	-1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VSS	
RON	Output resistance	-	1.0	1.5	KΩ	V0 = +30V	Y1 ~ Y160 pins, |ΔVON| = 0.5V
		-	1.5	2.0	KΩ	V0 = +20V	
ISB	Stand-by current	-	-	5.0	μA	VSS pin, Note 1	
IDD1	Consumed current 1 (Non-selection)	-	-	2.0	mA	VDD pin, Note 2	
IDD2	Consumed current 2 (Selection)	-	-	8.0	mA	VDD pin, Note 3	
I0	Consumed current	-	-	1.0	mA	V0 pin, Note 4	

Common Mode (VSS=V5=0V, VDD=2.5~5.5V, V0=15~30V, Ta = -30 to +85°C, unless otherwise noted)

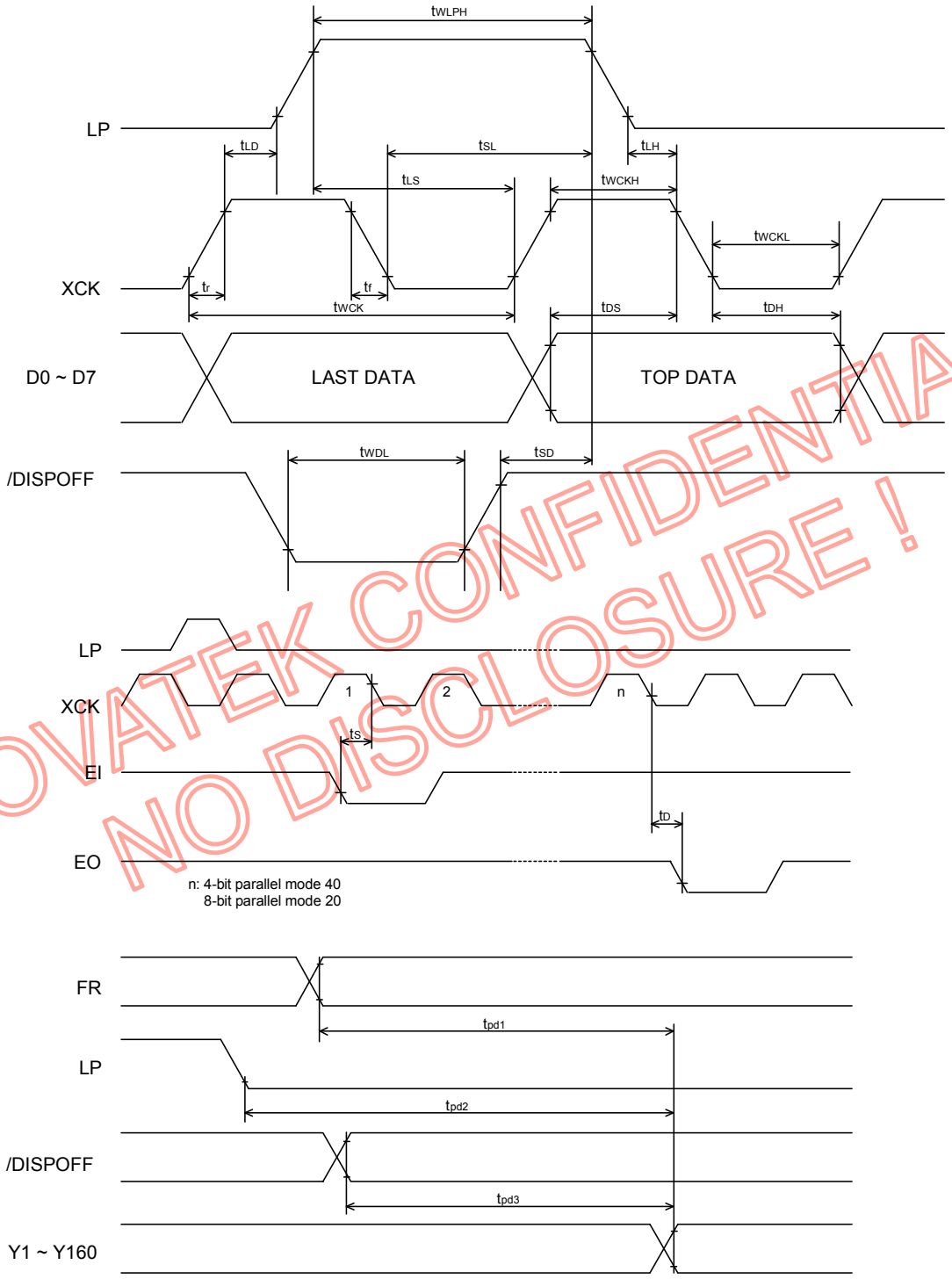
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.5	-	5.5	V	
V0	Operating Voltage	15	-	30	V	
VIH	Input high voltage	0.8 X VDD	-	-	V	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins
VIL	Input low voltage	-	-	0.2 X VDD	V	
VOH	Output high voltage	VDD - 0.4	-	-	V	EIO1, EIO2 pins, IOH = -0.4mA
VOL	Output low voltage	-	-	+0.4	V	EIO1, EIO2 pins, IOL = +0.4mA
IIH	Input leakage current 1	-	-	+1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VDD
IIL	Input leakage current 2	-	-	-1.0	μA	D0 ~ D7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and /DISPOFF pins, Vin = VSS
IPD	Input pull down current	-	-	100	μA	XCK, EIO1, EIO2, D7 pins
RON	Output resistance	-	1.0	1.5	KΩ	V0 = +30V | Y1 ~ Y160 pins, |ΔVON| = 0.5V
		-	1.5	2.0	KΩ	V0 = +20V | Y1 ~ Y160 pins, |ΔVON| = 0.5V
ISB	Stand-by current	-	-	5	μA	VSS pin, Note 5
IDD	Consumed current 1	-	-	80	μA	VDD pin, Note 6
I0	Consumed current 2	-	-	160	μA	V0 pin, Note 6

Notes:

1. VDD = +5.0V, V0 = +30V, Vin = VSS
2. VDD = +5.0V, V0 = +30V, fXCK = 14MHz, No-load, EIO = VDD
   The input data is turned over by the data taking clock (4-bit parallel input mode)
3. VDD = +5.0V, V0 = +30V, fXCK = 14MHz, No-load. EIO = VSS
   The input data is turned over by the data taking clock (4-bit parallel input mode)
4. VDD = +5.0V, V0 = +30V, fXCK = 14MHz, fLP = 41.6kHz. fFR = 80Hz, No-load
   The input data is turned over by the data taking clock (4-bit parallel-input mode)
5. VDD = +5.0V, V0 = +30V, Vin = VSS
6. VDD = +5.0V, V0 = +30V, fLP = 41.6KHz, fFR = 80Hz, case of 1/480 duty operation, No-load

AC Characteristics

1. Timing Characteristics of Segment Mode



Segment Mode 1 (VSS=V5=0V, VDD=4.5~5.5V, V0=15~30V, Ta = -30~+85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	71	-		ns	tr, tf ≤ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	23	-		ns	
Shift clock "L" pulse width	t_{WCKL}	23	-		ns	
Data setup time	t_{DS}	10	-		ns	
Data hold time	t_{DH}	20	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	23	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	25	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	25	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	25	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	21	-		ns	
/DISPOFF Removal time	t_{SD}	100	-		ns	
/DISPOFF enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	40	ns	CL=15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL=15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL=15pF

Note

1. Take the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is the maximum in the case of high speed operation.

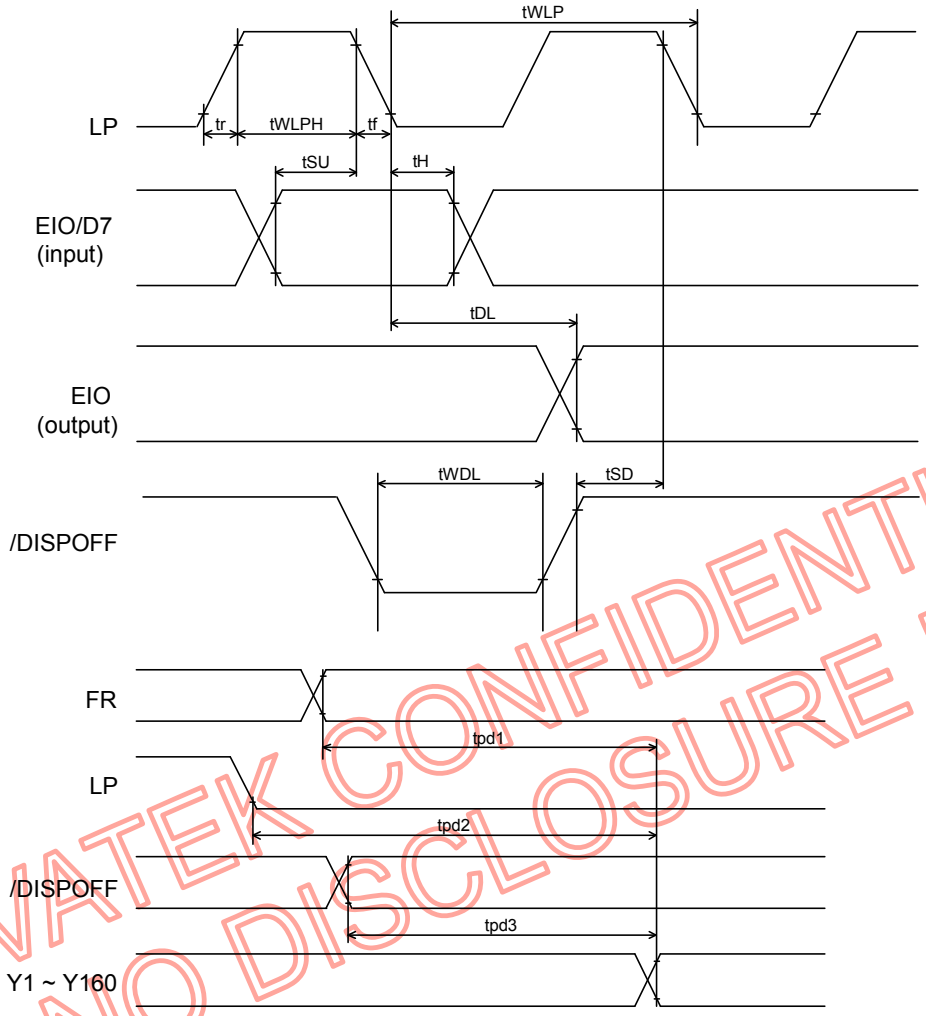
Segment Mode 2 (VSS=V5=0V, VDD=2.5~4.5V, V0=15~30V, Ta=-30~+85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	125	-		ns	tr, tf ≤ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	51	-		ns	
Shift clock "L" pulse width	t_{WCKL}	51	-		ns	
Data setup time	t_{DS}	30	-		ns	
Data hold time	t_{DH}	40	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	51	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	51	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	51	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	51	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	36	-		ns	
/DISPOFF Removal time	t_{SD}	100	-		ns	
/DISPOFF enable pulse width	t_{WDL}	1.2	-		µs	
Output delay time (1)	t_D		-	78	ns	CL=15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	µs	CL=15pF
Output delay time (3)	t_{pd3}		-	1.2	µs	CL=15pF

Note

1. Take the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is the maximum in the case of high speed operation.

2. Timing Characteristics of Common Mode

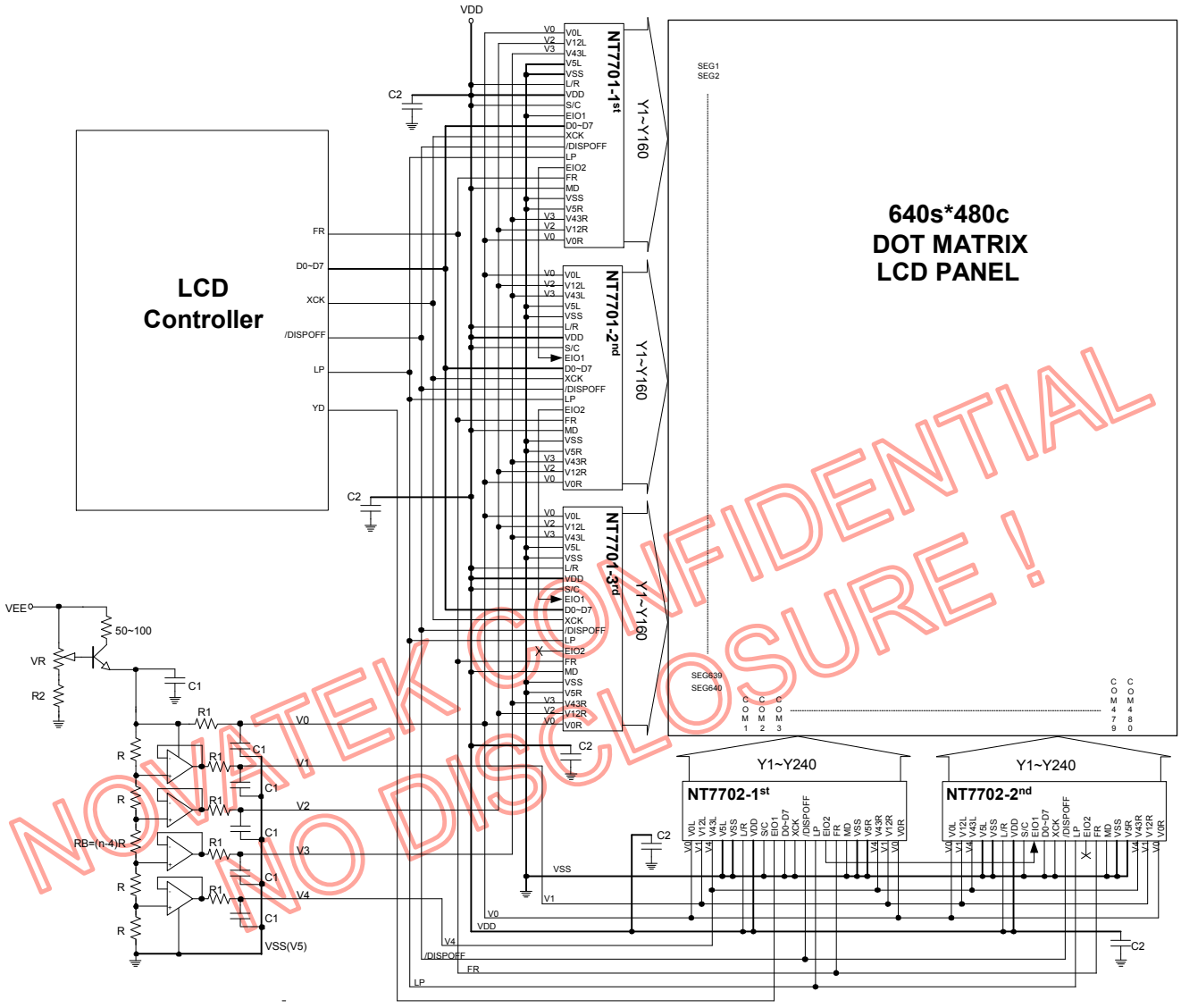


Common Mode (VSS=V5=0V, VDD=2.5~5.5V, V0=15~30V, Ta=-30~+85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	t_r, $t_f \leq$ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	VDD=5.0V±10%
		30	-	-	ns	VDD=2.5~4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	t_r		-	50	ns	
Input signal fall time	t_f		-	50	ns	
/DISPOFF Removal time	t_{SD}	100	-	-	ns	
/DISPOFF enable pulse width	t_{WDL}	1.2	-	-	µs	
Output delay time (1)	t_{DL}	-	-	200	ns	CL=15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	µs	CL=15pF
Output delay time (3)	t_{pd3}	-	-	1.2	µs	CL=15pF

Application Circuit (for reference only)

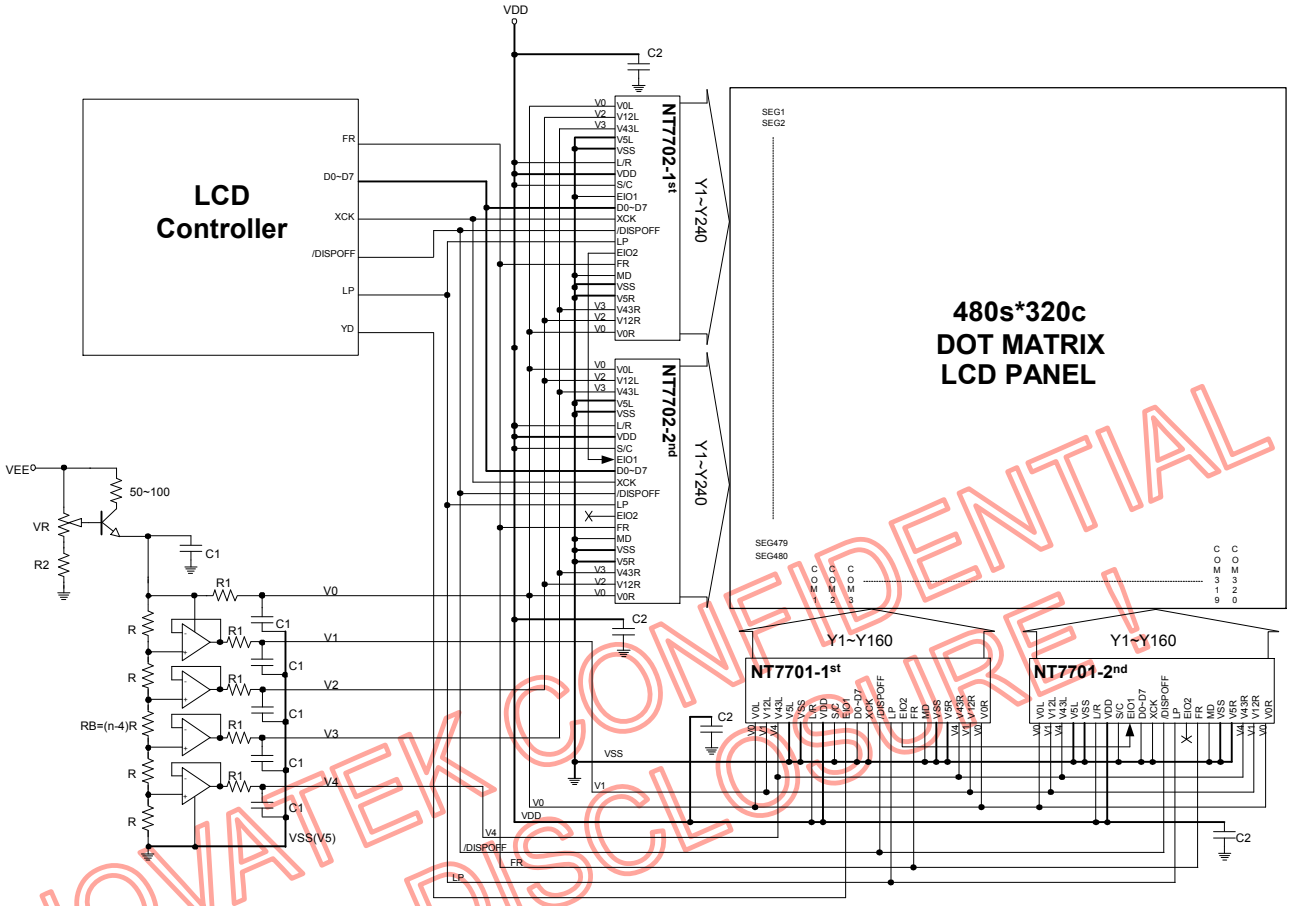
Segment Mode: (L/R=H、8bit mode)



Note

1. R=20KΩ~100KΩ
   Example of RB & R:
   → If R =20KΩ, bias=1/22, duty =1/480
   → RB =(22-4)*20KΩ
   =360KΩ
2. VR=50KΩ, R2=22KΩ(Adjust VR & R2 to get best range and contrast)
3. C1=2.2~4.7μF/50V(depend on LCD panel size), C2=0.1μF/10V, R1=15Ω.

Common Mode: (L/R=H、Single mode)



Note

1. R=20KΩ~100KΩ
   Example of RB & R:
   → If R =20KΩ, bias=1/18, duty=1/320
   → RB =(18-4)*20KΩ
   =280KΩ
2. VR=50KΩ, R2=22KΩ(Adjust VR & R2 to get best range and contrast)
3. C1=2.2~4.7μF/50V(depend on LCD panel size), C2=0.1μF/10V, R1=15Ω.

Application & ITO Layout Notice (for reference only)

Application Notices

1. Adjust the voltage of V1 and V4 you can amend the phenomena of “cross talk” (V1& V4 range of adjusting is less than 100mV, be sure V0-V1=V4-VSS after adjusting.
2. Add 0.1μf high frequency capacitors between VDD & V0 ~ V4 and VSS.
3. When OP (LP324) is used as following bias voltage, be sure OP power voltage must be 1.5V (or more) higher than output voltage.
4. XCK, D0~D7, LP are high frequency (Max. 14MHz) signals, pay attention to the distance between them and other signals nearby to avoid high frequency interference.
5. EIO1, EIO2 are enable signals for connecting chips, pay attention to the distance between them and other signals nearby to avoid interference. The distance of connection between two chips is the shorter better.

ITO Layout Notice（It is for application of COG type）

1. We suggest that the LCD panel is made of glass whose ITO resistor is about 15Ω/square, powers ITO are better if they are straight, its resistor value is the smaller the better.
2. Among interface Pins, first to be sure ITO resistors value of VDD, VSS and V0 ~ V4 are less than values we suggest. It is shown below:
   - ITO resistance value of power pins.

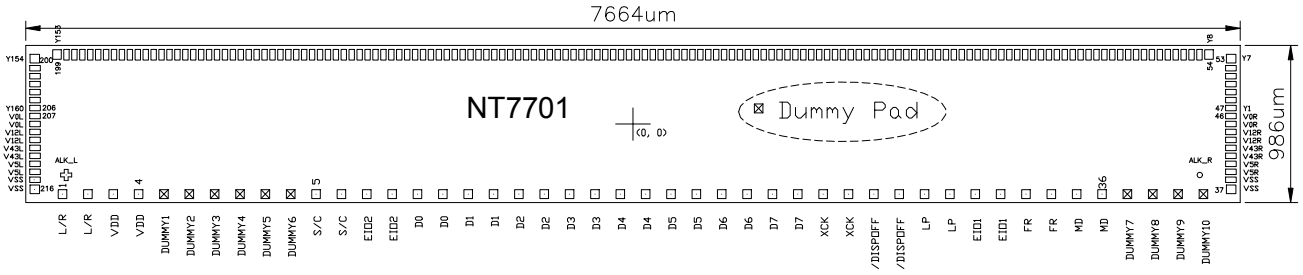
ITO path	Max. Resistance (Ω)	
	VDD＜2.7V	VDD≧2.7V
VDD	75	130
VSS	75	130
V0L(R)	200	
V12L(R)		
V43L(R)		
V5L(R)		

   - ITO resistance value of digital pins.

ITO path	Max. Resistance (Ω)
XCK, D0~D7, LP	500
EIO1, EIO2, FR, L/R, S/C, MD, /DISPOFF	1K

3. Single VSS and V0, V12, V43, V5 R/L are connected to FPC by ITO separately. At last shorten the distance of ITO by using metal on PCB.
4. VDD/VSS of IC and VDD/VSS of FPC are at the same vertical level as far as possible, ITO can be straight.
5. The distance of connection between IC to FPC is the shorter the better.

Bonding Diagram



Pad Location

unit: μm

Pad No.	Designation	X	Y
1	L/R	-3600	-440
2	L/R	-3440	-440
3	VDD	-3280	-440
4	VDD	-3120	-440
5	S/C	-2000	-440
6	S/C	-1840	-440
7	EIO2	-1680	-440
8	EIO2	-1520	-440
9	D0	-1360	-440
10	D0	-1200	-440
11	D1	-1040	-440
12	D1	-880	-440
13	D2	-720	-440
14	D2	-560	-440
15	D3	-400	-440
16	D3	-240	-440
17	D4	-80	-440
18	D4	80	-440
19	D5	240	-440
20	D5	400	-440
21	D6	560	-440
22	D6	720	-440
23	D7	880	-440
24	D7	1040	-440
25	XCK	1200	-440
26	XCK	1360	-440
27	/DISPOFF	1520	-440
28	/DISPOFF	1680	-440
29	LP	1840	-440
30	LP	2000	-440
31	EIO1	2160	-440
32	EIO1	2320	-440

Pad No.	Designation	X	Y
33	FR	2480	-440
34	FR	2640	-440
35	MD	2800	-440
36	MD	2960	-440
37	VSS	3779	-410
38	VSS	3779	-350
39	V5R	3779	-300
40	V5R	3779	-250
41	V43R	3779	-200
42	V43R	3779	-150
43	V12R	3779	-100
44	V12R	3779	-50
45	V0R	3779	0
46	V0R	3779	50
47	Y1	3779	100
48	Y2	3779	150
49	Y3	3779	200
50	Y4	3779	250
51	Y5	3779	300
52	Y6	3779	350
53	Y7	3779	410
54	Y8	3635	440
55	Y9	3575	440
56	Y10	3525	440
57	Y11	3475	440
58	Y12	3425	440
59	Y13	3375	440
60	Y14	3325	440
61	Y15	3275	440
62	Y16	3225	440
63	Y17	3175	440
64	Y18	3125	440

Pad Location (continued)

Pad No.	Designation	X	Y
65	Y19	3075	440
66	Y20	3025	440
67	Y21	2975	440
68	Y22	2925	440
69	Y23	2875	440
70	Y24	2825	440
71	Y25	2775	440
72	Y26	2725	440
73	Y27	2675	440
74	Y28	2625	440
75	Y29	2575	440
76	Y30	2525	440
77	Y31	2475	440
78	Y32	2425	440
79	Y33	2375	440
80	Y34	2325	440
81	Y35	2275	440
82	Y36	2225	440
83	Y37	2175	440
84	Y38	2125	440
85	Y39	2075	440
86	Y40	2025	440
87	Y41	1975	440
88	Y42	1925	440
89	Y43	1875	440
90	Y44	1825	440
91	Y45	1775	440
92	Y46	1725	440
93	Y47	1675	440
94	Y48	1625	440
95	Y49	1575	440
96	Y50	1525	440
97	Y51	1475	440
98	Y52	1425	440
99	Y53	1375	440
100	Y54	1325	440
101	Y55	1275	440
102	Y56	1225	440
103	Y57	1175	440
104	Y58	1125	440
105	Y59	1075	440
106	Y60	1025	440

Pad No.	Designation	X	Y
107	Y61	975	440
108	Y62	925	440
109	Y63	875	440
110	Y64	825	440
111	Y65	775	440
112	Y66	725	440
113	Y67	675	440
114	Y68	625	440
115	Y69	575	440
116	Y70	525	440
117	Y71	475	440
118	Y72	425	440
119	Y73	375	440
120	Y74	325	440
121	Y75	275	440
122	Y76	225	440
123	Y77	175	440
124	Y78	125	440
125	Y79	75	440
126	Y80	25	440
127	Y81	-25	440
128	Y82	-75	440
129	Y83	-125	440
130	Y84	-175	440
131	Y85	-225	440
132	Y86	-275	440
133	Y87	-325	440
134	Y88	-375	440
135	Y89	-425	440
136	Y90	-475	440
137	Y91	-525	440
139	Y92	-575	440
139	Y93	-625	440
140	Y94	-675	440
141	Y95	-725	440
142	Y96	-775	440
143	Y97	-825	440
144	Y98	-875	440
145	Y99	-925	440
146	Y100	-975	440
147	Y101	-1025	440
148	Y102	-1075	440

Pad Location (continued)

Pad No.	Designation	X	Y
149	Y103	-1125	440
150	Y104	-1175	440
151	Y105	-1225	440
152	Y106	-1275	440
153	Y107	-1325	440
154	Y108	-1375	440
155	Y109	-1425	440
156	Y110	-1475	440
157	Y111	-1525	440
158	Y112	-1575	440
159	Y113	-1625	440
160	Y114	-1675	440
161	Y115	-1725	440
162	Y116	-1775	440
163	Y117	-1825	440
164	Y118	-1875	440
165	Y119	-1925	440
166	Y120	-1975	440
167	Y121	-2025	440
168	Y122	-2075	440
169	Y123	-2125	440
170	Y124	-2175	440
171	Y125	-2225	440
172	Y126	-2275	440
173	Y127	-2325	440
174	Y128	-2375	440
175	Y129	-2425	440
176	Y130	-2475	440
177	Y131	-2525	440
178	Y132	-2575	440
179	Y133	-2625	440
180	Y134	-2675	440
181	Y135	-2725	440
182	Y136	-2775	440
183	Y137	-2825	440

Pad No.	Designation	X	Y
184	Y138	-2875	440
185	Y139	-2925	440
186	Y140	-2975	440
187	Y141	-3025	440
188	Y142	-3075	440
189	Y143	-3125	440
190	Y144	-3175	440
191	Y145	-3225	440
192	Y146	-3275	440
193	Y147	-3325	440
194	Y148	-3375	440
195	Y149	-3425	440
196	Y150	-3475	440
197	Y151	-3525	440
198	Y152	-3575	440
199	Y153	-3635	440
200	Y154	-3779	410
201	Y155	-3779	350
202	Y156	-3779	300
203	Y157	-3779	250
204	Y158	-3779	200
205	Y159	-3779	150
206	Y160	-3779	100
207	V0L	-3779	50
208	V0L	-3779	0
209	V12L	-3779	-50
210	V12L	-3779	-100
211	V43L	-3779	-150
212	V43L	-3779	-200
213	V5L	-3779	-250
214	V5L	-3779	-300
215	VSS	-3779	-350
216	VSS	-3779	-410
	ALK_L	-3577	-320
	ALK_R	3577	-320

Dummy Pad Location (Total: 10 pads)

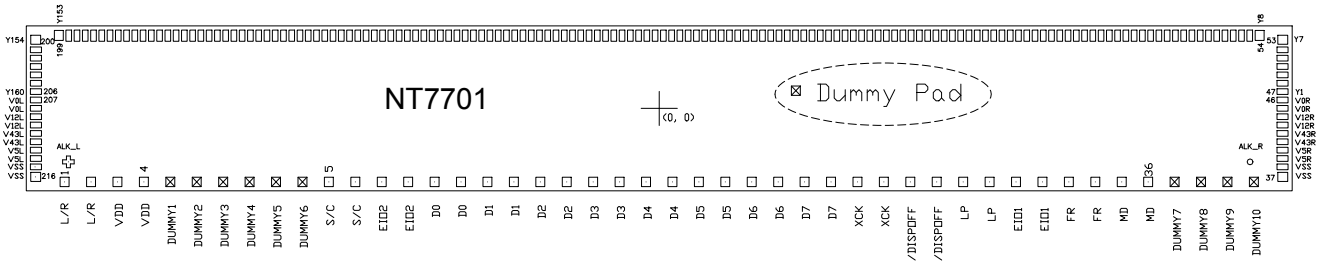
NO	X	Y
1	-2960	-440
2	-2800	-440
3	-2640	-440

NO	X	Y
4	-2480	-440
5	-2320	-440
6	-2160	-440

NO	X	Y
7	3120	-440
8	3280	-440
9	3440	-440

NO	X	Y
10	3600	-440

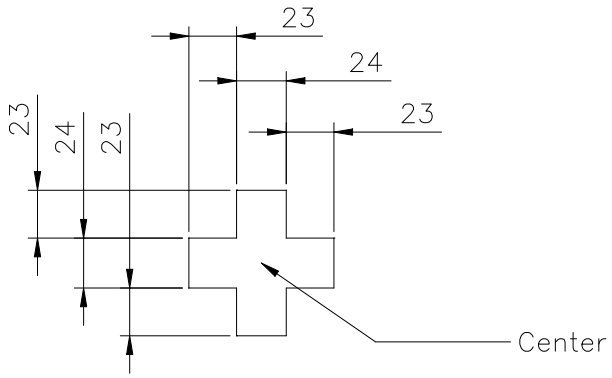
Package Information



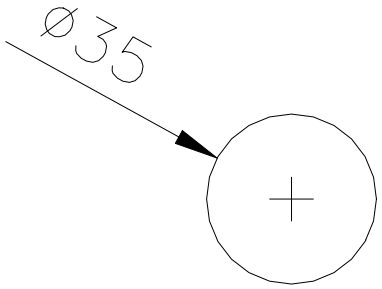
Pad Dimensions

	Pad No.	Size		UNIT
		X	Y	
Chip size	-	7664	986	μm
Chip thickness	-	525		μm
Pad pitch	1~36	160		μm
	37~38, 52~53, 54~55 198~199, 200~201, 215~216	60		
	38~52, 55~198, 201~215	50		
Bump size	1~36, Dummy pads	54	56	μm
	37, 53, 200, 216	60	52	
	54, 199	52	60	
	38~52, 201~215	67	32	
	55~198	32	67	
Bump height	All pads	15±3		μm

Alignment Marks: (Unit : μm)



ALK_L



ALK_R

Ordering Information

Part No.	Package
NT7701H-BDT	Au bump on chip tray
NT7701H-TABF1	TCP form
NT7701H-TABF2	TCP form
NT7701H-TABF3	TCP form

Cautions

1. The contents of this document are subject to change without notice.
2. Precautions against light projection:
   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.
   Observe the following instructions in using this product:
   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
   b. Test and inspect the product under an environment free of light source penetration.
   c. Confirm that all surfaces around the IC will not be exposed to a light source.