Table of Contents

Revision History

Date	Contents
2008-06-10	Preliminary spec version 0.1. First release.
2008-10-29	Preliminary spec version 0.2. Features update.
2009-02-15	Preliminary spec version 0.3. Features update.
2009-02-16	Preliminary spec version 0.4. Features update.
2009-04-15	Preliminary spec version 0.5. Add General Description, Block Diagram, Pin Configuration, Pin Descriptions, Package Outline & Electrical Characteristics.
2009-04-22	Preliminary spec version 0.6. Modify Features, General Description, Block Diagram & Electrical Characteristics.
2009-05-22	Preliminary spec version 0.7. Modofy HDMI power from 3.3V to 1.2V.
2009-06-03	Preliminary spec version 0.8. Modofy HDMI_REXT pin description.
2009-07-31	Preliminary spec version 0.8. Modofy some pin descriptions & add Electrical Characteristics.

Features

■ High Performance 32-bit CPU

- □ ARM v4 compatible
- □ MPU embedded
- □ 8KB instruction and 8KB data cache
- □ Embedded ICE makes firmware debugging easier

■ Power Management

- □ Firmware configurable operating frequency of each functional block to meet best power budget
- □ CPU operating frequency up to 300MHz, on the fly programmable

■ Integrated Clock Generator

- □ Internal PLL
- □ 12MHz system/USB oscillator
- □ 11.296 / 12.288 MHz oscillator for Digital Audio Interface
- □ 32768Hz RTC oscillator

■ Scaleable Memory Bus Architecture

- □ 16-bit DDR I / DDR II SDRAM bus, supporting up to 1Gb DDR SDRAM
- □ 8-bit static memory bus, supporting up to 4MB

■ LCD/TV Display

- □ High performance scaling up/down engine and programmable gamma correction for LCD or TV display
- □ Support digital LCD interface for AU, Casio new panels (all digital panels will be supported) and Toppoly
- □ Support PAL / NTSC video encoder
  - ➢ NTSC-M
  - ➢ PAL-BDGHI
  - ➢ PAL-M
  - ➢ PAL-NC
- □ Integrated 1 internal 10-bit video DACs
- □ Support digital interface CCIR601/656 output port
- □ Support 24-bit RGB parallel interface, up to 1024x768 resolution
- □ Support YCbCr to RGB color conversion
- □ Multistandard video output support:
  - ➢ Composite (CVBS)
- □ Support HDMI interface

- 24-bit RBG, YCbCr 444, YCbCr 422 output
- 1 ports of IIS audio outputs

□ 3.3V / 1.8V LCD / Digital video out

■ HDMI

□ Support HDMI v1.3a

□ Support DDC with maximum 100khz access rate for CEA-861-D format

□ Support CEC

□ Support 16 bits PCM 32 KHz, 44.1 KHz, 48KHz for maximum 2 channels audio output

□ Support 480p, 576p and 720p video output

■ Sensor Interface Engine

□ Support up to 32Mp CCD/CMOS image sensor

□ Support 12-bit CCD AFE input

□ Support pixel clock up to 96MHz

□ Support CCD/CMOS RGB Image Sensor

- CCD: SONY, Sharp, Panasonic
- CMOS: Aptina, OVT

□ Support movie CCD, and horizontal division CCD of SONY.

□ Support multiple field, line interleaved CCD of Sharp

□ Built-in color pattern generation

□ Sensor black level clamping

□ Efficient defect concealment algorithm

□ Raw image sub-sample for video

□ R/G/B Gamma LUT

□ Flexible image analysis flow for AE, AF and AWB purpose

- Programmable AE/AWB window
- 16x16 AF window
- Programmable histogram

□ Flash light control

□ Lens shading compensation technology

□ Geometric distortion correction technology

□ Support in-pipeline color shading compensation

□ Support in-frame dark frame subtraction with smart defect detection algorithm

□ Pixel binning for high ISO

■ Image Processing Engine

□ Proprietary anti-alias Bayer CFA color interpolation

- □ Flexible edge rendering, control and enhancement
- □ Powerful noise reduction technology
- □ Flexible image analysis flow for AE, AF and AWB purpose (i.e. intensity histogram, and more)
- □ R/G/B Gamma LUT
- □ High precision color correction matrix for sRGB or specific color requirement
- □ Brightness/contrast and hue/saturation adjustment
- □ Specific color control technology (Patent Pending)
- □ Same preview and capture paths
- □ False color suppression
- □ Advanced chroma noise reduction algorithm

■ Image Manipulation Engine

- □ High quality scaling engine for digital zooming
- □ Support thumb nail image generation
- □ Forward/inverse color space transform
- □ Seamless digital zoom

■ Face Detection Engine

- □ Very high speed face detection and tracking
- □ High accuracy under different light source
- □ Programmable target data base

■ Digital Image Stabilizer

- □ Remove unintended hand movement from an image sequence
- □ Single frame compensation for video (Total compensation)
- □ Accumulate frame compensation for video (Smart compensation)
- □ Interface search range up to ±32
- □ Programmable total compensation range
- □ Accommodate resolution 720p
- □ For Motion Detection, adjustable number of motion vectors. Maximum 256 motion vectors per process (16 regions x 16 blocks/region).

■ Image Related HW Engine

- □ Face detection
- □ Lens geometric compensation

■ Graphic Engine

- □ Copy and paste
- □ Geometric operation including mirror, flip and rotation
- □ Arithmetic operation including addition, subtraction, color keying, logic operation and alpha

blending

■ Cipher

- □ 64-bit DES, 3DES, and AES-128
- □ Both encryption and decryption
- □ Big and little endian of input data

■ H.264/AVC CODEC

- □ Real-time capability up to 720p 30fps or 480p 60fps
- □ H.264 main profile
  - ➢ B-frame
  - ➢ CABAC
- □ 1 reference picture for P-frame, 2 reference pictures for B-frame

■ Motion Estimation

- □ [-140.75,+140.75] search range in horizontal component
- □ [-70.75, +70.75] search range in vertical component
- □ MB mode: 16x16, 16x8, 8x16, 8x8, skip, and direct (B-frame)

■ F/W Audio CODEC

- □ Dolby Digital Consumer Encoding (DDCE) also known as AC-3(2) 2 channel audio encoding at 256 kbit/s or 384 kbit/s
- □ MPEG-1 layer 2 audio encoding at 256 kbit/s or 384 kbit/s
- □ MPEG-4 AAC audio encoding at 256 kbit/s or 384 kbit/s
- □ Noise cancellation for lens operation, HD access and wind
- □ Linear Pulse Code Modulation (LPCM)

■ H/W Audio CODEC

- □ stereo 16-bits ADC audio recording
- □ stereo 16-bits DAC audio playback
- □ Programmable ALC / Noise Gate I
- □ Audio sampling rate : 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48kHz
- □ On-chip speaker driver / stereo headphone drive

■ JPEG CODEC

- □ Supports Motion JPEG 30fps@720P30 video clip/playback function
- □ Support ISO/IEC 10918-1 baseline JPEG compression/decompression. The still image resolutions will be up to 16,384x8,192 pixels
- □ JPEG supports downloadable Quantization and Huffman tables
- □ Support Exchangeable Image File format (EXIF 2.2)

■ 8/16-Bit Digital Video I/O Port

- □ Provides a real-time uncompressed video interface to support a broad range of component digital formats including YUV, RGB
- □ CCIR601/656 digital video input/Private digital video input

■ ATA/ATAPI-6 Host Controller

- □ Support PIO mode 0, 1, 2, 3, and 4, data transfer rate up to 16.6MB/s
- □ Support ultra DMA modes 0, 1, 2, 4,and 5 data transfer rate up to 100MB/s
- □ Support TrueIDE mode for Compact FlashANSI ATA/ATAPI-6

■ Digital Audio Interface

- □ Support of AC97 codec interface (AC-Link), I2S codec interface
- □ Support full duplex
- □ Support ADPCM, uLaw coding/decoding
- □ Audio clock generator

■ Dual Graphic-based OSD

- □ Support 8-bit palette and 32-bit ARGB OSD architecture
- □ 256 colors simultaneously out of true color at 8-bit palette OSD
- □ 8 levels of opacity for 8-bit palette OSD
- □ Programmable width & height to meet LCD/TV's resolution exactly
- □ Picture in picture function

■ Memory Card Controller

- □ Compact flash card with PC card memory mode and True-IDE mode
- □ Secure Digital card
  - ➢ Support SD 2.0
  - ➢ Capacity up to 128GB
  - ➢ Bus clock up to 48MHz
- □ Multi-Media card
  - ➢ Support MMC 4.2
  - ➢ Capacity up to 128GB
  - ➢ Bus clock up to 48MHz
  - ➢ 8 bits data bus
- □ Memory Stick Pro card
  - ➢ Support Memory Stick PRO-HG 1.01.00
  - ➢ Capacity up to 32GB
  - ➢ Bus clock up to 60MHz
  - ➢ 8 bits data bus
- □ Smart Media card

- ➢ Capacity up to 8TB
- ➢ Bus clock up to 60MHz

□ MLC / SLC NAND type flash

- ➢ Capacity up to 8TB
- ➢ Support SLC with page size 512/2K Bytes
- ➢ Support MLC with page size 512/2K/4K Bytes
- ➢ Bus clock up to 60MHz

□ xD picture card

- ➢ Capacity up to 8TB
- ➢ Support normal Type / M Type / H Type xD card
- ➢ Bus clock up to 60MHz

■ USB

- □ Fully compliant with USB2.0 OTG
- □ High speed (480Mbps) supported
- □ Optionally switchable to be fully compliant with USB 1.1
- □ Support Control / Isochronous / Interrupt and Bulk transfer
- □ Support PC camera mode

■ Timers

- □ RTC can be powered by separate backup battery and operating from 1.5V to 3.6V
- □ Watch dog timer

■ Peripheral Interface

- □ Support I2C interface
- □ Support GPIO and flexible PWM interface with DC motor control
- □ Support programmable 3-wired serial interface
- □ Support UART interface
  - ➢ Support UART function with/without hardware flow control which data rate is up to 3Mbps (4/2 pins)
  - ➢ Support Modem function which data rate is up to 3Mbps (8 pins)
  - ➢ Support IrDA interface which can support SIR mode up to 115200bps and FIR mode up to 4Mbps (2 pins)
- □ Support 8 channels of 10-bit ADC with touch panel interface(2 channels), the max. sample rate up to 62.5 KHz per channel

■ On-chip Boot Strap Loader

- □ Built-in on-chip mask ROM
- □ User program can be stored in NAND-type flash and external static memory is not necessary

- On-chip mask ROM can be disabled
- System can boot from internal/external ROM, serial ROM, NAND flash, memory cards and USB

Triple Voltage Power Supply

- 1.2V core logic voltage
- 2.5V / 1.8V DDRI / DDRII SDRAM interface voltage
- 3.3V I/O interface and analog circuit voltage

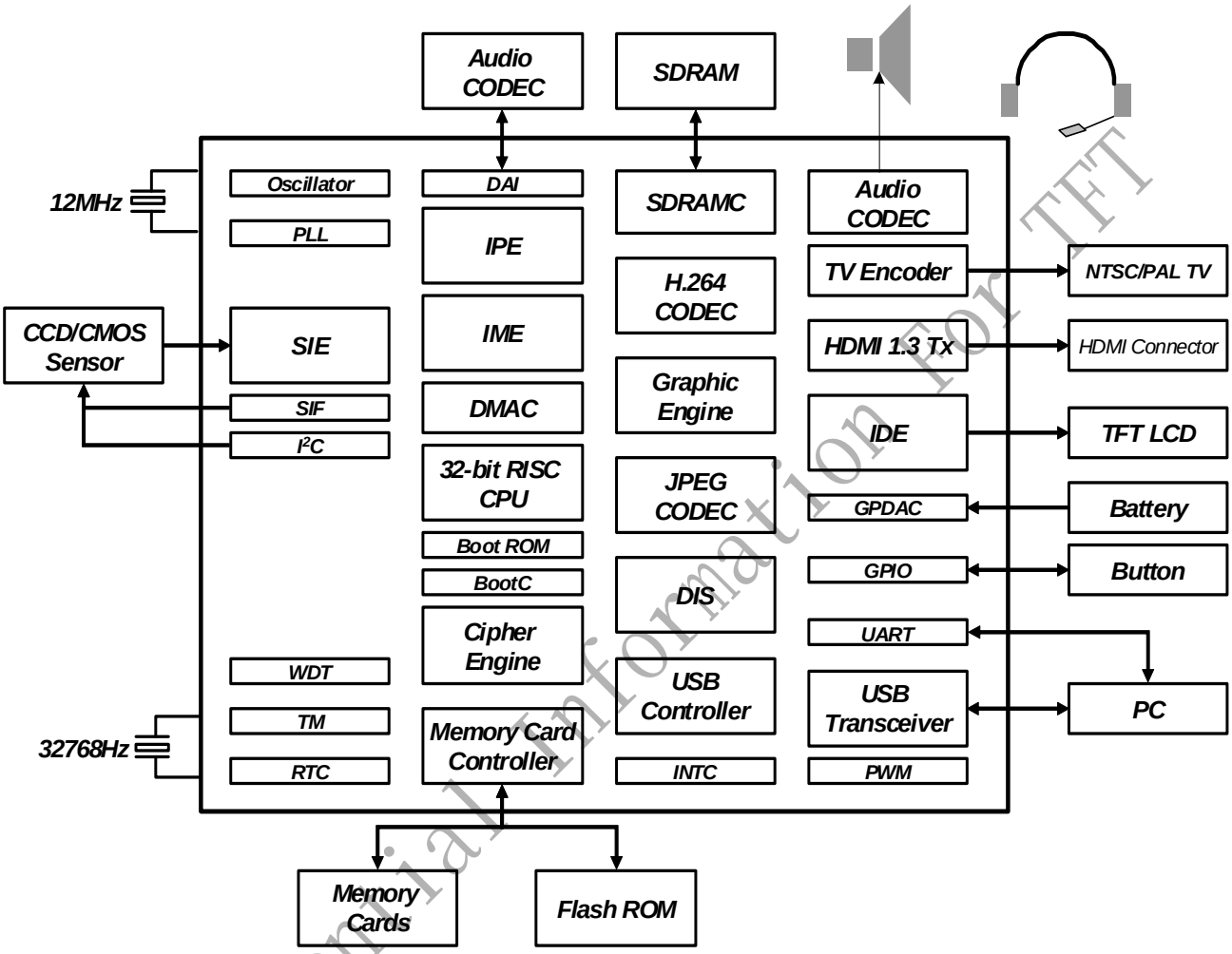
Package

- NT96630BG: 352 ball TFBGA, 15x15 mm^2
- NT96632BG: 297 ball TFBGA, 13x13 mm^2

General Description

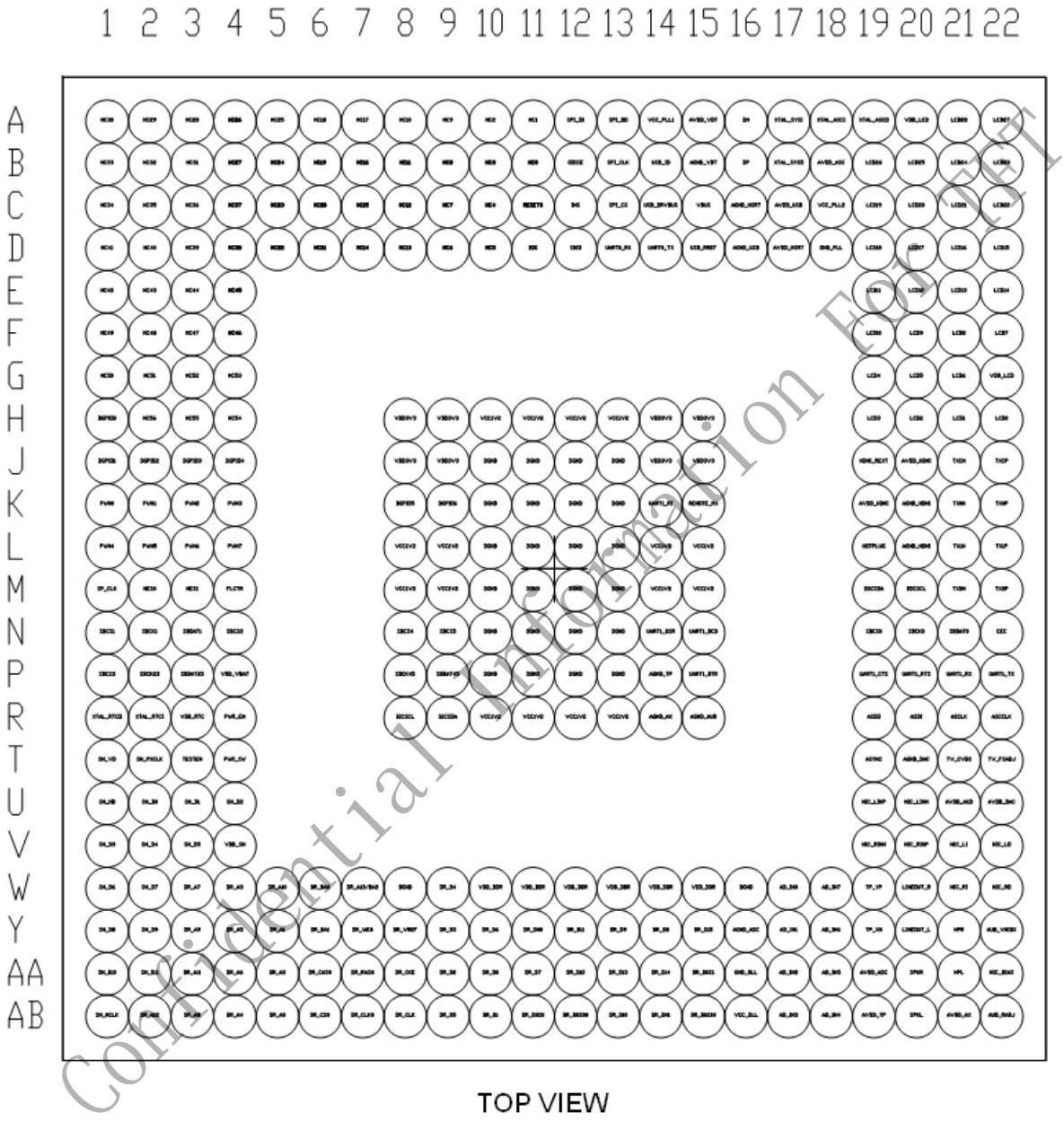
NT96630BG/NT96632BG is a high image quality, high performance, and cost effective digital still camera (DSC) or digital video camera (DV) with excellent digital still image capturing and video streaming capabilities. It is targeted for the application of VGA to 32M pixel DSC/DV resolutions. It can be easily adapted to many CCD and CMOS sensor with on chip programmable interface timing approach. The controller provides sophisticated video processing methods with built-in hardware acceleration pipeline. This is essential for achieving high performance for per-shot, shot-to-shot, and continuous shooting pictures. The controller provides flexible mechanism for auto white balance, auto exposure and auto-focusing in order to better tradeoff hardware and software efforts over the performance. Hardware H.264 video CODEC is embedded with HD resolution. The HDMI 1.3 Tx is also equipped for HDTV output. The interface to CF, SD/MMC, MS/MS-pro, SMC, and xD makes it ideal for the storage of still pictures and video streaming data. The USB2.0 high speed interface can upload/download the audio/video data efficiently to/from PC.

Block Diagram



Pin Configuration

NT96630BG: TFBGA-352



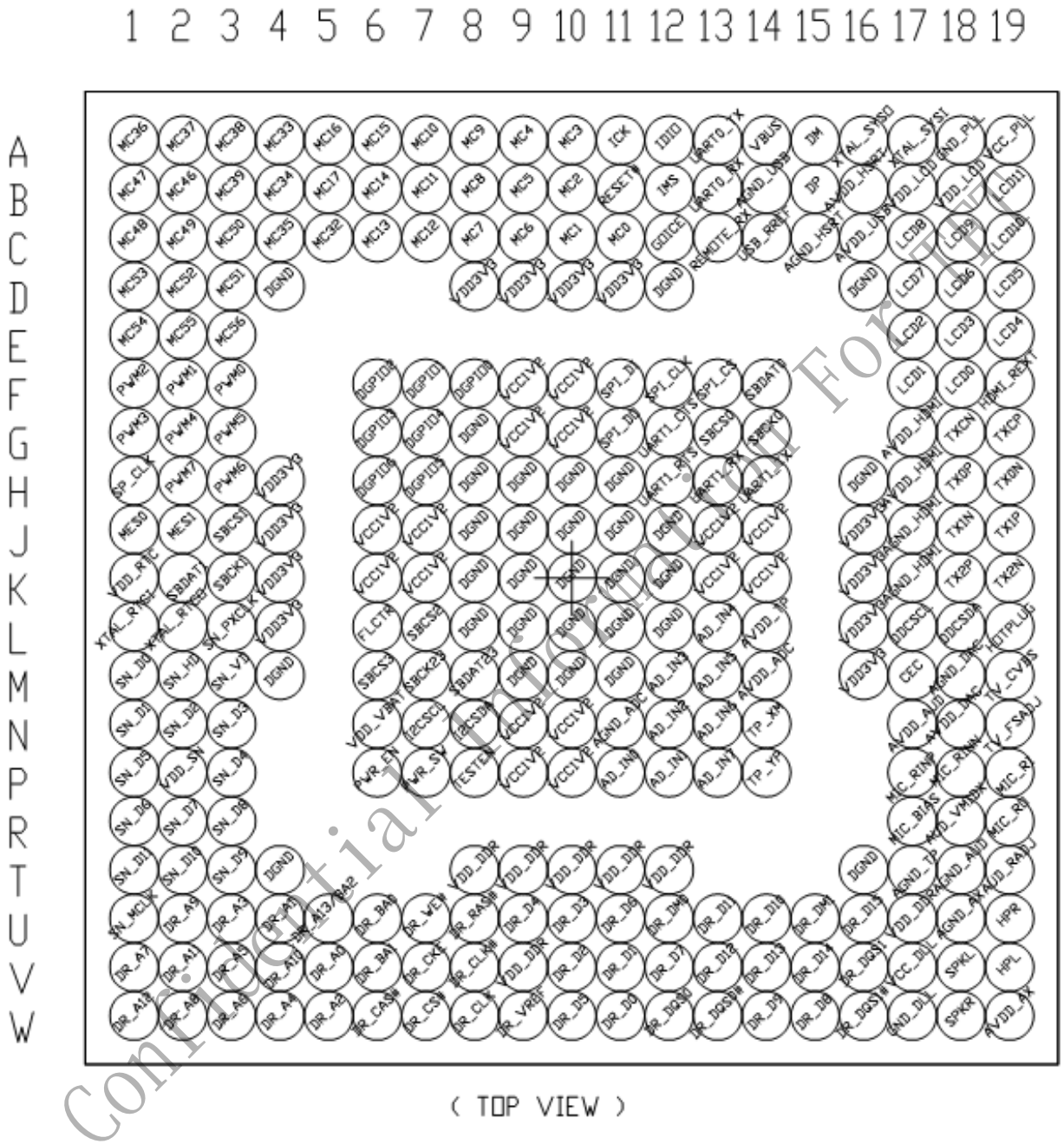
TOP VIEW

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
B11	MC0	T19	ASYNC	K21	TX0N	H10	VCC1V2
A11	MC1	R19	ASDO	L22	TX1P	H11	VCC1V2
A10	MC2	R20	ASDI	L21	TX1N	H12	VCC1V2
B10	MC3	R21	ASCLK	M22	TX2P	H13	VCC1V2

C10	MC4	N19	SBCS0	M21	TX2N	L8	VCC1V2
D10	MC5	N20	SBCK0	J19	HDMI_REXT	L9	VCC1V2
D9	MC6	N21	SBDAT0	N22	CEC	L14	VCC1V2
C9	MC7	N1	SBCS1	M19	DDCSDA	L15	VCC1V2
B9	MC8	N2	SBCK1	M20	DDCSCL	M8	VCC1V2
A9	MC9	N3	SBDAT1	L19	HOTPLUG	M9	VCC1V2
A8	MC10	N4	SBCS2	V20	MIC_RINP	M14	VCC1V2
B8	MC11	P1	SBCS3	V19	MIC_RINN	M15	VCC1V2
C8	MC12	P2	SBCK23	U19	MIC_LINP	R10	VCC1V2
D8	MC13	P3	SBDAT23	U20	MIC_LINN	R11	VCC1V2
D7	MC14	N8	SBCS4	AA22	MIC_BIAS	R12	VCC1V2
C7	MC15	N9	SBCS5	W21	MIC_RI	R13	VCC1V2
B7	MC16	P8	SBCK45	V21	MIC_LI	H8	VDD3V3
A7	MC17	P9	SBDAT45	W22	MIC_RO	H9	VDD3V3
A6	MC18	D14	UART_TX	V22	MIC_LO	H14	VDD3V3
B6	MC19	D13	UART_RX	Y22	AUD_VMIDX	H15	VDD3V3
C6	MC20	P22	UART2_TX	AB22	AUD_RADJ	J8	VDD3V3
D6	MC21	P21	UART2_RX	Y21	HPR	J9	VDD3V3
D5	MC22	P20	UART2_RTS	AA21	HPL	J14	VDD3V3
C5	MC23	P19	UART2_CTS	W20	LINEOUT_R	J15	VDD3V3
B5	MC24	P15	UART2_DTR	Y20	LINEOOUT_L	V4	VDD_SN
A5	MC25	N14	UART2_DSR	AA20	SPKR	A20	VDD_LCD
A4	MC26	N15	UART2_DCD	AB20	SPKL	G22	VDD_LCD
B4	MC27	K14	UART2_RI	A17	XTAL_SYSI	J10	DGND
A3	MC28	C13	SPI_CS	B17	XTAL_SYSO	J11	DGND
A2	MC29	B13	SPI_CLK	A18	XTAL_ASCI	J12	DGND
A1	MC30	A13	SPI_DO	A19	XTAL_ASCO	J13	DGND
B3	MC31	A12	SPI_DI	C11	RESET#	K10	DGND
B2	MC32	K15	REMOTE_RX	D12	IDIO	K11	DGND
B1	MC33	H22	LCD0	B12	GOICE	K12	DGND
C1	MC34	H21	LCD1	C12	IMS	K13	DGND
C2	MC35	H20	LCD2	D11	ICK	L10	DGND
C3	MC36	H19	LCD3	H1	DGPIO0	L11	DGND
C4	MC37	G19	LCD4	J1	DGPIO1	L12	DGND
D4	MC38	G20	LCD5	J2	DGPIO2	L13	DGND
D3	MC39	G21	LCD6	J3	DGPIO3	M10	DGND
D2	MC40	F22	LCD7	J4	DGPIO4	M11	DGND
D1	MC41	F21	LCD8	K8	DGPIO5	M12	DGND
E1	MC42	F20	LCD9	K9	DGPIO6	M13	DGND
E2	MC43	F19	LCD10	AA10	DR_D0	N10	DGND
E3	MC44	E19	LCD11	AB10	DR_D1	N11	DGND
E4	MC45	E20	LCD12	AA9	DR_D2	N12	DGND
F4	MC46	E21	LCD13	Y9	DR_D3	N13	DGND
F3	MC47	E22	LCD14	W9	DR_D4	P10	DGND
F2	MC48	D22	LCD15	AB9	DR_D5	P11	DGND
F1	MC49	D21	LCD16	Y10	DR_D6	P12	DGND
G1	MC50	D20	LCD17	AA11	DR_D7	P13	DGND
G2	MC51	D19	LCD18	Y14	DR_D8	W8	DGND
G3	MC52	C19	LCD19	Y13	DR_D9	W16	DGND
G4	MC53	C20	LCD20	AB13	DR_D10	AA19	AVDD_ADC
H4	MC54	C21	LCD21	Y12	DR_D11	Y16	AGND_ADC
H3	MC55	C22	LCD22	AA12	DR_D12	U22	AVDD_DAC
H2	MC56	B22	LCD23	AA13	DR_D13	T20	AGND_DAC
T2	SN_PXCLK	B21	LCD24	AA14	DR_D14	U21	AVDD_AUD
T1	SN_VD	B20	LCD25	Y15	DR_D15	R15	AGND_AUD
U1	SN_HD	B19	LCD26	AB5	DR_A0	AB21	AVDD_AX
U2	SN_D0	A22	LCD27	Y5	DR_A1	R14	AGND_AX
U3	SN_D1	A21	LCD28	AA5	DR_A2	D17	AVDD_HSRT
U4	SN_D2	W17	AD_IN0	W4	DR_A3	C16	AGND_HSRT
V1	SN_D3	Y17	AD_IN1	AB4	DR_A4	C17	AVDD_USB
V2	SN_D4	AA17	AD_IN2	Y4	DR_A5	D16	AGND_USB
V3	SN_D5	AB17	AD_IN3	AA4	DR_A6	A15	AVDD_VDT
W1	SN_D6	AB18	AD_IN4	W3	DR_A7	B15	AGND_VDT

W2	SN_D7	AA18	AD_IN5	AB3	DR_A8	R3	VDD_RTC
Y1	SN_D8	Y18	AD_IN6	Y3	DR_A9	P4	VDD_VBAT
Y2	SN_D9	W18	AD_IN7	W5	DR_A10	A14	VCC_PLL1
AA1	SN_D10	W19	TP_YP	AA3	DR_A11	C18	VCC_PLL2
AA2	SN_D11	Y19	TP_XM	AB2	DR_A12	D18	GND_PLL
AB1	SN_MCLK	C15	VBUS	W7	DR_A13/BA2	AB16	VCC_DLL
M1	SP_CLK	A16	DM	W6	DR_BA0	AA16	GND_DLL
M2	MES0	B16	DP	Y6	DR_BA1	W10	VDD_DDR
M3	MES1	D15	USB_RREF	AA6	DR_CAS#	W11	VDD_DDR
M4	FLCTR	B14	USB_ID	AA7	DR_RAS#	W12	VDD_DDR
K1	PWM0	C14	USB_DRVBUS	Y7	DR_WE#	W13	VDD_DDR
K2	PWM1	T4	PWR_SW	AB6	DR_CS#	W14	VDD_DDR
K3	PWM2	R4	PWR_EN	Y11	DR_DM0	W15	VDD_DDR
K4	PWM3	R2	XTAL_RTCI	AB14	DR_DM1	Y8	VDD_VREF
L1	PWM4	R1	XTAL_RTCO	AB11	DR_DQS0	B18	AVDD_ASC
L2	PWM5	T3	TESTEN	AA15	DR_DQS1	AB19	AVDD_TP
L3	PWM6	T22	TV_FSADJ	AB12	DR_DQS0#	P14	AGND_TP
L4	PWM7	T21	TV_CVBS	AB15	DR_DQS1#	J20	AVDD_HDMI
R9	I2CSDA	J22	TXCP	AB8	DR_CLK	K19	AVDD_HDMI
R8	I2CSCL	J21	TXCN	AB7	DR_CLK#	K20	AGND_HDMI
R22	ASCCLK	K22	TX0P	AA8	DR_CKE	L20	AGND_HDMI

NT96632BG: TFBGA-297



Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
C11	MC0	M6	SBCS3	A12	IDIO	D10	VDD3V3
C10	MC1	M7	SBCK23	C12	GOICE	D11	VDD3V3
B10	MC2	M8	SBDAT23	B12	IMS	H4	VDD3V3
A10	MC3	A13	UART_TX	A11	ICK	J4	VDD3V3
A9	MC4	B13	UART_RX	F8	DGPIO0	J16	VDD3V3

B9	MC5	H14	UART2_TX	F7	DGPIO1	K4	VDD3V3
C9	MC6	H13	UART2_RX	F6	DGPIO2	K16	VDD3V3
C8	MC7	H12	UART2_RTS	G6	DGPIO3	L4	VDD3V3
B8	MC8	G12	UART2_CTS	G7	DGPIO4	L16	VDD3V3
A8	MC9	F13	SPI_CS	H7	DGPIO5	M16	VDD3V3
A7	MC10	F12	SPI_CLK	H6	DGPIO6	P2	VDD_SN
B7	MC11	G11	SPI_DO	W11	DR_D0	B17	VDD_LCD
C7	MC12	F11	SPI_DI	V11	DR_D1	B18	VDD_LCD
C6	MC13	C13	REMOTE_RX	V10	DR_D2	D4	DGND
B6	MC14	F18	LCD0	U10	DR_D3	D12	DGND
A6	MC15	F17	LCD1	U9	DR_D4	D16	DGND
A5	MC16	E17	LCD2	W10	DR_D5	G8	DGND
B5	MC17	E18	LCD3	U11	DR_D6	H8	DGND
C5	MC32	E19	LCD4	V12	DR_D7	H9	DGND
A4	MC33	D19	LCD5	W15	DR_D8	H10	DGND
B4	MC34	D18	LCD6	W14	DR_D9	H11	DGND
C4	MC35	D17	LCD7	U14	DR_D10	H16	DGND
A1	MC36	C17	LCD8	U13	DR_D11	J8	DGND
A2	MC37	C18	LCD9	V13	DR_D12	J9	DGND
A3	MC38	C19	LCD10	V14	DR_D13	J10	DGND
B3	MC39	B19	LCD11	V15	DR_D14	J11	DGND
B2	MC46	P11	AD_IN0	U16	DR_D15	J12	DGND
B1	MC47	P12	AD_IN1	V5	DR_A0	K8	DGND
C1	MC48	N12	AD_IN2	U4	DR_A1	K9	DGND
C2	MC49	M12	AD_IN3	W5	DR_A2	K10	DGND
C3	MC50	L13	AD_IN4	U3	DR_A3	K11	DGND
D3	MC51	M13	AD_IN5	W4	DR_A4	K12	DGND
D2	MC52	N13	AD_IN6	V3	DR_A5	L8	DGND
D1	MC53	P13	AN_IN7	W3	DR_A6	L9	DGND
E1	MC54	P14	TP_YP	V1	DR_A7	L10	DGND
E2	MC55	N14	TP_XM	W2	DR_A8	L11	DGND
E3	MC56	A14	VBUS	U2	DR_A9	L12	DGND
L3	SN_PXCLK	A15	DM	V4	DR_A10	M4	DGND
M3	SN_VD	B15	DP	V2	DR_A11	M9	DGND
M2	SN_HD	C14	USB_RREF	W1	DR_A12	M10	DGND
M1	SN_D0	P7	PWR_SW	U5	DR_A13/BA2	M11	DGND
N1	SN_D1	P6	PWR_EN	U6	DR_BA0	T4	DGND
N2	SN_D2	L1	XTAL_RTCI	V6	DR_BA1	T16	DGND
N3	SN_D3	L2	XTAL_RTCO	W6	DR_CAS#	M14	AVDD_ADC
P3	SN_D4	P8	TESTEN	U8	DR_RAS#	N11	AGND_ADC
P1	SN_D5	N19	TV_FSADJ	U7	DR_WE#	N18	AVDD_DAC
R1	SN_D6	M19	TV_CVBS	W7	DR_CS#	M18	AGND_DAC
R2	SN_D7	G19	TXCP	U12	DR_DM0	N17	AVDD_AUD
R3	SN_D8	G18	TXCN	U15	DR_DM1	T18	AGND_AUD
T3	SN_D9	H18	TX0P	W12	DR_DQS0	W19	AVDD_AX
T2	SN_D10	H19	TX0N	V16	DR_DQS1	U18	AGND_AX
T1	SN_D11	J19	TX1P	W13	DR_DQS0#	B16	AVDD_HSRT
U1	SN_MCLK	J18	TX1N	W16	DR_DQS1#	C15	AGND_HSRT
H1	SP_CLK	K18	TX2P	W8	DR_CLK	C16	AVDD_USB
J1	MES0	K19	TX2N	V8	DR_CLK#	B14	AGND_USB
J2	MES1	F19	HDMI_REXT	V7	DR_CKE	K1	VDD_RTC
L6	FLCTR	M17	CEC	F9	VCC1V2	N6	VDD_VBAT
F3	PWM0	L18	DDCSDA	F10	VCC1V2	A19	VCC_PLL
F2	PWM1	L17	DDCSCL	G9	VCC1V2	A18	GND_PLL
F1	PWM2	L19	HOTPLUG	G10	VCC1V2	V17	VCC_DLL
G1	PWM3	P17	MIC_RINP	J6	VCC1V2	W17	GND_DLL
G2	PWM4	P18	MIC_RINN	J7	VCC1V2	T8	VDD_DDR
G3	PWM5	P19	MIC_RI	J13	VCC1V2	T9	VDD_DDR
H3	PWM6	R19	MIC_RO	J14	VCC1V2	T10	VDD_DDR
H2	PWM7	R17	MIC_BIAS	K6	VCC1V2	T11	VDD_DDR
N8	I2CSDA	R18	AUD_VMIDX	K7	VCC1V2	T12	VDD_DDR
N7	I2CSCL	T19	AUD_RADJ	K13	VCC1V2	U17	VDD_DDR
G13	SBCS0	U19	HPR	K14	VCC1V2	V9	VDD_DDR

G14	SBCK0	V19	HPL	N9	VCC1V2	W9	VDD_VREF
F14	SBDAT0	W18	SPKR	N10	VCC1V2	L14	AVDD_TP
J3	SBCS1	V18	SPKL	P9	VCC1V2	T17	AGND_TP
K3	SBCK1	A17	XTAL_SYSI	P10	VCC1V2	G17	AVDD_HDMI
K2	SBDAT1	A16	XTAL_SYSO	D8	VDD3V3	H17	AVDD_HDMI
L7	SBCS2	B11	RESET#	D9	VDD3V3	J17	AGND_HDMI
--	----	--	----	--	----	K17	AGND_HDMI

Pin Descriptions

I = input port with Schmitt trigger

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking and Schmitt trigger

OD = open drain output with normal sinking

I/OD = bi-directional port, open drain output with normal sinking and Schmitt trigger

p/u = internal pull-up

p/d = internal pull-down

AI = analog input port

AO = analog output port

AI/O = analog bi-directional port

H = output high

L = output low

The Reset column below means the pin's default state after power on reset.

NT96630 Pin Descriptions

System Interface

Pin No.	Name	Type	Reset	Descriptions
A17	XTAL_SYSI	AI	AI	System / USB Crystal Input. Connect to 12MHz crystal.
B17	XTAL_SYSO	O	O	System / USB Crystal or Output. Connect to 12MHz crystal.
C11	RESET#	I	I	System Reset
T3	TESTEN	I	I	Testing Mode Enable. Keep low for normal operation.
D12	IDIO / G_GPIO[0]	I/O	I p/d	ICE Data
B12	GOICE / G_GPIO[1]	I/O	I p/d	ICE Going
C12	IMS / G_GPIO[2]	I/O	I p/d	ICE Mode
D11	ICK / G_GPIO[3]	I/O	I p/d	ICE Clock
A18	XTAL_ASCI	AI	AI	Audio Crystal Input. It is option for external audio clock source.
A19	XTAL_ASCO	O	O	Audio Crystal Output. It is option for external audio clock source.

Sensor Interface

Pin No.	Name	Type	Reset	Descriptions

T2	SN_PXCLK	I	I p/d	Pixel clock input
T1	SN_VD	I/O	I p/d	Sensor Vertical Sync
U1	SN_HD	I/O	I p/d	Sensor Horizontal Sync
U2	SN_D0 / S_GPIO[0]	I/O	I p/d	Sensor Data Input
U3	SN_D1 / S_GPIO[1]	I/O	I p/d	Sensor Data Input
U4	SN_D2 / S_GPIO[2]	I/O	I p/d	Sensor Data Input
V1	SN_D3 / S_GPIO[3]	I/O	I p/d	Sensor Data Input
V2	SN_D4	I	I p/d	Sensor Data Input
V3	SN_D5	I	I p/d	Sensor Data Input
W1	SN_D6	I	I p/d	Sensor Data Input
W2	SN_D7	I	I p/d	Sensor Data Input
Y1	SN_D8	I	I p/d	Sensor Data Input
Y2	SN_D9	I	I p/d	Sensor Data Input
AA1	SN_D10	I	I p/d	Sensor Data Input
AA2	SN_D11	I	I p/d	Sensor Data Input
AB1	SN_MCLK / S_GPIO[4]	I/O	I p/d	Master Clock Output for Sensor
M1	SP_CLK / S_GPIO[5]	I/O	I p/d	Clock Output for Micro-stepping Motor Control
M2	MES0 / S_GPIO[6]	I/O	I p/d	Mechanical Shutter Control 0
M3	MES1 / S_GPIO[7]	I/O	I p/d	Mechanical Shutter Control 1
M4	FLCTR / S_GPIO[8]	I/O	I p/d	Flash Light Control

Sensor interface pinmux table

	SENSOR		CCIR IN (16 bits)		CCIR IN (8 bits)	
SN_PXCLK	I	PXCLK	I	PXCLK	I	PXCLK
SN_VD	IO	VD	IO	VD	IO	VD
SN_HD	IO	HD	IO	HD	IO	HD
SN_D0	I	DATA0	I	C4		
SN_D1	I	DATA1	I	C5		
SN_D2	I	DATA2	I	C6		
SN_D3	I	DATA3	I	C7		
SN_D4	I	DATA4	I	Y0	I	Y/C0
SN_D5	I	DATA5	I	Y1	I	Y/C1
SN_D6	I	DATA6	I	Y2	I	Y/C2
SN_D7	I	DATA7	I	Y3	I	Y/C3

SN_D8	I	DATA8	I	Y4	I	Y/C4
SN_D9	I	DATA9	I	Y5	I	Y/C5
SN_D10	I	DATA10	I	Y6	I	Y/C6
SN_D11	I	DATA11	I	Y7	I	Y/C7
SN_MCLK	O	MCLK	O	MCLK	O	MCLK

Serial Interface

Pin No.	Name	Type	Reset	Descriptions
R9	I2CSDA / P_GPIO[0]	I/O	I p/u	I2C Serial Data. I2CSDA is 5V tolerance input.
R8	I2CSCL / P_GPIO[1]	I/O	I p/u	I2C Serial Clock. I2CSCL is 5V tolerance input.
R21	ASCLK / P_GPIO[2]	I/O	I p/u	AC'97 Serial Data Clock / I2S Bit Clock
T19	ASYNC / P_GPIO[3]	I/O	I p/u	AC'97 48kHz Frame Sync / I2S Word Select
R19	ASDO / P_GPIO[4]	I/O	I p/u	AC'97 Serial Data Output / I2S Serial Data Output
R20	ASDI / P_GPIO[5]	I/O	I p/u	AC'97 Serial Data Input / I2S Serial Data Input
R22	ASCCLK / P_GPIO[6]	I/O	I p/u	AC'97 System Clock / I2S System Clock
N19	SBCS0 / P_GPIO[7]	I/O	I p/u	Serial Interface Chip Select 0
N20	SBCK0 / P_GPIO[8]	I/O	I p/u	Serial Interface Clock 0
N21	SBDAT0 / P_GPIO[9]	I/O	I p/u	Serial Interface Data 0
N1	SBCS1 / P_GPIO[10]	I/O	I p/u	Serial Interface Chip Select 1
N2	SBCK1 / P_GPIO[11]	I/O	I p/u	Serial Interface Clock 1
N3	SBDAT1 / P_GPIO[12]	I/O	I p/u	Serial Interface Data 1
N4	SBCS2 / P_GPIO[13]	I/O	I p/d	Serial Interface Chip Select 2
P1	SBCS3 / P_GPIO[14]	I/O	I p/d	Serial Interface Chip Select 3
P2	SBCK23 / P_GPIO[15]	I/O	I p/d	Serial Interface Clock 2 & 3
P3	SBDAT23 / P_GPIO[16]	I/O	I p/d	Serial Interface Data 2 & 3
N8	SBCS4 / P_GPIO[17]	I/O	I p/d	Serial Interface Chip Select 4
N9	SBCS5 / P_GPIO[18]*	I/O	I p/d	Serial Interface Chip Select 5

P8	SBCK45 / P_GPIO[19]	I/O	I p/d	Serial Interface Clock 4 & 5
P9	SBDAT45 / P_GPIO[20]	I/O	I p/d	Serial Interface Data 4 & 5
D14	UART_TX / P_GPIO[21]*	I/O	I p/u	UART Transmitted Data
D13	UART_RX / P_GPIO[22]*	I/O	I p/u	UART Received Data
P22	UART2_TX / P_GPIO[23]	I/O	I p/u	UART2 Transmitted Data
P21	UART2_RX / P_GPIO[24]	I/O	I p/u	UART2 Received Data
P20	USRT2_RTS / P_GPIO[25]*	I/O	I p/u	UART2 Request To Send
P19	UART2_CTS / P_GPIO[26]*	I/O	I p/u	UART2 Clear To Send
P15	UART2_DTR / P_GPIO[27]*	I/O	I p/u	UART2 Data Terminal Ready
N14	UART2_DSR / P_GPIO[28]*	I/O	I p/u	UART2 Data Set Ready
N15	UART2_DCD / P_GPIO[29]*	I/O	I p/u	UART2 Carrier Detect
K14	UART2_RI / P_GPIO[30]*	I/O	I p/u	UART2 Ring Indicator
C13	SPI_CS / P_GPIO[31]	I/O	I p/u	Serial Peripheral Interface Chip Select
B13	SPI_CLK / P_GPIO[32]	I/O	I p/u	Serial Peripheral Interface Clock
A13	SPI_DO / P_GPIO[33]	I/O	I p/u	Serial Peripheral Interface Data Output
A12	SPI_DI / P_GPIO[34]	I/O	I p/u	Serial Peripheral Interface Data Input
K15	REMOTE_RX / P_GPIO[35]*	I/O	I p/u	Infrared Remote-control Received Data

*P_GPIO18, 21, 22, 25, 26, 27, 28, 29, 30, 35 can trigger interrupt.

LCD Interface

Pin No.	Name	Type	Reset	Descriptions
H22	LCD0 / L_GPIO[0]	I/O	I p/d	LCD Signal Bus
H21	LCD1 / L_GPIO[1]	I/O	I p/d	LCD Signal Bus
H20	LCD2 / L_GPIO[2]	I/O	I p/d	LCD Signal Bus
H19	LCD3 / L_GPIO[3]	I/O	I p/d	LCD Signal Bus
G19	LCD4 /	I/O	I p/d	LCD Signal Bus

	L_GPIO[4]			
G20	LCD5 / L_GPIO[5]	I/O	I p/d	LCD Signal Bus
G21	LCD6 / L_GPIO[6]	I/O	I p/d	LCD Signal Bus
F22	LCD7 / L_GPIO[7]	I/O	I p/d	LCD Signal Bus
F21	LCD8 / L_GPIO[8]	I/O	I p/d	LCD Signal Bus
F20	LCD9 / L_GPIO[9]	I/O	I p/d	LCD Signal Bus
F19	LCD10 / L_GPIO[10]	I/O	I p/d	LCD Signal Bus
E19	LCD11 / L_GPIO[11]	I/O	I p/d	LCD Signal Bus
E20	LCD12 / L_GPIO[12]*	I/O	I p/d	LCD Signal Bus
E21	LCD13 / L_GPIO[13]*	I/O	I p/d	LCD Signal Bus
E22	LCD14 / L_GPIO[14]	I/O	I p/d	LCD Signal Bus
D22	LCD15 / L_GPIO[15]	I/O	I p/d	LCD Signal Bus
D21	LCD16 / L_GPIO[16]	I/O	I p/d	LCD Signal Bus
D20	LCD17 / L_GPIO[17]	I/O	I p/d	LCD Signal Bus
D19	LCD18 / L_GPIO[18]	I/O	I p/d	LCD Signal Bus
C19	LCD19 / L_GPIO[19]	I/O	I p/d	LCD Signal Bus
C20	LCD20 / L_GPIO[20]*	I/O	I p/d	LCD Signal Bus
C21	LCD21 / L_GPIO[21]*	I/O	I p/d	LCD Signal Bus
C22	LCD22 / L_GPIO[22]*	I/O	I p/d	LCD Signal Bus
B22	LCD23 / L_GPIO[23]*	I/O	I p/d	LCD Signal Bus
B21	LCD24 / L_GPIO[24]*	I/O	I p/d	LCD Signal Bus
B20	LCD25 / L_GPIO[25]	I/O	I p/d	LCD Signal Bus
B19	LCD26 / L_GPIO[26]	I/O	I p/d	LCD Signal Bus
A22	LCD27 / L_GPIO[27]	I/O	I p/d	LCD Signal Bus
A21	LCD28 /	I/O	I p/d	LCD Signal Bus

	L_GPIO[28]*			

*L_GPIO12, 13, 20, 21, 22, 23, 24, 28 can trigger interrupt.

LCD pinmux table

	CCIR-656 (8 bits)	CCIR-656 (16 bits)	CCIR-601 (8 bits)	CCIR-601 (16 bits)	Serial RGB666	Serial RGB888	Parallel LCD	HDMI	YCbCr422
LCD0	O YC0	O Y0	O YC0	O YC0	O AD0	O YC0	O C0_0	O C0_0	O YC0
LCD1	O YC1	O Y1	O YC1	O YC1	O AD1	O YC1	O C0_1	O C0_1	O YC1
LCD2	O YC2	O Y2	O YC2	O YC2	O AD2	O YC2	O C0_2	O C0_2	O YC2
LCD3	O YC3	O Y3	O YC3	O YC3	O AD3	O YC3	O C0_3	O C0_3	O YC3
LCD4	O YC4	O Y4	O YC4	O YC4	O AD4	O YC4	O C0_4	O C0_4	O YC4
LCD5	O YC5	O Y5	O YC5	O YC5	O AD5	O YC5	O C0_5	O C0_5	O YC5
LCD6	O YC6	O Y6	O YC6	O YC6		O YC6	O C0_6	O C0_6	O YC6
LCD7	O YC7	O Y7	O YC7	O YC7		O YC7	O C0_7	O C0_7	O YC7
LCD8	O VDCK	O VDCK	O VDCK	O VDCK	O ADCLK	O DCLK	O DCLK	O DCLK	O VDCK
LCD9			O VS601	O VS601	O AVS	O VS	O VS	O VS	O VS601
LCD10			O HS601	O HS601	O AHS	O HS	O HS	O HS	O HS601
LCD11	O DE	O DE	O FIELD	O FIELD	O DE	O DE	O DE	O DE	O DE
LCD12		O C0		O C0			O C1_0	O C1_0	
LCD13		O C1		O C1			O C1_1	O C1_1	
LCD14		O C2		O C2			O C1_2	O C1_2	
LCD15		O C3		O C3			O C1_3	O C1_3	
LCD16		O C4		O C4			O C1_4	O C1_4	
LCD17		O C5		O C5			O C1_5	O C1_5	
LCD18		O C6		O C6			O C1_6	O C1_6	
LCD19		O C7		O C7			O C1_7	O C1_7	
LCD20			O HVLD	O HVLD			O C2_0	O C2_0	
LCD21			O VVLD	O VVLD			O C2_1	O C2_1	
LCD22							O C2_2	O C2_2	
LCD23							O C2_3	O C2_3	
LCD24							O C2_4	O C2_4	

LCD25													O	C2_5	O	C2_5			
LCD26													O	C2_6	O	C2_6			
LCD27													O	C2_7	O	C2_7			
LCD28															I	HDMI_INT			

TV-out Interface

Pin No.	Name	Type	Reset	Descriptions
T22	TV_FSADJ	AI	-	Full Screen Adjust Pin TV DAC Full-scale adjust control pin. A resistor connected between this pin and GND controls the full-scale output current on the TV_CVBS output.
T21	TV_CVBS	AO	-	Composite Video Output

HDMI Transmitter Interface

Pin No.	Name	Type	Reset	Descriptions
J22	TXCP	AO	-	TMDS Low Voltage Differential Signal Ouput Clock
J21	TXCN	AO	-	TMDS Low Voltage Differential Signal Ouput Clock
K22	TX0P	AO	-	TMDS Low Voltage Differential Signal Ouput Data
K21	TX0N	AO	-	TMDS Low Voltage Differential Signal Ouput Data
L22	TX1P	AO	-	TMDS Low Voltage Differential Signal Ouput Data
L21	TX1N	AO	-	TMDS Low Voltage Differential Signal Ouput Data
M22	TX2P	AO	-	TMDS Low Voltage Differential Signal Ouput Data
M21	TX2N	AO	-	TMDS Low Voltage Differential Signal Ouput Data
J19	HDMI_REXT	AI	-	Voltage Swing Adjust. A resistor should tie this pin to ground. This resistor sets the amplitude of the voltage swing.
N22	CEC / G_GPIO[8]*	I/O	I p/u	Consumer Electronics Control. CEC is 5V tolerance input.
M19	DDCSDA / G_GPIO[9]	I/O	I p/u	Display Data Channel SDA. DDCSDA is 5V tolerance input.
M20	DDCSCL / G_GPIO[10]	I/O	I p/u	Display Data Channel SCL. DDCSCL is 5V tolerance input.
L19	HOTPLUG / G_GPIO[11]	I/O	I p/d	Hot Plug Detect. HOTPLUG is 5V tolerance input.

*G_GPIO8 can trigger interrupt.

ADC & Touch Panel Interface

Pin No.	Name	Type	Reset	Descriptions
W17	A D_IN0	AI	-	General ADC Input
Y17	A D_IN1	AI	-	General ADC Input
AA17	A D_IN2	AI	-	General ADC Input
AB17	A D_IN3	AI	-	General ADC Input
AB18	A D_IN4	AI	-	General ADC Input

AA18	A D_IN5	AI	-	General ADC Input
Y18	A D_IN6	AI	-	General ADC Input
W18	A D_IN7	AI	-	General ADC Input
W19	TP_YP	AI	-	Touch Panel Control Interface
Y19	TP_XM	AI	-	Touch Panel Control Interface

ADC pinmux table

	ADC		GYRO		TP	
AD_IN0	I	AD_IN0				
AD_IN1	I	AD_IN1				
AD_IN2	I	AD_IN2				
AD_IN3	I	AD_IN3				
AD_IN4	I	AD_IN4	I	GYRO_IN1		
AD_IN5	I	AD_IN5	I	GYRO_IN2		
AD_IN6	I	AD_IN6			I	TPXP
AD_IN7	I	AD_IN7			I	TPYM
TP_YP					I	TPYP
TP_XM					I	TPXM

Memory Card Interface

Pin No.	Name	Type	Reset	Descriptions
B11	MC0 / C_GPIO[0]	I/O	I p/u	Memory Card Interface
A11	MC1 / C_GPIO[1]	I/O	I p/u	Memory Card Interface
A10	MC2 / C_GPIO[2]	I/O	I p/u	Memory Card Interface
B10	MC3 / C_GPIO[3]	I/O	I p/u	Memory Card Interface
C10	MC4 / C_GPIO[4]	I/O	I p/u	Memory Card Interface
D10	MC5 / C_GPIO[5]	I/O	I p/u	Memory Card Interface
D9	MC6 / C_GPIO[6]	I/O	I p/u	Memory Card Interface
C9	MC7 / C_GPIO[7]	I/O	I p/u	Memory Card Interface
B9	MC8 / C_GPIO[8]	I/O	I p/u	Memory Card Interface
A9	MC9 / C_GPIO[9]	I/O	I p/u	Memory Card Interface
A8	MC10 / C_GPIO[10]	I/O	I p/u	Memory Card Interface

B8	MC11 / C_GPIO[11]	I/O	I p/u	Memory Card Interface
C8	MC12 / C_GPIO[12]	I/O	I p/u	Memory Card Interface
D8	MC13 / C_GPIO[13]	I/O	I p/d	Memory Card Interface
D7	MC14 / C_GPIO[14]	I/O	I p/d	Memory Card Interface
C7	MC15 / C_GPIO[15]	I/O	I p/d	Memory Card Interface
B7	MC16 / C_GPIO[16]	I/O	I p/u	Memory Card Interface
A7	MC17 / C_GPIO[17]	I/O	I p/d	Memory Card Interface
A6	MC18 / C_GPIO[18]*	I/O	I p/u	Memory Card Interface
B6	MC19 / C_GPIO[19]	I/O	I p/u	Memory Card Interface
C6	MC20 / C_GPIO[20]*	I/O	I p/u	Memory Card Interface
D6	MC21 / C_GPIO[21]	I/O	I p/d	Memory Card Interface
D5	MC22 / C_GPIO[22]	I/O	I p/d	Memory Card Interface
C5	MC23 / C_GPIO[23]	I/O	I p/d	Memory Card Interface
B5	MC24 / C_GPIO[24]	I/O	I p/d	Memory Card Interface
A5	MC25 / C_GPIO[25]	I/O	I p/d	Memory Card Interface
A4	MC26 / C_GPIO[26]	I/O	I p/d	Memory Card Interface
B4	MC27 / C_GPIO[27]	I/O	I p/d	Memory Card Interface
A3	MC28 / C_GPIO[28]	I/O	I p/d	Memory Card Interface
A2	MC29 / C_GPIO[29]	I/O	I p/d	Memory Card Interface
A1	MC30 / C_GPIO[30]	I/O	I p/d	Memory Card Interface
B3	MC31 / C_GPIO[31]	I/O	I p/d	Memory Card Interface
B2	MC32 / C_GPIO[32]	I/O	I p/u	Memory Card Interface
B1	MC33 / C_GPIO[33]	I/O	I p/u	Memory Card Interface
C1	MC34 / C_GPIO[34]	I/O	I p/u	Memory Card Interface

C2	MC35 / C_GPIO[35]	I/O	I p/u	Memory Card Interface
C3	MC36 / C_GPIO[36]*	I/O	I p/d	Memory Card Interface
C4	MC37 / C_GPIO[37]*	I/O	I p/d	Memory Card Interface
D4	MC38 / C_GPIO[38]*	I/O	I p/d	Memory Card Interface
D3	MC39 / C_GPIO[39]*	I/O	I p/d	Memory Card Interface
D2	MC40 / C_GPIO[40]	I/O	I p/d	Memory Card Interface
D1	MC41 / C_GPIO[41]	I/O	I p/u	Memory Card Interface
E1	MC42 / C_GPIO[42]	I/O	I p/u	Memory Card Interface
E2	MC43 / C_GPIO[43]	I/O	I p/d	Memory Card Interface
E3	MC44 / C_GPIO[44]	I/O	I p/u	Memory Card Interface
E4	MC45 / C_GPIO[45]	I/O	I p/u	Memory Card Interface
F4	MC46 / C_GPIO[46]	I/O	I p/u	Memory Card Interface
F3	MC47 / C_GPIO[47]	I/O	I p/u	Memory Card Interface
F2	MC48 / C_GPIO[48]	I/O	I p/u	Memory Card Interface
F1	MC49 / C_GPIO[49]	I/O	I p/u	Memory Card Interface
G1	MC50 / C_GPIO[50]*	I/O	I p/u	Memory Card Interface
G2	MC51 / C_GPIO[51]*	I/O	I p/u	Memory Card Interface
G3	MC52 / C_GPIO[52]	I/O	I p/u	Memory Card Interface
G4	MC53 / C_GPIO[53]	I/O	I p/u	Memory Card Interface
H4	MC54 / C_GPIO[54]	I/O	I p/u	Memory Card Interface
H3	MC55 / C_GPIO[55]	I/O	I p/u	Memory Card Interface
H2	MC56 / C_GPIO[56]	I/O	I p/u	Memory Card Interface

C_GPIO18, 20, 36, 37, 38, 39, 50, 51 can trigger interrupt.

Memory card interface pinmux table

	SM/NAND		xD Socket		SD/MMC		MS/MS-PRO		CF		ATA		Parallel ROM / Flash		Serial Flash	
MC0	IO	SM_D0				SDIO_D0 *(1)			IO	CF_D0	IO	DD0	IO	P_D0	I	S_DI
MC1	IO	SM_D1				SDIO_D1 *(1)			IO	CF_D1	IO	DD1	IO	P_D1	O	S_DO
MC2	IO	SM_D2				SDIO_D2 *(1)			IO	CF_D2	IO	DD2	IO	P_D2	IO	S_SCK
MC3	IO	SM_D3				SDIO_D3 *(1)			IO	CF_D3	IO	DD3	IO	P_D3		
MC4	IO	SM_D4	IO	SM_D4		SDIO_CMD *(1)			IO	CF_D4	IO	DD4	IO	P_D4		
MC5	IO	SM_D5							IO	CF_D5	IO	DD5	IO	P_D5		
MC6	IO	SM_D6							IO	CF_D6	IO	DD6	IO	P_D6		
MC7	IO	SM_D7	IO	SM_D7					IO	CF_D7	IO	DD7	IO	P_D7		
MC8	O	NAND_/CS0														
MC9	O	NAND_/CS1											O	P_/CS0	IO	S_CS
MC10	O	xD_/CS	IO	SM_D5	O	SDIO_CLK	O	MS_BS								
MC11	O	SM_/WE	O	SM_/WE					O	CF_/WE	O	DATA_OE	O	P_/WE		
MC12	O	SM_/RE	O	SM_/RE					O	CF_/OE	O	ATA_SEL	O	P_/OE		
MC13	O	SM_CLE	O	SM_CLE					O	CF_/IOWR	O	/DIOW	IO	P_A0(D15)		
MC14	O	SM_ALE	O	SM_ALE					O	CF_/IORD	O	/DIOR	O	P_A1		
MC15	O	NAND_/WP														
MC16	I	SM_RDY	I	SM_RDY												
MC17	O	xD_/WP	O	xD_/WP												
MC18									I	CF_RDY	I	INTRQ				
MC19													O	P_/CS1		
MC20									I	CF_/WAIT	I	IDRDY	I	IOWAIT		
MC21									IO	CF_D8	IO	DD8	IO	P_D8		
MC22									IO	CF_D9	IO	DD9	IO	P_D9		
MC23									IO	CF_D10	IO	DD10	IO	P_D10		
MC24									IO	CF_D11	IO	DD11	IO	P_D11		
MC25									IO	CF_D12	IO	DD12	IO	P_D12		
MC26									IO	CF_D13	IO	DD13	IO	P_D13		
MC27									IO	CF_D14	IO	DD14	IO	P_D14		
MC28									IO	CF_D15	IO	DD15	O	P_A17		
MC29									O	CF_A0	O	DA0	O	P_A18		
MC30									O	CF_A1	O	DA1	O	P_A19		
MC31									O	CF_A2	O	DA2	O	P_A20		
MC32			IO	SM_D0	IO	SDIO_D0 *(0)			O	CF_A3			O	P_A16		
MC33			IO	SM_D1	IO	SDIO_D1 *(0)			O	CF_A4			O	P_A2		
MC34			IO	SM_D2	IO	SDIO_D2 *(0)			O	CF_A5			O	P_A3		

MC35			IO	SM_D3	IO	SDIO_D3 *(0)			O	CF_A6			O	P_A4				
MC36					IO	MMC_D4	IO	MS_D4	O	CF_A7			O	P_A5				
MC37					IO	MMC_D5	IO	MS_D5	O	CF_A8			O	P_A6				
MC38					IO	MMC_D6	IO	MS_D6	O	CF_A9			O	P_A7				
MC39					IO	MMC_D7	IO	MS_D7	O	CF_A10			O	P_A8				
MC40									O	CF_/REG	O	/DMACK	O	P_A21				
MC41									O	CF_RESET	O	/RESET						
MC42									I	CF_/IOIS16	I	/IOSC16						
MC43									I	CF_/INPACK	I	DMARQ						
MC44									O	CF_/CE	O	/CS0						
MC45									O	CF_/CE2	O	/CS1						
MC46			IO	SM_D6	IO	SDIO_CMD *(0)	O	MS_CLK										
MC47					O	SDIO2_CLK												
MC48					IO	SDIO2_CMD												
MC49					IO	SDIO2_D0							O	P_A9				
MC50					IO	SDIO2_D1							O	P_A10				
MC51					IO	SDIO2_D2							O	P_A11				
MC52					IO	SDIO2_D3							O	P_A12				
MC53							IO	MS_D3					O	P_A13				
MC54							IO	MS_D2					O	P_A14				
MC55							IO	MS_D1					O	P_A15				
MC56			O	xD_/CS			IO	MS_D0										

*(0) SD pin mode 0 pin out position.

*(1) SD pin mode 1 pin out position.

DDR1/2 SDRAM Interface

Pin No.	Name	Type	Reset	Descriptions
AA10	DR_D0	I/O	-	DDR1/2 data input/output.
AB10	DR_D1	I/O	-	
AA9	DR_D2	I/O	-	
Y9	DR_D3	I/O	-	
W9	DR_D4	I/O	-	
AB9	DR_D5	I/O	-	
Y10	DR_D6	I/O	-	
AA11	DR_D7	I/O	-	
Y14	DR_D8	I/O	-	
Y13	DR_D9	I/O	-	
AB13	DR_D10	I/O	-	
Y12	DR_D11	I/O	-	

AA12	DR_D12	I/O	-	
AA13	DR_D13	I/O	-	
AA14	DR_D14	I/O	-	
Y15	DR_D15	I/O	-	
AB5	DR_A0	I/O	-	DDR1/2 address output.
Y5	DR_A1	O	-	
AA5	DR_A2	O	-	
W4	DR_A3	O	-	
AB4	DR_A4	O	-	
Y4	DR_A5	O	-	
AA4	DR_A6	O	-	
W3	DR_A7	O	-	
AB3	DR_A8	O	-	
Y3	DR_A9	O	-	
W5	DR_A10	O	-	
AA3	DR_A11	O	-	
AB2	DR_A12	O	-	
W7	DR_A13/BA2	O	-	DDR1/2 bank address or address output.
W6	DR_BA0	O	-	DDR1/2 bank address outputs.
Y6	DR_BA1	O	-	
AA6	DR_CAS#	O	-	DDR1/2 command output.
AA7	DR_RAS#	O	-	
Y7	DR_WE#	O	-	
AB6	DR_CS#	O	-	DDR1/2 chip select.
Y11	DR_DM0	O	-	DDR1/2 data mask.
AB14	DR_DM1	O	-	
AB11	DR_DQS0	I/O	-	DDR1/2 data strobe for lower byte.
AA15	DR_DQS1	I/O	-	DDR1/2 data strobe for upper byte.
AB12	DR_DQS0#	I/O	-	DDR2 data strobe for lower byte when differential data strobe mode is enable.
AB15	DR_DQS1#	I/O	-	DDR2 data strobe for upper byte when differential data strobe mode is enable.
AB8	DR_CLK	O	-	DDR1/2 differential clock output.
AB7	DR_CLK#	O	-	
AA8	DR_CKE	O	-	DDR1/2 clock enable.

USB Interface

Pin No.	Name	Type	Reset	Descriptions
C15	VBUS	AI	-	USB VBUS input. VBUS is 5V tolerance input.
A16	DM	AI/O	-	USB differential data pairs minus side.
B16	DP	AI/O	-	USB differential data pairs plus side.
D15	USB_RREF	AI	-	USB reference resistor. A 12kOhm/1% resistor should be tied to this pin and ground.
B14	USB_ID / P_GPIO[36]*	I	Ip/u	USB ID pin for host/device function selecting. Low for host and high for device.
C14	USB_DRVBUS/ P_GPIO[37]*	I/O	-	USB driver VBUS. For VBUS 5V power turn on/off control.

P_GPIO36, 37 can trigger interrupt.

PWM

Pin No.	Name	Type	Reset	Descriptions
K1	PWM0 / S_GPIO[9] / BST[0]	I/O		PWM output pin and boot strap setting. BST[3..0] configure the boot source. Boot source selection: 0000: NAND with Hamming ECC - Support 512bytes/2Kbytes/4Kbytes page 0001: xD with Hamming ECC (with XD SOCKET) - Support Normal type/ M type/ H type xD 0010: NAND without ECC - Support 512bytes/2Kbytes/4Kbytes page 0011: USB (Auto speed detection) 0100: SDIO (SD_PINMODE = 0) - Support SD/SDHC 0101: CF True IDE/ATA mode - Support CF at True IDE mode, ATA 48 bits addressing and host protected area 0110: MS - Support MS-Pro/MS-HG 0111: NOR Flash 1000: NAND with RS ECC - Support 512bytes/2Kbytes/4Kbytes page 1001: SDIO2 - Support SD/SDHC 1010: xD without Hamming ECC (with XD SOCKET) - Support Normal type/ M type/ H type xD 1011: Serial Flash (SPI) - Support 3 bytes address 1100: USB (Force full speed) 1101: SDIO (SD_PINMODE = 1) - Support SD/SDHC 1110: xD with Hamming ECC (without XD_SOCKET) - Support Normal type/ M type/ H type xD 1111: xD without Hamming ECC (without XD_SOCKET) - Support Normal type/ M type/ H type xD
K2	PWM1 / S_GPIO[10] / BST[1]	I/O		
K3	PWM2 / S_GPIO[11] / BST[2]	I/O		
K4	PWM3 / S_GPIO[12] / BST[3]	I/O		
L1	PWM4 / S_GPIO[13]	I/O		PWM output pin.
L2	PWM5 / S_GPIO[14]	I/O		PWM output pin.
L3	PWM6 / S_GPIO[15]	I/O		PWM output pin.
L4	PWM7 / S_GPIO[16] / BST[8]	I/O		PWM output pin and boot strap setting. BST[8] is for debug only. Please keep this pin low at reset signal rising edge.

DGPIO

Pin No.	Name	Type	Reset	Descriptions
H1	DGPIO0*	I/O	Ip/d	General purpose input/output pin.
J1	DGPIO1*	I/O	Ip/d	General purpose input/output pin.
J2	DGPIO2*	I/O	Ip/d	General purpose input/output pin.
J3	DGPIO3*	I/O	Ip/d	General purpose input/output pin.
J4	DGPIO4*	I/O	Ip/d	General purpose input/output pin.
K8	DGPIO5*	I/O	Ip/d	General purpose input/output pin.
K9	DGPIO6*	I/O	Ip/d	General purpose input/output pin.

DGPIO0~9 can trigger interrupt.

GPIO pinmux table

	DGPIO		CCIR IN (16 bits)		CCIR IN (8 bits)		Dedicat PIN	
DGPIO0	IO	DGPIO0	I	Field	I	Field		
DGPIO1	IO	DGPIO1	I	C0				
DGPIO2	IO	DGPIO2	I	C1				
DGPIO3	IO	DGPIO3	I	C2				
DGPIO4	IO	DGPIO4	I	C3				
DGPIO5	IO	DGPIO5					I	PICNT
DGPIO6	IO	DGPIO6					I	Card Detect

RTC & Power Button Control (PWBC)

Pin No.	Name	Type	Reset	Descriptions
T4	PWR_SW	I	I	Power on/off signal input.
R4	PWR_EN	O	O	Power switch or power IC enable signal output.
R2	XTAL_RTCI	AI	-	Real time clock input. Connect to 32768Hz crystal.
R1	XTAL_RTCO	AO	-	Real time clock output. Connect to 32768Hz crystal.

Embedded Audio Codec

Pin No.	Name	Type	Reset	Descriptions
V20	MIC_RINP	AI	-	Right channel microphone differential input positive side.
V19	MIC_RINN	AI	-	Right channel microphone differential input negative side.
U19	MIC_LINP	AI	-	Left channel microphone differential input positive side.
U20	MIC_LINN	AI	-	Left channel microphone differential input negative side.
AA22	MIC_BIAS	AO	-	Microphone working bias output.
W21	MIC_RI	AI	-	Right channel DC canceling input path. Connect 1uF capacitor to MIC_RO.
V21	MIC_LI	AI	-	Left channel DC canceling input path. Connect 1uF

				capacitor to MIC_LO.
W22	MIC_RO	AO	-	Right channel DC canceling output path. Connect 1uF capacitor to MIC_RI.
V22	MIC_LO	AO	-	Left channel DC canceling output path. Connect 1uF capacitor to MIC_LI.
Y22	AUD_VMIDX	AO	-	Decoupling for audio codec reference voltage. Connect 4.7uF capacitor to ground.
AB22	AUD_RADJ	AI	-	Reference resistor for audio codec. Connector 12kohm resistor to ground.
Y21	HPR	AO	-	Right channel headphone output.
AA21	HPL	AO	-	Left channel headphone output.
W20	LINEOUT_R	AO	-	Right channel line-out output.
Y20	LINEOUT_L	AO	-	Left channel line-out output.
AA20	SPKR	AO	-	Speaker output positive side. Connect speaker to SPKL for BTL mode application.
AB20	SPKL	AO	-	Speaker output negative side. Connect speaker to SPKL for BTL mode application.

Power

Pin No.	Name	Descriptions
H10,H11,H12,H13,L8, L9,L14,L15,M8,M9, M14,M15,R10,R11,R12, R13	VCC1V2	1.2V core power.
H8,H9,H14,H15,J8, J9,J14,J15	VDD3V3	3.3V I/O power.
V4	VDD_SN	Sensor multi-level I/O power. (3.3V/2.5V/1.8V)
A20,G22	VDD_LCD	LCD multi-level I/O power. (3.3V/2.5V/1.8V)
J10,J11,J12,J13,K10, K11,K12,K13,L10,L11, L12,L13,M10,M11,M12, M13,N10,N11,N12,N13, P10,P11,P12,P13,W8, W16	DGND	Digital ground.
AA19	AVDD_ADC	3.3V general ADC power.
Y16	AGND_ADC	General ADC analog ground.
U22	AVDD_DAC	3.3V DAC power.
T20	AGND_DAC	DAC analog ground.
U21	AVDD_AUD	3.3V audio codec ground.
R15	AGND_AUD	Audio codec analog ground.
AB21	AVDD_AX	3.3V Audio output buffer power.
R14	AGND_AX	Audio output buffer analog ground.
D17	AVDD_HSRT	3.3V USB high speed receiver/transmitter power.
C16	AGND_HSRT	USB high speed receiver/transmitter analog ground.
C17	AVDD_USB	3.3V USB analog power.
D16	AGND_USB	USB analog ground.
A15	AVDD_VDT	3.3V USB voltage detection power.

B15	AGND_VDT	USB voltage detection analog ground.
R3	VDD_RTC	Real time clock power.
P4	VDD_VBAT	PWBC block power.
A14	VCC_PLL1	1.2V PLL1 power.
C18	VCC_PLL2	1.2V PLL2 power.
D18	GND_PLL	PLL ground.
AB16	VCC_DLL	1.2V DLL power
AA16	GND_DLL	DLL ground.
W10,W11,W12,W13,W14, W15	VDD_DDR	DDR I/O power. 2.5V for DDR1; 1.8V for DDR2
Y8	VDD_VREF	DDR I/O reference voltage. 1.25V for DDR1; 0.9V for DDR2
B18	AVDD_ASC	3.3V audio crystal pad power.
AB19	AVDD_TP	3.3V touch panel controller power
P14	AGND_TP	Touch panel controller ground.
J20,K19	AVDD_HDMI	1.2V HDMI transmitter analog power
K20,L20	AGND_HDMI	HDMI transmitter analog ground.

NT96632 Pin Descriptions

System Interface

Pin No.	Name	Type	Reset	Descriptions
A17	XTAL_SYSI	AI	AI	System / USB Crystal Input. Connect to 12MHz crystal.
A16	XTAL_SYSO	O	O	System / USB Crystal or Output. Connect to 12MHz crystal.
B11	RESET#	I	I	System Reset
P8	TESTEN	I	I	Testing Mode Enable. Keep low for normal operation.
A12	IDIO / G_GPIO[0]	I/O	I p/d	ICE Data
C12	GOICE / G_GPIO[1]	I/O	I p/d	ICE Going
B12	IMS / G_GPIO[2]	I/O	I p/d	ICE Mode
A11	ICK / G_GPIO[3]	I/O	I p/d	ICE Clock

Sensor Interface

Pin No.	Name	Type	Reset	Descriptions
L3	SN_PXCLK	I	I p/d	Pixel clock input
M3	SN_VD	I/O	I p/d	Sensor Vertical Sync
M2	SN_HD	I/O	I p/d	Sensor Horizontal Sync
M1	SN_D0 / S_GPIO[0]	I/O	I p/d	Sensor Data Input
N1	SN_D1 / S_GPIO[1]	I/O	I p/d	Sensor Data Input

N2	SN_D2 / S_GPIO[2]	I/O	I p/d	Sensor Data Input
N3	SN_D3 / S_GPIO[3]	I/O	I p/d	Sensor Data Input
P3	SN_D4	I	I p/d	Sensor Data Input
P1	SN_D5	I	I p/d	Sensor Data Input
R1	SN_D6	I	I p/d	Sensor Data Input
R2	SN_D7	I	I p/d	Sensor Data Input
R3	SN_D8	I	I p/d	Sensor Data Input
T3	SN_D9	I	I p/d	Sensor Data Input
T2	SN_D10	I	I p/d	Sensor Data Input
T1	SN_D11	I	I p/d	Sensor Data Input
U1	SN_MCLK / S_GPIO[4]	I/O	I p/d	Master Clock Output for Sensor
H1	SP_CLK / S_GPIO[5]	I/O	I p/d	Clock Output for Micro-stepping Motor Control
J1	MES0 / S_GPIO[6]	I/O	I p/d	Mechanical Shutter Control 0
J2	MES1 / S_GPIO[7]	I/O	I p/d	Mechanical Shutter Control 1
L6	FLCTR / S_GPIO[8]	I/O	I p/d	Flash Light Control

Sensor interface pinmux table

	SENSOR		CCIR IN (16 bits)		CCIR IN (8 bits)	
SN_PXCLK	I	PXCLK	I	PXCLK	I	PXCLK
SN_VD	IO	VD	IO	VD	IO	VD
SN_HD	IO	HD	IO	HD	IO	HD
SN_D0	I	DATA0	I	C4		
SN_D1	I	DATA1	I	C5		
SN_D2	I	DATA2	I	C6		
SN_D3	I	DATA3	I	C7		
SN_D4	I	DATA4	I	Y0	I	Y/C0
SN_D5	I	DATA5	I	Y1	I	Y/C1
SN_D6	I	DATA6	I	Y2	I	Y/C2
SN_D7	I	DATA7	I	Y3	I	Y/C3
SN_D8	I	DATA8	I	Y4	I	Y/C4
SN_D9	I	DATA9	I	Y5	I	Y/C5
SN_D10	I	DATA10	I	Y6	I	Y/C6
SN_D11	I	DATA11	I	Y7	I	Y/C7
SN_MCLK	O	MCLK	O	MCLK	O	MCLK

Serial Interface

Pin No.	Name	Type	Reset	Descriptions
N8	I2CSDA / P_GPIO[0]	I/O	I p/u	I2C Serial Data. I2CSDA is 5V tolerance input.
N7	I2CSCL / P_GPIO[1]	I/O	I p/u	I2C Serial Clock. I2CSCL is 5V tolerance input.
G13	SBCS0 / P_GPIO[7]	I/O	I p/u	Serial Interface Chip Select 0
G14	SBCK0 / P_GPIO[8]	I/O	I p/u	Serial Interface Clock 0
F14	SBDAT0 / P_GPIO[9]	I/O	I p/u	Serial Interface Data 0
J3	SBCS1 / P_GPIO[10]	I/O	I p/u	Serial Interface Chip Select 1
K3	SBCK1 / P_GPIO[11]	I/O	I p/u	Serial Interface Clock 1
K2	SBDAT1 / P_GPIO[12]	I/O	I p/u	Serial Interface Data 1
L7	SBCS2 / P_GPIO[13]	I/O	I p/d	Serial Interface Chip Select 2
M6	SBCS3 / P_GPIO[14]	I/O	I p/d	Serial Interface Chip Select 3
M7	SBCK23 / P_GPIO[15]	I/O	I p/d	Serial Interface Clock 2 & 3
M8	SBDAT23 / P_GPIO[16]	I/O	I p/d	Serial Interface Data 2 & 3
A13	UART_TX / P_GPIO[21]*	I/O	I p/u	UART Transmitted Data
B13	UART_RX / P_GPIO[22]*	I/O	I p/u	UART Received Data
H14	UART2_TX / P_GPIO[23]	I/O	I p/u	UART2 Transmitted Data
H13	UART2_RX / P_GPIO[24]	I/O	I p/u	UART2 Received Data
H12	USRT2_RTS / P_GPIO[25]*	I/O	I p/u	UART2 Request To Send
G12	UART2_CTS / P_GPIO[26]*	I/O	I p/u	UART2 Clear To Send
F13	SPI_CS / P_GPIO[31]	I/O	I p/u	Serial Peripheral Interface Chip Select
F12	SPI_CLK / P_GPIO[32]	I/O	I p/u	Serial Peripheral Interface Clock
G11	SPI_DO / P_GPIO[33]	I/O	I p/u	Serial Peripheral Interface Data Output
F11	SPI_DI / P_GPIO[34]	I/O	I p/u	Serial Peripheral Interface Data Input
C13	REMOTE_RX / P_GPIO[35]*	I/O	I p/u	Infrared Remote-control Received Data

*P_GPIO 21, 22, 25, 26, 35 can trigger interrupt.

LCD Interface

Pin No.	Name	Type	Reset	Descriptions
F18	LCD0 / L_GPIO[0]	I/O	I p/d	LCD Signal Bus
F17	LCD1 / L_GPIO[1]	I/O	I p/d	LCD Signal Bus
E17	LCD2 / L_GPIO[2]	I/O	I p/d	LCD Signal Bus
E18	LCD3 / L_GPIO[3]	I/O	I p/d	LCD Signal Bus
E19	LCD4 / L_GPIO[4]	I/O	I p/d	LCD Signal Bus
D19	LCD5 / L_GPIO[5]	I/O	I p/d	LCD Signal Bus
D18	LCD6 / L_GPIO[6]	I/O	I p/d	LCD Signal Bus
D17	LCD7 / L_GPIO[7]	I/O	I p/d	LCD Signal Bus
C17	LCD8 / L_GPIO[8]	I/O	I p/d	LCD Signal Bus
C18	LCD9 / L_GPIO[9]	I/O	I p/d	LCD Signal Bus
C19	LCD10 / L_GPIO[10]	I/O	I p/d	LCD Signal Bus
B19	LCD11 / L_GPIO[11]	I/O	I p/d	LCD Signal Bus

LCD pinmux table

	CCIR-656 (8 bits)		CCIR-601 (8 bits)		Serial RGB666		Serial RGB888		YCbCr422	
LCD0	O	YC0	O	YC0	O	AD0	O	YC0	O	YC0
LCD1	O	YC1	O	YC1	O	AD1	O	YC1	O	YC1
LCD2	O	YC2	O	YC2	O	AD2	O	YC2	O	YC2
LCD3	O	YC3	O	YC3	O	AD3	O	YC3	O	YC3
LCD4	O	YC4	O	YC4	O	AD4	O	YC4	O	YC4
LCD5	O	YC5	O	YC5	O	AD5	O	YC5	O	YC5
LCD6	O	YC6	O	YC6			O	YC6	O	YC6
LCD7	O	YC7	O	YC7			O	YC7	O	YC7

LCD8	O	VDCK	O	VDCK	O	ADCLK	O	DCLK	O	VDCK
LCD9			O	VS601	O	AVS	O	VS	O	VS601
LCD10			O	HS601	O	AHS	O	HS	O	HS601
LCD11	O	DE	O	FIELD	O	DE	O	DE	O	DE

TV-out Interface

Pin No.	Name	Type	Reset	Descriptions
N19	TV_FSADJ	AI	-	Full Screen Adjust Pin TV DAC Full-scale adjust control pin. A resistor connected between this pin and GND controls the full-scale output current on the TV_CVBS output.
M19	TV_CVBS	AO	-	Composite Video Output

HDMI Transmitter Interface

Pin No.	Name	Type	Reset	Descriptions
G19	TXCP	AO	-	TMDS Low Voltage Differential Signal Output Clock
G18	TXCN	AO	-	TMDS Low Voltage Differential Signal Output Clock
H18	TX0P	AO	-	TMDS Low Voltage Differential Signal Output Data
H19	TX0N	AO	-	TMDS Low Voltage Differential Signal Output Data
J19	TX1P	AO	-	TMDS Low Voltage Differential Signal Output Data
J18	TX1N	AO	-	TMDS Low Voltage Differential Signal Output Data
K18	TX2P	AO	-	TMDS Low Voltage Differential Signal Output Data
K19	TX2N	AO	-	TMDS Low Voltage Differential Signal Output Data
F19	HDMI_REXT	AI	-	Voltage Swing Adjust. A resistor should tie this pin to ground. This resistor sets the amplitude of the voltage swing.
M17	CEC / G_GPIO[8]*	I/O	I p/u	Consumer Electronics Control. CEC is 5V tolerance input.
L18	DDCSDA / G_GPIO[9]	I/O	I p/u	Display Data Channel SDA. DDCSDA is 5V tolerance input.
L17	DDCSCL / G_GPIO[10]	I/O	I p/u	Display Data Channel SCL. DDCSCL is 5V tolerance input.
L19	HOTPLUG / G_GPIO[11]	I/O	I p/d	Hot Plug Detect. HOTPLUG is 5V tolerance input.

*G_GPIO8 can trigger interrupt.

ADC & Touch Panel Interface

Pin No.	Name	Type	Reset	Descriptions
P11	AD_IN0	AI	-	General ADC Input
P12	AD_IN1	AI	-	General ADC Input
N12	AD_IN2	AI	-	General ADC Input
M12	AD_IN3	AI	-	General ADC Input
L13	AD_IN4	AI	-	General ADC Input

M13	A D_IN5	AI	-	General ADC Input
N13	A D_IN6	AI	-	General ADC Input
P13	A D_IN7	AI	-	General ADC Input
P14	TP_YP	AI	-	Touch Panel Control Interface
N14	TP_XM	AI	-	Touch Panel Control Interface

ADC pinmux table

	ADC		GYRO		TP	
AD_IN0	I	AD_IN0				
AD_IN1	I	AD_IN1				
AD_IN2	I	AD_IN2				
AD_IN3	I	AD_IN3				
AD_IN4	I	AD_IN4	I	GYRO_IN1		
AD_IN5	I	AD_IN5	I	GYRO_IN2		
AD_IN6	I	AD_IN6			I	TPXP
AD_IN7	I	AD_IN7			I	TPYM
TP_YP					I	TPYP
TP_XM					I	TPXM

Memory Card Interface

Pin No.	Name	Type	Reset	Descriptions
C11	MC0 / C_GPIO[0]	I/O	I p/u	Memory Card Interface
C10	MC1 / C_GPIO[1]	I/O	I p/u	Memory Card Interface
B10	MC2 / C_GPIO[2]	I/O	I p/u	Memory Card Interface
A10	MC3 / C_GPIO[3]	I/O	I p/u	Memory Card Interface
A9	MC4 / C_GPIO[4]	I/O	I p/u	Memory Card Interface
B9	MC5 / C_GPIO[5]	I/O	I p/u	Memory Card Interface
C9	MC6 / C_GPIO[6]	I/O	I p/u	Memory Card Interface
C8	MC7 / C_GPIO[7]	I/O	I p/u	Memory Card Interface
B8	MC8 / C_GPIO[8]	I/O	I p/u	Memory Card Interface
A8	MC9 / C_GPIO[9]	I/O	I p/u	Memory Card Interface
A7	MC10 / C_GPIO[10]	I/O	I p/u	Memory Card Interface

B7	MC11 / C_GPIO[11]	I/O	I p/u	Memory Card Interface
C7	MC12 / C_GPIO[12]	I/O	I p/u	Memory Card Interface
C6	MC13 / C_GPIO[13]	I/O	I p/d	Memory Card Interface
B6	MC14 / C_GPIO[14]	I/O	I p/d	Memory Card Interface
A6	MC15 / C_GPIO[15]	I/O	I p/d	Memory Card Interface
A5	MC16 / C_GPIO[16]	I/O	I p/u	Memory Card Interface
B5	MC17 / C_GPIO[17]	I/O	I p/d	Memory Card Interface
C5	MC32 / C_GPIO[32]	I/O	I p/u	Memory Card Interface
A4	MC33 / C_GPIO[33]	I/O	I p/u	Memory Card Interface
B4	MC34 / C_GPIO[34]	I/O	I p/u	Memory Card Interface
C4	MC35 / C_GPIO[35]	I/O	I p/u	Memory Card Interface
A1	MC36 / C_GPIO[36]*	I/O	I p/d	Memory Card Interface
A2	MC37 / C_GPIO[37]*	I/O	I p/d	Memory Card Interface
A3	MC38 / C_GPIO[38]*	I/O	I p/d	Memory Card Interface
B3	MC39 / C_GPIO[39]*	I/O	I p/d	Memory Card Interface
B2	MC46 / C_GPIO[46]	I/O	I p/u	Memory Card Interface
B1	MC47 / C_GPIO[47]	I/O	I p/u	Memory Card Interface
C1	MC48 / C_GPIO[48]	I/O	I p/u	Memory Card Interface
C2	MC49 / C_GPIO[49]	I/O	I p/u	Memory Card Interface
C3	MC50 / C_GPIO[50]*	I/O	I p/u	Memory Card Interface
D3	MC51 / C_GPIO[51]*	I/O	I p/u	Memory Card Interface
D2	MC52 / C_GPIO[52]	I/O	I p/u	Memory Card Interface
D1	MC53 / C_GPIO[53]	I/O	I p/u	Memory Card Interface
E1	MC54 / C_GPIO[54]	I/O	I p/u	Memory Card Interface

E2	MC55 / C_GPIO[55]	I/O	I p/u	Memory Card Interface
E3	MC56 / C_GPIO[56]	I/O	I p/u	Memory Card Interface

C_GPIO 36, 37, 38, 39, 50, 51 can trigger interrupt.

Memory card interface pinmux table

	SM/NAND		xD Socket		SD/MMC		MS/MS-PRO		Parallel ROM / Flash		Serial Flash	
MC0	IO	SM_D0				SDIO_D0 *(1)			IO	P_D0	I	S_DI
MC1	IO	SM_D1				SDIO_D1 *(1)			IO	P_D1	O	S_DO
MC2	IO	SM_D2				SDIO_D2 *(1)			IO	P_D2	IO	S_SCK
MC3	IO	SM_D3				SDIO_D3 *(1)			IO	P_D3		
MC4	IO	SM_D4	IO	SM_D4		SDIO_CMD *(1)			IO	P_D4		
MC5	IO	SM_D5							IO	P_D5		
MC6	IO	SM_D6							IO	P_D6		
MC7	IO	SM_D7	IO	SM_D7					IO	P_D7		
MC8	O	NAND_/CS0										
MC9	O	NAND_/CS1							O	P_/CS0	IO	S_CS
MC10	O	xD_/CS	IO	SM_D5	O	SDIO_CLK	O	MS_BS				
MC11	O	SM_/WE	O	SM_/WE					O	P_/WE		
MC12	O	SM_/RE	O	SM_/RE					O	P_/OE		
MC13	O	SM_CLE	O	SM_CLE					IO	P_A0(D15)		
MC14	O	SM_ALE	O	SM_ALE					O	P_A1		
MC15	O	NAND_/WP										
MC16	I	SM_RDY	I	SM_RDY								
MC17	O	xD_/WP	O	xD_/WP								
MC32			IO	SM_D0	IO	SDIO_D0 *(0)			O	P_A16		
MC33			IO	SM_D1	IO	SDIO_D1 *(0)			O	P_A2		
MC34			IO	SM_D2	IO	SDIO_D2 *(0)			O	P_A3		
MC35			IO	SM_D3	IO	SDIO_D3 *(0)			O	P_A4		
MC36					IO	MMC_D4	IO	MS_D4	O	P_A5		
MC37					IO	MMC_D5	IO	MS_D5	O	P_A6		
MC38					IO	MMC_D6	IO	MS_D6	O	P_A7		
MC39					IO	MMC_D7	IO	MS_D7	O	P_A8		
MC46			IO	SM_D6	IO	SDIO_CMD *(0)	O	MS_CLK				
MC47					O	SDIO2_CLK						
MC48					IO	SDIO2_CMD						

MC49					IO	SDIO2_D0			O	P_A9		
MC50					IO	SDIO2_D1			O	P_A10		
MC51					IO	SDIO2_D2			O	P_A11		
MC52					IO	SDIO2_D3			O	P_A12		
MC53							IO	MS_D3	O	P_A13		
MC54							IO	MS_D2	O	P_A14		
MC55							IO	MS_D1	O	P_A15		
MC56			O	xD_/CS			IO	MS_D0				

*(0) SD pin mode 0 pin out position.

*(1) SD pin mode 1 pin out position.

DDR1/2 SDRAM Interface

Pin No.	Name	Type	Reset	Descriptions
W11	DR_D0	I/O	-	DDR1/2 data input/output.
V11	DR_D1	I/O	-	
V10	DR_D2	I/O	-	
U10	DR_D3	I/O	-	
U9	DR_D4	I/O	-	
W10	DR_D5	I/O	-	
U11	DR_D6	I/O	-	
V12	DR_D7	I/O	-	
W15	DR_D8	I/O	-	
W14	DR_D9	I/O	-	
U14	DR_D10	I/O	-	
U13	DR_D11	I/O	-	
V13	DR_D12	I/O	-	
V14	DR_D13	I/O	-	
V15	DR_D14	I/O	-	
U16	DR_D15	I/O	-	
V5	DR_A0	I/O	-	DDR1/2 address output.
U4	DR_A1	O	-	
W5	DR_A2	O	-	
U3	DR_A3	O	-	
W4	DR_A4	O	-	
V3	DR_A5	O	-	
W3	DR_A6	O	-	
V1	DR_A7	O	-	
W2	DR_A8	O	-	
U2	DR_A9	O	-	
V4	DR_A10	O	-	
V2	DR_A11	O	-	
W1	DR_A12	O	-	
U5	DR_A13/BA2	O	-	DDR1/2 bank address or address output.
U6	DR_BA0	O	-	DDR1/2 bank address outputs.

V6	DR_BA1	O	-	
W6	DR_CAS#	O	-	DDR1/2 command output.
U8	DR_RAS#	O	-	
U7	DR_WE#	O	-	
W7	DR_CS#	O	-	DDR1/2 chip select.
U12	DR_DM0	O	-	DDR1/2 data mask.
U15	DR_DM1	O	-	
W12	DR_DQS0	I/O	-	DDR1/2 data strobe for lower byte.
V16	DR_DQS1	I/O	-	DDR1/2 data strobe for upper byte.
W13	DR_DQS0#	I/O	-	DDR2 data strobe for lower byte when differential data strobe mode is enable.
W16	DR_DQS1#	I/O	-	DDR2 data strobe for upper byte when differential data strobe mode is enabled.
W8	DR_CLK	O	-	DDR1/2 differential clock output.
V8	DR_CLK#	O	-	
V7	DR_CKE	O	-	DDR1/2 clock enable.

USB Interface

Pin No.	Name	Type	Reset	Descriptions
A14	VBUS	AI	-	USB VBUS input. VBUS is 5V tolerance input.
A15	DM	AI/O	-	USB differential data pairs minus side.
B15	DP	AI/O	-	USB differential data pairs plus side.
C14	USB_RREF	AI	-	USB reference resistor. A 12kOhm/1% resistor should be tied to this pin and ground.

PWM

Pin No.	Name	Type	Reset	Descriptions
F3	PWM0 / S_GPIO[9] / BST[0]	I/O		PWM output pin and boot strap setting. BST[3..0] configure the boot source. Boot source selection: 0000: NAND with Hamming ECC - Support 512bytes/2Kbytes/4Kbytes page 0001: xD with Hamming ECC (with XD SOCKET) - Support Normal type/ M type/ H type xD 0010: NAND without ECC - Support 512bytes/2Kbytes/4Kbytes page 0011: USB (Auto speed detection) 0100: SDIO (SD_PINMODE = 0) - Support SD/SDHC 0101: CF True IDE/ATA mode - Support CF at True IDE mode, ATA 48 bits addressing and host protected area 0110: MS - Support MS-Pro/MS-HG 0111: NOR Flash 1000: NAND with RS ECC - Support 512bytes/2Kbytes/4Kbytes page
F2	PWM1 / S_GPIO[10] / BST[1]	I/O		
F1	PWM2 / S_GPIO[11] / BST[2]	I/O		
G1	PWM3 / S_GPIO[12] / BST[3]	I/O		

				1001: SDIO2 - Support SD/SDHC 1010: xD without Hamming ECC (with XD SOCKET) - Support Normal type/ M type/ H type xD 1011: Serial Flash (SPI) - Support 3 bytes address 1100: USB (Force full speed) 1101: SDIO (SD_PINMODE = 1) - Support SD/SDHC 1110: xD with Hamming ECC (without XD_SOCKET) - Support Normal type/ M type/ H type xD 1111: xD without Hamming ECC (without XD_SOCKET) - Support Normal type/ M type/ H type xD
G2	PWM4 / S_GPIO[13]	I/O		PWM output pin.
G3	PWM5 / S_GPIO[14]	I/O		PWM output pin.
H3	PWM6 / S_GPIO[15]	I/O		PWM output pin.
H2	PWM7 / S_GPIO[16] / BST[8]	I/O		PWM output pin and boot strap setting. BST[8] is for debug only. Please keep this pin low at reset signal rising edge.

DGPIO

Pin No.	Name	Type	Reset	Descriptions
F8	DGPIO0*	I/O	Ip/d	General purpose input/output pin.
F7	DGPIO1*	I/O	Ip/d	General purpose input/output pin.
F6	DGPIO2*	I/O	Ip/d	General purpose input/output pin.
G6	DGPIO3*	I/O	Ip/d	General purpose input/output pin.
G7	DGPIO4*	I/O	Ip/d	General purpose input/output pin.
H7	DGPIO5*	I/O	Ip/d	General purpose input/output pin.
H6	DGPIO6*	I/O	Ip/d	General purpose input/output pin.

DGPIO0~9 can trigger interrupt.

GPIO pinmux table

	DGPIO		CCIR IN (16 bits)		CCIR IN (8 bits)		Dedicate PIN	
DGPIO0	IO	DGPIO0	I	Field	I	Field		
DGPIO1	IO	DGPIO1	I	C0				
DGPIO2	IO	DGPIO2	I	C1				
DGPIO3	IO	DGPIO3	I	C2				
DGPIO4	IO	DGPIO4	I	C3				
DGPIO5	IO	DGPIO5					I	PICNT

DGPIO6	IO	DGPIO6					I	Card Detect

RTC & Power Button Control (PWBC)

Pin No.	Name	Type	Reset	Descriptions
P7	PWR_SW	I	I	Power on/off signal input.
P6	PWR_EN	O	O	Power switch or power IC enable signal output.
L1	XTAL_RTCI	AI	-	Real time clock input. Connect to 32768Hz crystal.
L2	XTAL_RTCO	AO	-	Real time clock output. Connect to 32768Hz crystal.

Embedded Audio Codec

Pin No.	Name	Type	Reset	Descriptions
P17	MIC_RINP	AI	-	Right channel microphone differential input positive side.
P18	MIC_RINN	AI	-	Right channel microphone differential input negative side.
R17	MIC_BIAS	AO	-	Microphone working bias output.
P19	MIC_RI	AI	-	Right channel DC canceling input path. Connect 1uF capacitor to MIC_RO.
R19	MIC_RO	AO	-	Right channel DC canceling output path. Connect 1uF capacitor to MIC_RI.
R18	AUD_VMIDX	AO	-	Decoupling for audio codec reference voltage. Connect 4.7uF capacitor to ground.
T19	AUD_RADJ	AI	-	Reference resistor for audio codec. Connector 12kohm resistor to ground.
U19	HPR	AO	-	Right channel headphone output.
V19	HPL	AO	-	Left channel headphone output.
W18	SPKR	AO	-	Speaker output positive side. Connect speaker to SPKL for BTL mode application.
V18	SPKL	AO	-	Speaker output negative side. Connect speaker to SPKL for BTL mode application.

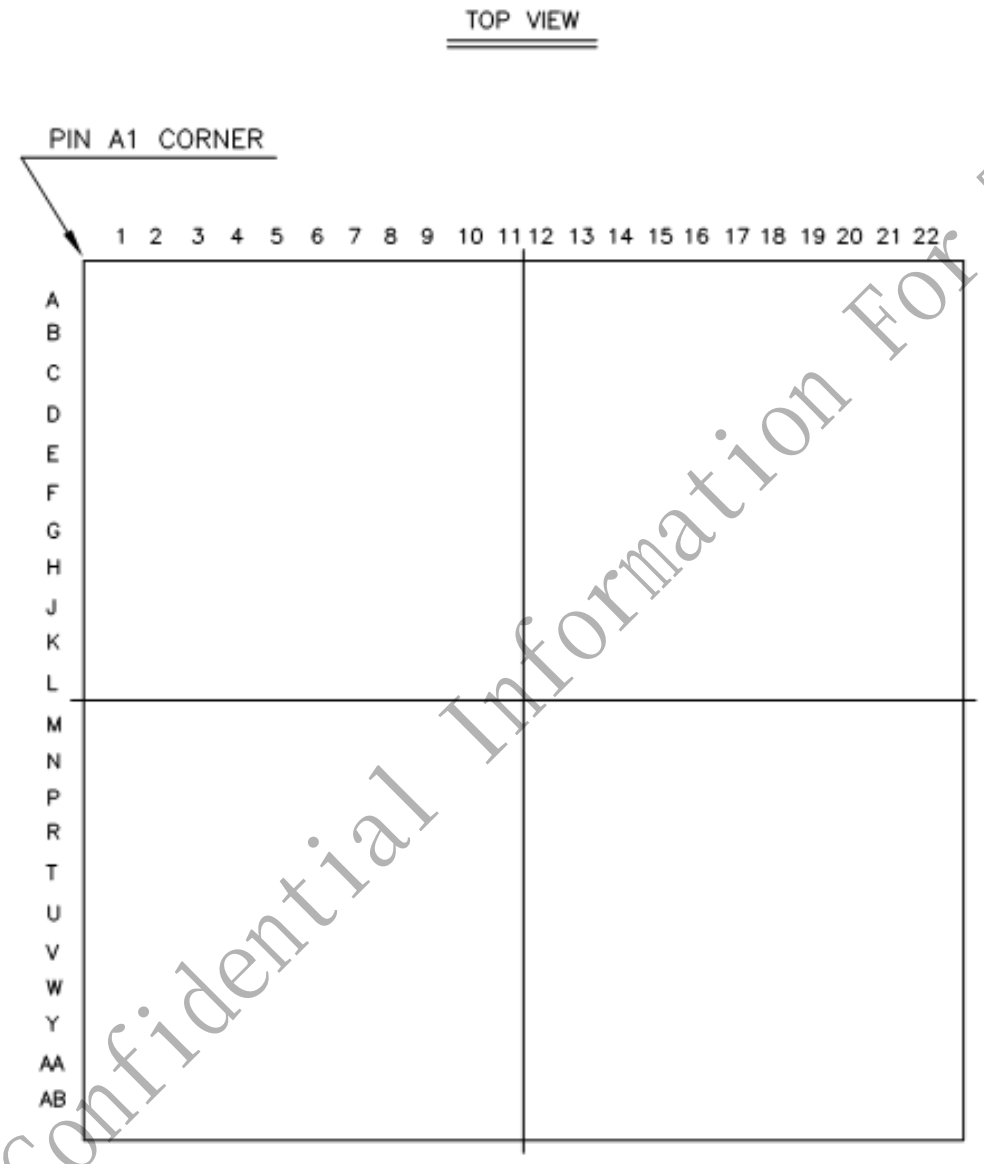
Power

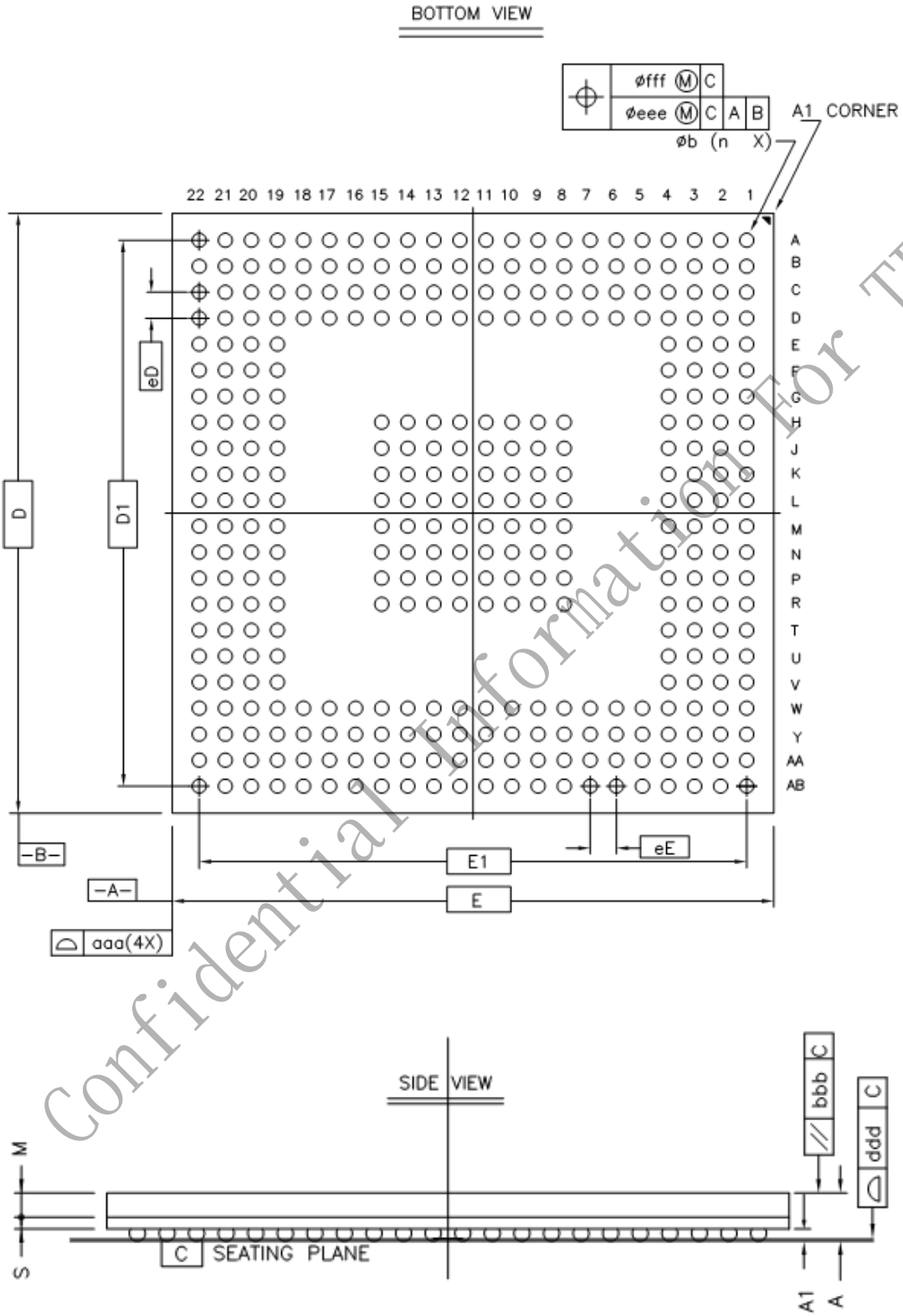
Pin No.	Name	Descriptions
F9,F10,G9,G10,J6, J7,J13,J14,K6,K7, K13,K14,N9,N10,P9, P10	VCC1V2	1.2V core power.
D8,D9,D10,D11,H4, J4,J16,K4,K16,L4, L16,M16	VDD3V3	3.3V I/O power.
P2	VDD_SN	Sensor multi-level I/O power. (3.3V/2.5V/1.8V)
B17,B18	VDD_LCD	LCD multi-level I/O power. (3.3V/2.5V/1.8V)
D4,D12,D16,G8,H8, H9,H10,H11,H16,J8, J9,J10,J11,J12,K8,	DGND	Digital ground.

K9,K10,K11,K12,L8, L9,L10,L11,L12,M4, M9,M10,M11,T4,T16		
M14	AVDD_ADC	3.3V general ADC power.
N11	AGND_ADC	General ADC analog ground.
N18	AVDD_DAC	3.3V DAC power.
M18	AGND_DAC	DAC analog ground.
N17	AVDD_AUD	3.3V audio codec ground.
T18	AGND_AUD	Audio codec analog ground.
W19	AVDD_AX	3.3V Audio output buffer power.
U18	AGND_AX	Audio output buffer analog ground.
B16	AVDD_HSRT	3.3V USB high speed receiver/transmitter power.
C15	AGND_HSRT	USB high speed receiver/transmitter analog ground.
C16	AVDD_USB	3.3V USB analog power.
B14	AGND_USB	USB analog ground.
K1	VDD_RTC	Real time clock power.
N6	VDD_VBAT	PWBC block power.
A19	VCC_PLL	1.2V PLL power.
A18	GND_PLL	PLL ground.
V17	VCC_DLL	1.2V DLL power
W17	GND_DLL	DLL ground.
T8,T9,T10,T11,T12, U17,V9	VDD_DDR	DDR I/O power. 2.5V for DDR1; 1.8V for DDR2
W9	VDD_VREF	DDR I/O reference voltage. 1.25V for DDR1; 0.9V for DDR2
L14	AVDD_TP	3.3V touch panel controller power
T17	AGND_TP	Touch panel controller ground.
G17,H17	AVDD_HDMI	1.2V HDMI transmitter analog power
J17,K17	AGND_HDMI	HDMI transmitter analog ground.

Package Outline

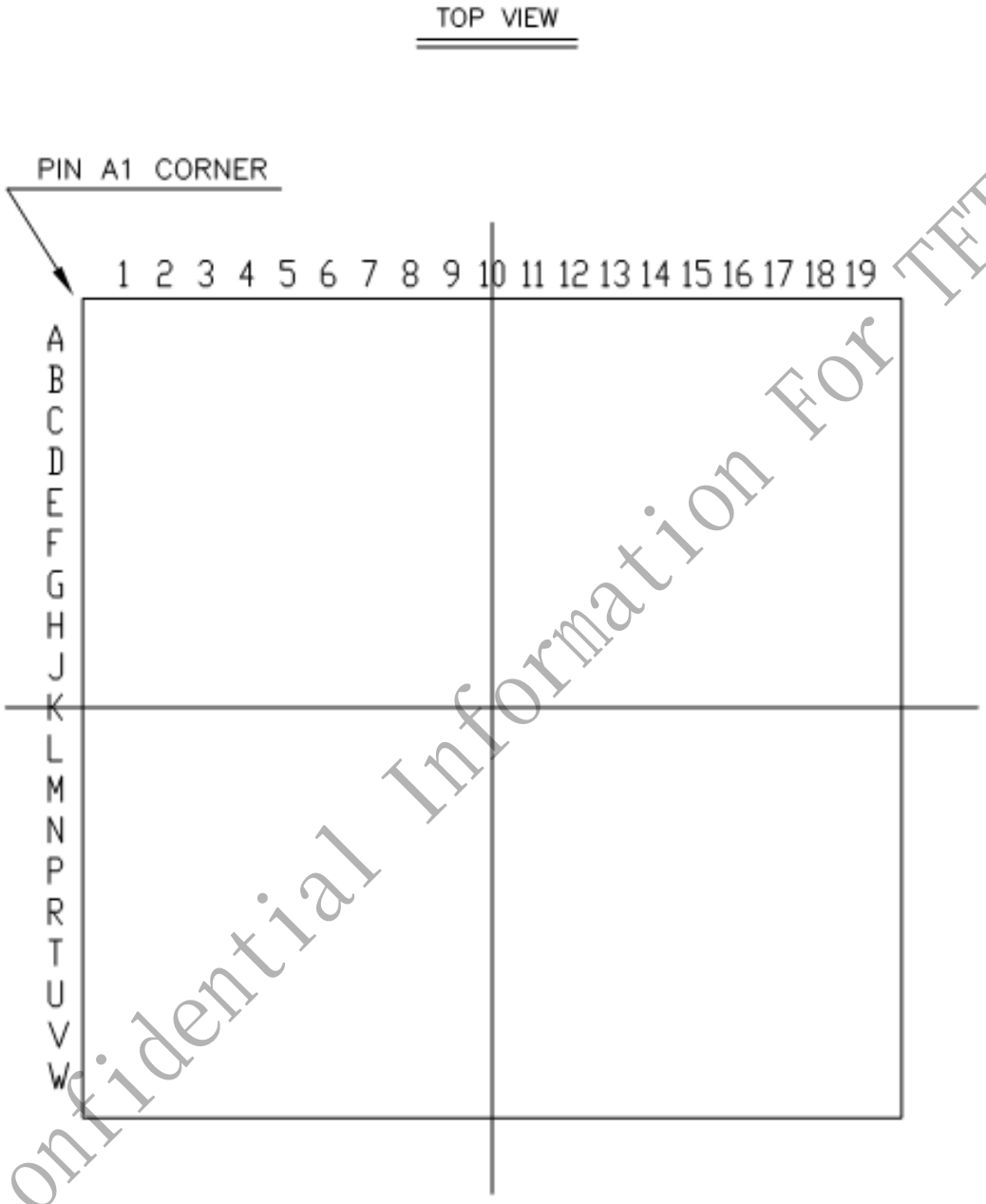
NT96630BG: TFBGA-352

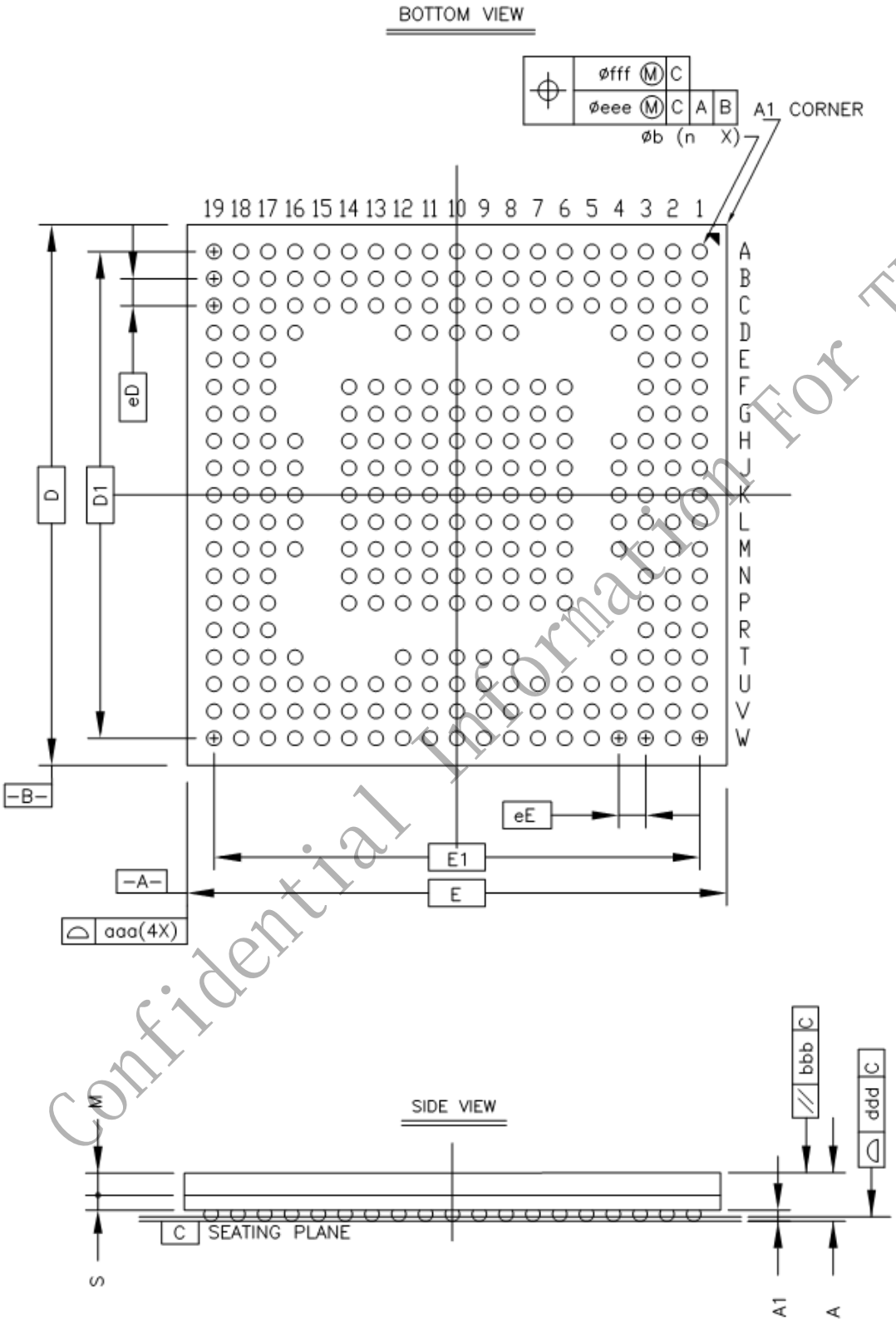




		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	15.000
	Y	D	15.000
Ball Pitch :	X	eE	0.650
	Y	eD	0.650
Total Thickness :		A	1.200 MAX.
Mold Thickness :		M	0.530 Ref.
Substrate Thickness :		S	0.260 Ref.
Ball Diameter :			0.350
Stand Off :		A1	0.220 ~ 0.320
Ball Width :		b	0.320 ~ 0.420
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	352
Edge Ball Center to Center :	X	E1	13.650
	Y	D1	13.650

NT96632BG: TFBGA-297





		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	13.000
	Y	D	13.000
Ball Pitch :	X	eE	0.650
	Y	eD	0.650
Total Thickness :		A	1.200 max
Mold Thickness :		M	0.530 Ref.
Substrate Thickness :		S	0.360 Ref.
Ball Diameter :			0.350
Stand Off :		A1	0.220 ~ 0.320
Ball Width :		b	0.320 ~ 0.420
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	297
Edge Ball Center to Center :	X	E1	11.700
	Y	D1	11.700

Electrical Characteristics

Absolute Maximum Ratings

Core Power Supply	-0.3	to	1.68V
DC Supply Voltage	-0.3	to	4.0V
Input/Output Voltage	-0.3	to	4.0V
Operating Ambient Temperature	-10°C	to	+70°C
Storage Temperature	-40°C	to	+125°C

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

(V_{CC}=1.2V, V_{DD}=3.3V, GND=0V, Temp=25°C)

V_{CC} & V_{DD}

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{CC}	Core Logic Operating Voltage	1.08	1.2	1.32	V	
V_{DD}	I/O Interface Operating Voltage	3.0	3.3	3.6	V	
V_{DDRTC}	RTC Operating Voltage	1.2	3.3	3.6	V	
V_{DDPLL}	PLL Operating Voltage	1.08	1.2	1.32	V	
V_{DDDLL}	DLL Operating Voltage	1.08	1.2	1.32	V	
V_{DDHSRT}	USB Transceiver Operating Voltage	3.0	3.3	3.6	V	
V_{DDUSB}	USB Analog Block Operating Voltage	3.0	3.3	3.6	V	
V_{DDDAC}	Video DAC Operating Voltage	3.0	3.3	3.6	V	
V_{DDADC}	ADC Operating Voltage	3.0	3.3	3.6	V	
P_{RUN}	Operating Power Consumption	-	TBD	-	mW	
V_{IH}	Input High Voltage	2.0	-	-	V	
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{T+}	Schmitt Trigger Positive Going Threshold	-	1.5	2.0	V	
V_{T-}	Schmitt Trigger Negative	0.8	1.3	-	V	

	Going Threshold					
I_{OH}	Output Driving Current	2	-	-	mA	$V_{OH}=V_{DD}$-0.4V, 2mA setting
		4	-	-	mA	$V_{OH}=V_{DD}$-0.4V, 4mA setting
		6	-	-	mA	$V_{OH}=V_{DD}$-0.4V, 6mA setting
		8	-	-	mA	$V_{OH}=V_{DD}$-0.4V, 8mA setting
I_{OL}	Output Sinking Current	2	-	-	mA	V_{OL}=GND+0.4V, 2mA setting
		4	-	-	mA	V_{OL}=GND+0.4V, 4mA setting
		6	-	-	mA	V_{OL}=GND+0.4V, 6mA setting
		8	-	-	mA	V_{OL}=GND+0.4V, 8mA setting
I_{IL}	Input Leakage Current	-	±1	±10	uA	$V_{OUT}=V_{DD}$/GND
R_{PU}	Internal Pull-up Resistor	40	75	190	KΩ	$V_{IN}=V_{DD}$/GND

V_{DD_LCD} & V_{DD_SEN} (Multi-voltage I/O)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD_LCD} & V_{DD_SEN}	3.3V power supply	2.97	3.3	3.63	V	
	2.5V power supply	2.25	2.5	2.75	V	
	1.8V power supply	1.62	1.8	1.98	V	
I_{IN}	Input leakage current		±1		uA	
DC Characteristics of Multi-voltage I/O Operating at 3.3V						
V_{IH}	Input High Voltage	2.0	-	-	V	3.3V LVTTL
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{T+}	Schmitt Trigger Positive Going Threshold	-	1.58	2.0	V	3.3V LVTTL
V_{T-}	Schmitt Trigger Negative Going Threshold	0.8	1.1	-	V	
V_{OH}	Output high voltage	2.4	-	-	V	$\|I_{OH}\|$ = 2mA ~ 16mA
V_{OL}	Output low voltage	-	-	0.4	V	$\|I_{OL}\|$ = 2mA ~ 16mA
R_{PU}	Internal pull-up resistor	40	75	190	KΩ	
R_{PD}	Internal pull-down resistor	40	75	190	KΩ	
DC Characteristics of Multi-voltage I/O Operating at 2.5V						
V_{IH}	Input High Voltage	0.7*V_{CC}	-	-	V	2.5V CMOS
V_{IL}	Input Low Voltage	-	-	0.3*V_{CC}	V	
V_{T+}	Schmitt Trigger Positive Going Threshold	-	1.26	0.7*V_{CC}	V	2.5V CMOS
V_{T-}	Schmitt Trigger Negative Going Threshold	0.3*V_{CC}	0.83	-	V	
V_{OH}	Output high voltage	1.85	-	-	V	$\|I_{OH}\|$ = 1.5mA ~ 12mA
V_{OL}	Output low voltage	-	-	0.4	V	$\|I_{OL}\|$ = 1.5mA ~ 12mA
R_{PU}	Internal pull-up resistor	50	110	250	KΩ	
R_{PD}	Internal pull-down resistor	50	110	290	KΩ	
DC Characteristics of Multi-voltage I/O Operating at 1.8V						
V_{IH}	Input High Voltage	0.7*V_{CC}	-	-	V	1.8V CMOS
V_{IL}	Input Low Voltage	-	-	0.3*V_{CC}	V	
V_{T+}	Schmitt Trigger Positive Going Threshold	-	1.00	0.7*V_{CC}	V	1.8V CMOS
V_{T-}	Schmitt Trigger Negative Going Threshold	0.3*V_{CC}	0.6	-	V	

V_{OH}	Output high voltage	0.75*V_{CC}	-	-	V	$\|I_{OH}\|$ = 0.9mA ~ 7.2mA
V_{OL}	Output low voltage	-	-	0.4	V	$\|I_{OL}\|$ = 0.9mA ~ 7.2mA
R_{PU}	Internal pull-up resistor	85	200	455	KΩ	
R_{PD}	Internal pull-down resistor	80	210	515	KΩ	

DDR SDRAM (SSTL2 mode)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD_DDR}	DDR I/O Supply Voltage	2.3	2.5	2.7	V	
V_{REF_DDR}	DDR I/O Reference Voltage	1.13	1.25	1.38	V	
V_{TT}	I/O termination voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	
$V_{IH(DC)\_DDR}$	DDR I/O DC Input High (Logic 1) Voltage	V_{REF_DDR} + 0.15	-	V_{DD_DDR} + 0.3	V	
$V_{IL(DC)\_DDR}$	DDR I/O DC Input Low (Logic 0) Voltage	-0.3	-	V_{REF_DDR} - 0.15	V	
$V_{IH(AC)\_DDR}$	DDR I/O AC Input High (Logic 1) Voltage	V_{REF_DDR} + 0.31	-	V_{DD_DDR} + 0.3	V	
$V_{IL(AC)\_DDR}$	DDR I/O AC Input Low (Logic 0) Voltage	-0.3	-	V_{REF_DDR} - 0.31	V	
V_{ID}	Input differential voltage for differential input	0.30	-	V_{DD_DDR} + 0.6	V	
I_{OH_DDR}	DDR I/O Output Driving Current	7.6	-	-	mA	V_{OH}=1.68V
I_{OL_DDR}	DDR I/O Output Sinking Current	7.6	-	-	mA	V_{OL}=0.54V
I_{IL_DDR}	Input Leakage Current	-2	-	2	uA	0< V_{IN}< V_{DD_DDR}

DDRII SDRAM (SSTL-18 mode)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD_DDR}	DDR I/O Supply Voltage	1.7	1.8	1.9	V	
V_{REF_DDR}	DDR I/O Reference Voltage	0.833	0.9	0.969	V	
$V_{IH(DC)\_DDR}$	DDR I/O DC Input High (Logic 1) Voltage	V_{REF_DDR} + 0.125	-	V_{DD_DDR} + 0.3	V	
$V_{IL(DC)\_DDR}$	DDR I/O DC Input Low (Logic 0) Voltage	-0.3	-	V_{REF_DDR} - 0.125	V	
$V_{IH(AC)\_DDR}$	DDR I/O AC Input High (Logic 1) Voltage	V_{REF_DDR} + 0.25	-	V_{DD_DDR} + 0.3	V	
$V_{IL(AC)\_DDR}$	DDR I/O AC Input Low (Logic 0) Voltage	-0.3	-	V_{REF_DDR} - 0.25	V	
V_{ID}	Input differential voltage for differential input	0.30	-	V_{DD_DDR} + 0.6	V	
I_{OH_DDR}	DDR I/O Output Driving Current	4.6		-	mA	V_{OH}=1.42V
I_{OL_DDR}	DDR I/O Output Sinking Current	4.6		-	mA	V_{OL}=0.28V

$I_{IL\ DDR}$	Input Leakage Current	-2	-	+2	uA	0< V_{IN}< $V_{DD\ DDR}$

USB

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
USB 2.0 High Speed Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	300	-	-	mV	$\|V_{I(DP)}-V_{I(DM)}\|$ measured at the connection as application circuit
V_{HSCM}	High speed data signaling common mode voltage range	-50	-	500	mV	
V_{HSSQ}	High speed squelch detection threshold	-	-	100	mV	squelch detected
		200	-	-	mV	no squelch detected
V_{HSDSC}	High speed disconnection detection threshold	625	-	-	mV	disconnection detected
		-	-	525	mV	disconnection not detected
Output Levels						
V_{HSOI}	High speed idle level output voltage (differential)	-10	-	10	mV	
V_{HSOL}	High speed low level output voltage (differential)	-10	-	10	mV	
V_{HSOH}	High speed high level output voltage (differential)	-360	400	400	mV	
V_{CHRPJ}	Chirp-J output voltage (differential)	700	-	1100	mV	
V_{CHIRPK}	Chirp-K output voltage (differential)	-900	-	-500	mV	
$I_{DP/DM}$	Allowable output current of DM/DP	14.55	17.78	21.79	mA	The termination is 45Ω±10%
Resistance						
R_{DRV}	Driver output impedance	40.5	45	49.5	Ω	equivalent resistance used as internal chip only
Z_{HSTERM}	Differential impedance	76.5	90	103.5	Ω	
USB 1.1 Full / Low Speed Transceiver (FS/LS)						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	0.2	-	-	V	$\|V_{I(DP)}-V_{I(DM)}\|$
V_{CM}	Differential common mode voltage	0.8	-	2.5	V	
Input Levels (single-ended receivers)						
V_{SE}	Single ended receiver threshold	0.8	-	2.0	V	
Output Levels						
V_{OL}	Low-level output voltage	0	-	0.3	V	
V_{OH}	High-level output voltage	2.8	-	3.6	V	

Touch panel controller

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
	Touch panel switch on resistance		-	15	-	Ω	
	Programmable resistor range	Max	-	64	-	KΩ	
		Min	-	1	-	KΩ	
	Programmable resistor step size		-	1	-	KΩ	
	Current source (V1)	Max	-	200	-	uA	
		Min	-	100	-	uA	

HDMI Tx

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OFF}	Single-ended standby output voltage	3.125	3.3	3.475	V	
V_{SWING}	Single-ended output swing voltage	400	500	600	mV	
V_H	Single-ended high level output voltage	2.935	3.3	3.475	V	
V_L	Single-ended low level output voltage	2.435	2.8	3.065	V	

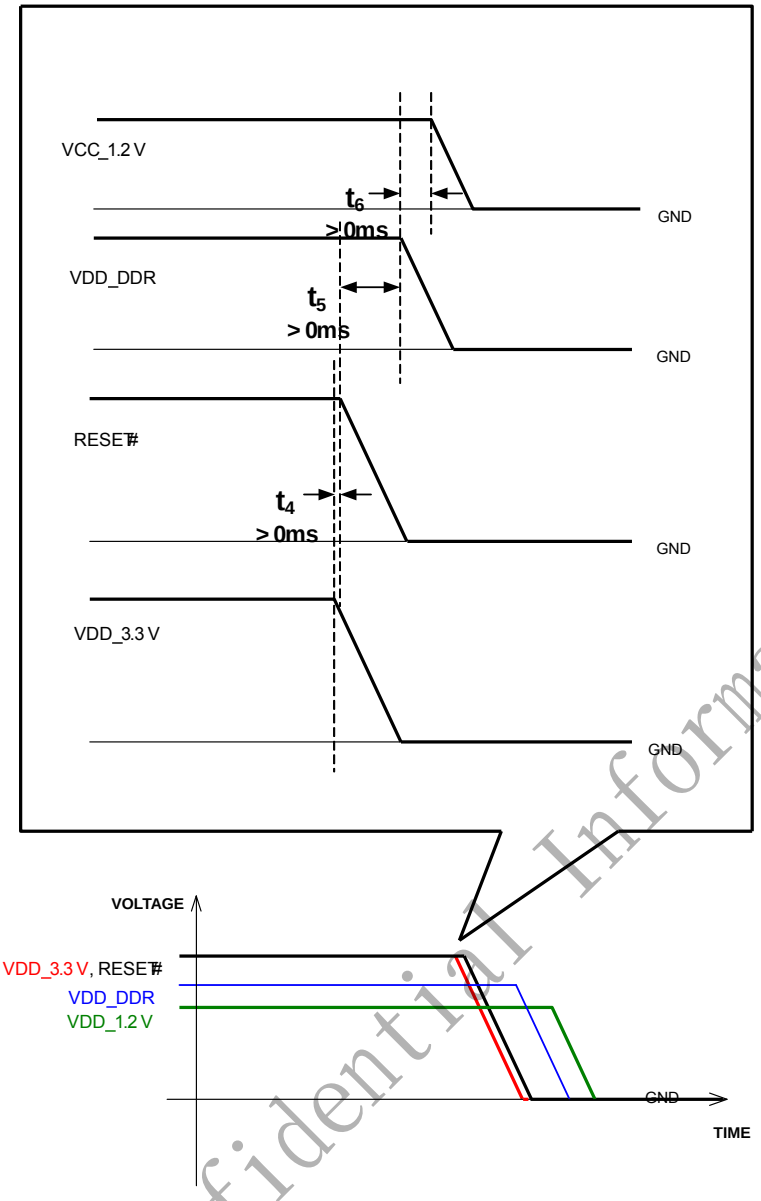
AC Characteristics

(V_{CC}=1.2V, V_{DD}=3.3V, GND=0V, Temp=25°C)

RTC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_{RTC}	RTC 32768Hz oscillator warm up time	-	265	500	ms	V_{DDRTC}=1.8V
t_{DBC}	GPIO read de-bounce time	-	3	-	clk	
t_{RST}	RESET# sustained time	1	-	-	ms	after power being stable
t_{PWR}	Core power prior to I/O power time	1	-	-	ms	

Power on sequence



POWER - OFF SEQUENCE

Note：

1. Even $t_1 \geqq 0$ ms or $t_1 < 0$ ms is acceptable, but it is necessary to make sure $t_2 > 0$ ms .
2. It is necessary that $t_{PWR} > 1$ ms.
3. It is necessary that $t_{RST} \geqq 1$ ms.
4. V_{DD_DDR} = 2.5V for using DDR SDRAM , V_{DD_DDR}=1.8V for using DDRII SDRAM

Note：

Novatek recommends that $t_4 > 0$ ms, $t_5 > 0$ ms, and $t_6 > 0$ ms for a stable system application. But they are not the required restrictions for Novatek DSP.

ADC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{Input}	ADC Input signal	0	-	3.3	V	
RES	ADC Resolution	-	8	-	bits	
INL	Integral nonlinearity	-	±1	-	LSB	
DNL	Differential nonlinearity	-	±0.5	-	LSB	

TV encoder

(V_{DDTV} =3.3V, R_{load} = 37.5Ω, V_{ref} = 1.21V, Conversion rate = 27MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RES	Video DAC Resolution	-	8	-	bits	
INL	Integral Nonlinearity, INL	-	±1	-	LSB	
DNL	Differential Nonlinearity, DNL	-	±0.5	-	LSB	
I_{code}	Output Current-DAC Code 1023 (Iout FS)	-	34.08	-	mA	
V_{code}	Out Voltage-DAC Code 1023	-	1.28	-	V	
VLE	Video Level Error	-5	-	+5	%	
V_{oc}	Output Compliance Range	0	-	1.4	V	
F_{clk}	Conversion rate	-	27	-	MHz	

Audio CODEC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Mic Input						
V_{IN}	Input full scale		-9.1		dBV	
SNR	Signal to noise ratio		-74		dBA	@-9.1dBV source , 0dB gain
THD+N	Total harmonic distortion plus noise ratio		-71		dBA	@-9.1dBV source , 0dB gain
Line Output @10KΩ load						
V_{OUT}	Line output full scale		0.698		V_{RMS}	
SNR	Signal to noise ratio		-72		dBA	
THD+N	Total harmonic distortion plus noise ratio		-69		dBA	
Headphone Output @16Ω load						
SNR	Signal to noise ratio		-73		dBA	
THD+N	Total harmonic distortion plus noise ratio		1		%	@29.11mW
			-69		dBA	@6.7mW

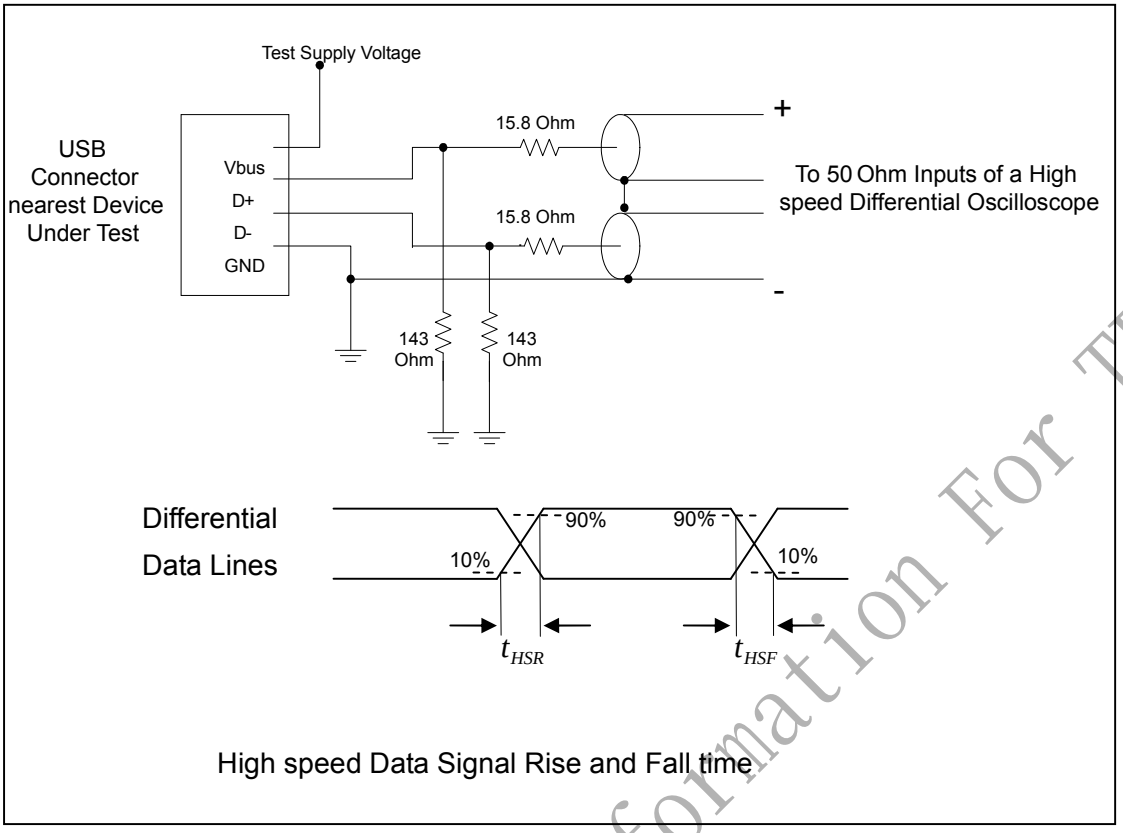
Speaker Output @8Ω BTL						
SNR	Signal to noise ratio		-77		dBA	
THD+N	Total harmonic distortion plus noise ratio		1		%	@121.5mW
			-70		dBA	@50.4mW

* The SNR of audio output is measured according to AES17-1998 CL 9.3

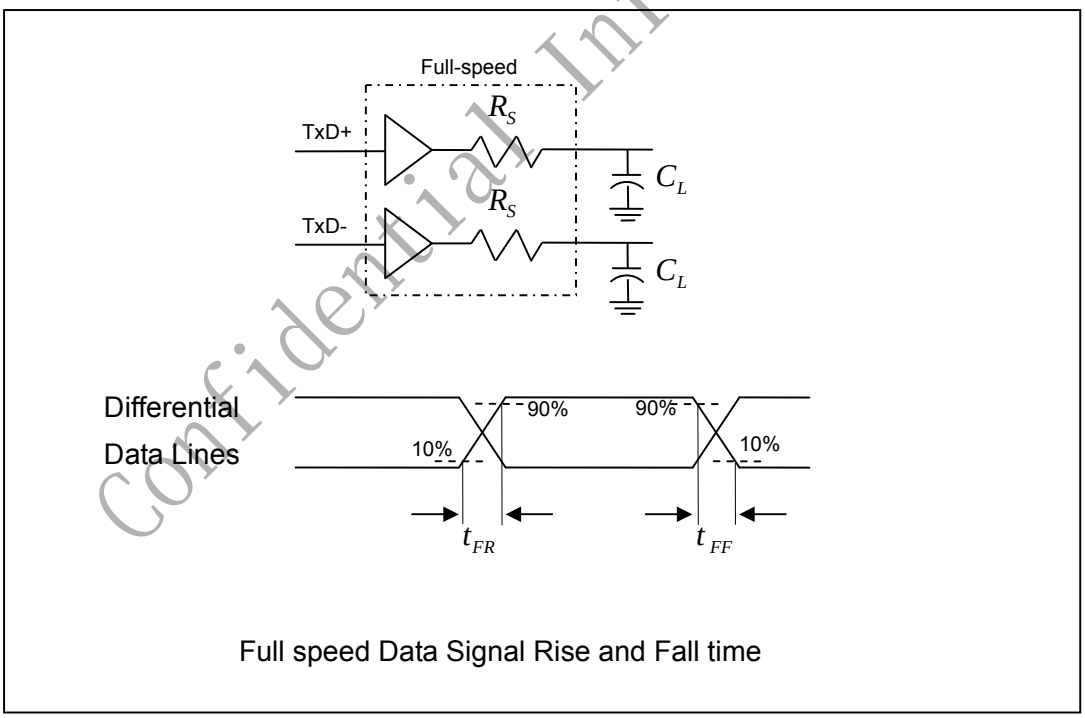
USB

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Driver Characteristics						
High speed mode						
$T_{HSDRATE}$	High speed TX data rate	479.76	-	480.24	Mbps	
$T_{HSRDRATE}$	High speed RX data rate	479.76	-	480.24	Mbps	
t_{HSR}	High speed differential rise time	500	-	-	ps	
t_{HSF}	High speed differential fall time	500	-	-	ps	
Full speed mode						
$T_{FSDRATE}$	Full speed TX data rate	11.994	-	12.006	Mbps	
$T_{FSRDRATE}$	Full speed RX data rate	11.97	-	12.03	Mbps	
t_{FR}	Rise time	4	-	20	ns	CL=50pF; 10 to 90% of $\|V_{OH}-V_OL\|$
t_{FF}	Fall time	4	-	20	ns	CL=50pF; 90 to 10% of $\|V_{OH}-V_{OL}\|$
t_{FRMA}	Differential rise/fall time matching (t_{FR}/t_{FF})	90	-	110	%	Excluding the first transition from idle mode
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V	Excluding the first transition from idle mode
Low speed mode						
$T_{LSDRATE}$	Low speed TX data rate	1.49925	-	1.50075	Mbps	
$T_{LSRDRATE}$	Low speed RX data rate	1.49625	-	1.50375	Mbps	
t_{LR}	Rise time	75	-	300	ns	CL=200pF ~ 600pF; 10 to 90% of $\|V_{OH}-V_{OL}\|$
t_{LR}	Fall time	75	-	300	ns	CL=200pF ~ 600pF; 10 to 90% of $\|V_{OH}-V_{OL}\|$
t_{FRMA}	Differential rise/fall time matching (t_{FR}/t_{FF})	80	-	125	%	Excluding the first transition in the idle mode
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V	Excluding the first transition in the idle mode
Driving timing						
High speed mode						
	Driver waveform requirement	see eye pattern of template 1				Follow template1 described in USB2.0 spec, revision 2.0.
Full speed mode						
	VI, FSE0, OE to DP, DM Propagation delay	-	-	15	ns	For a detailed description of VI, FSE0, and OE, please refer to USB 1.1

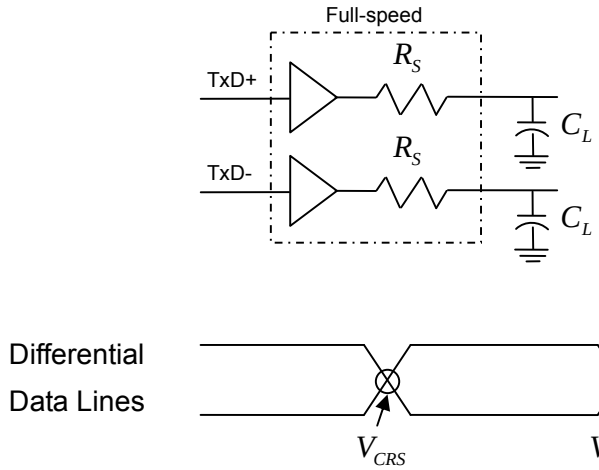
						specification.
T_{FDEOP}	Source jitter for differential transition to SE0 transition	-2	-	5	ns	
T_{JR1}	Receiver jitter	-18.5	-	18.5	ns	To next transition
T_{JR2}	Receiver jitter	-9	-	9	ns	For paired transition
T_{FEOPT}	Source SE0 interval of EOP	160	-	175	ns	
T_{FEOPR}	Receiver SE0 interval of EOP	82	-	-	ns	
T_{FST}	Width of SE0 interval during differential transition	-	-	14	ns	
Low speed mode						
T_{LDEOP}	Source jitter for differential transition to SE0 transition	-40	-	100	ns	
T_{JR1}	Receiver jitter	-75	-	75	ns	To next transition
T_{JR2}	Receiver jitter	-45	-	45	ns	For paired transition
T_{LEOPT}	Source SE0 interval of EOP	1.25	-	1.5	μs	
T_{LEOPR}	Receiver SE0 interval of EOP	670	-	-	ns	
T_{LST}	Width of SE0 interval during differential transition	-	-	210	ns	
Receiver timing						
High speed mode						
	Data source jitter and receiver jitter tolerance	see eye pattern of template 4				Follow template 4 described in USB2.0 spec, revision 2.0.
Full speed mode						
$t_{PLH(rcv)}$ $t_{PHL(rcv)}$	Receiver propagation delay(DP; DM to RX_RCV)	-	-	30	ns	For a detailed description of RCV, please refer to USB 1.1 specification.
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay(DP; DM to RX_DP, RX_DM)	-	-	30	ns	



High speed Data Signal Rise and Fall time



Full speed Data Signal Rise and Fall time



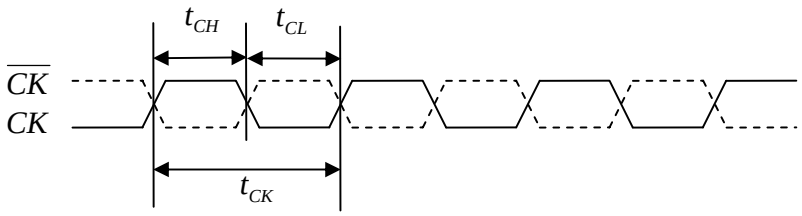
Full speed Output Signal Crossover Voltage

DDR SDRAM

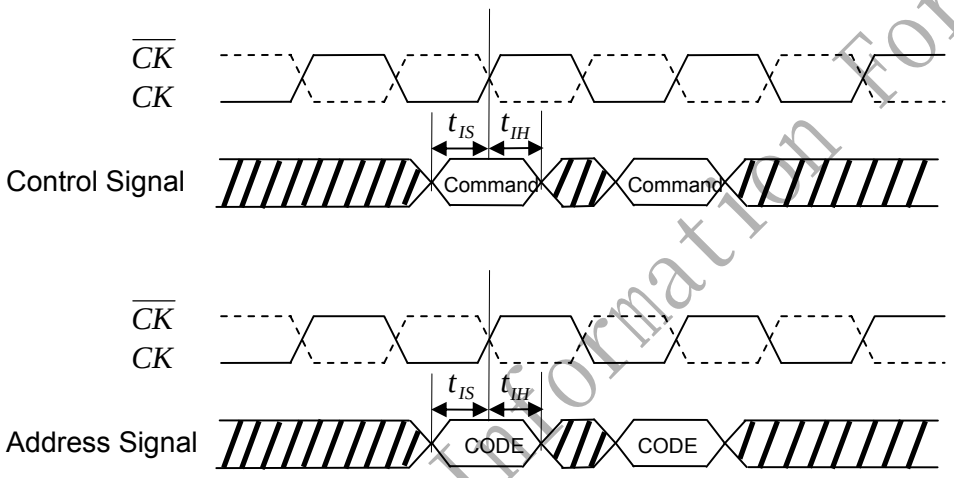
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CH}	SDRAM clock high pulse width	0.45	-	-	t_{Ck}
t_{CL}	SDRAM clock low pulse width	0.45	-	-	t_{Ck}
t_{IS}	Address and Control input setup time	0.6	-	-	ns
t_{IH}	Address and Control input hold time	0.6	-	-	ns
t_{DQSQ}	DQS--DQ Skew	-	-	0.4	ns
t_{DS}	DQ and DM input setup time	0.4	-	-	ns
t_{DH}	DQ and DM input hold time	0.4	-	-	ns

DDRII SDRAM

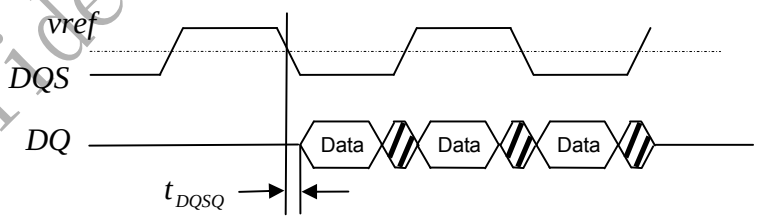
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CH}	SDRAM clock high pulse width	0.45	-	-	t_{Ck}
t_{CL}	SDRAM clock low pulse width	0.45	-	-	t_{Ck}
t_{IS}	Address and Control input setup time	0.35	-	-	ns
t_{IH}	Address and Control input hold time	0.475	-	-	ns
t_{DQSQ}	DQS--DQ Skew	-	-	0.35	ns
t_{DS}	DQ and DM input setup time	0.15	-	-	ns
t_{DH}	DQ and DM input hold time	0.275	-	-	ns



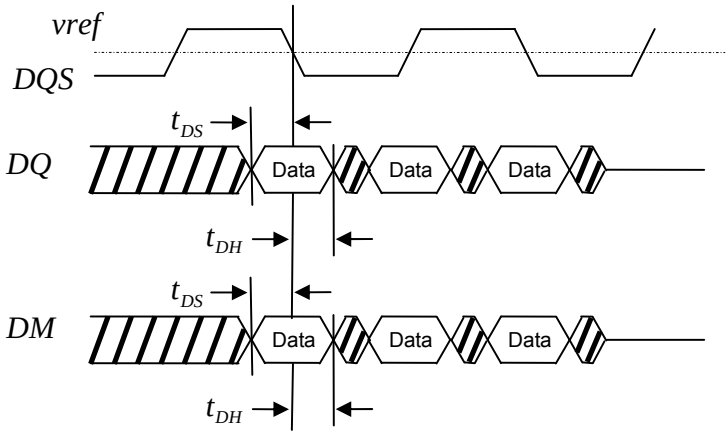
DDR clock high pulse and low pulse width



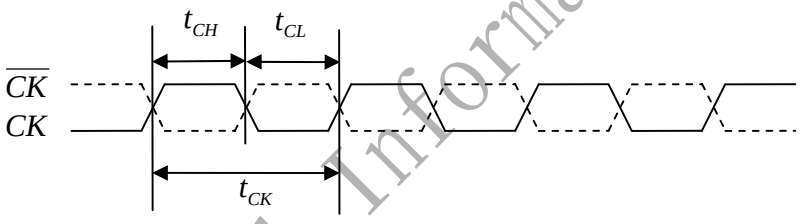
DDR Address and Control input setup time and hold



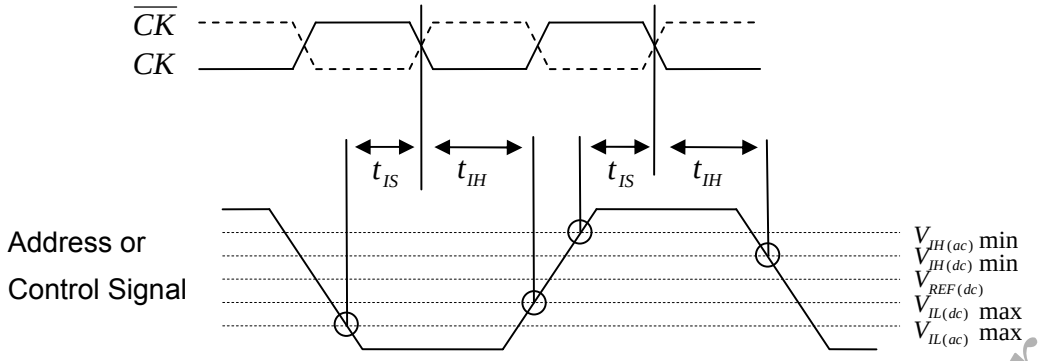
DDR DQS-DQ Skew



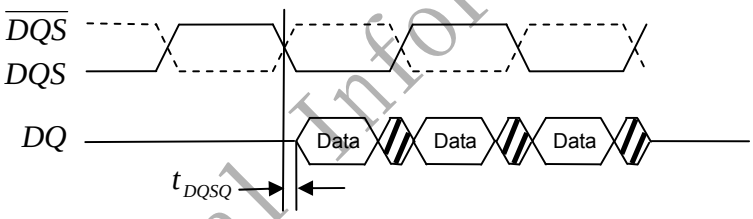
DDR DQ and DM input setup and hold time



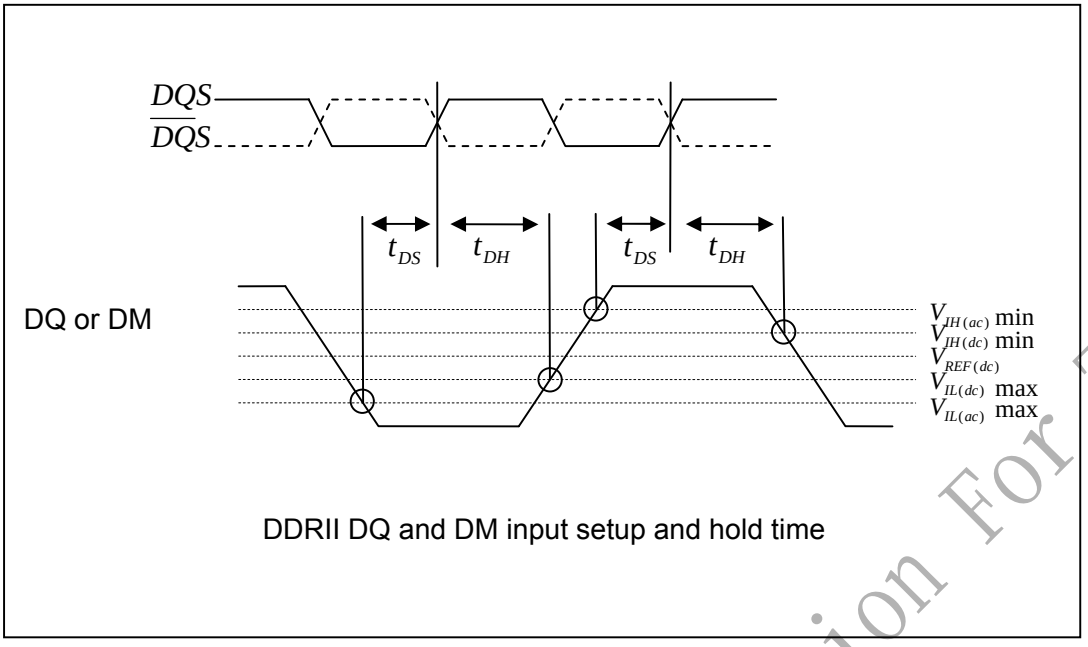
DDRII clock high pulse and low pulse width



DDRII SDRAM Address and Control input setup time



DDRII DQS-DQ Skew



DDRII DQ and DM input setup and hold time

HDMI Tx

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	Rise/fall time	75	-	-	ps	
	Intra-Pair Skew at source connector	-	-	0.15	T_{bit}	
	Inter-Pair Skew at source connector	-	-	0.20	$T_{charactracter}$	
	Clock duty cycle	40	50	60	%	
	TMDS Differential Clock Jitter	-	-	0.25	T_{bit}	