NOVATEK
聯 詠 科 技

Data Sheet

NT96655

Hybrid DSC/DV Processor

Version 0.8

Preliminary

Table of Contents

Revision History

Rev.	Date	Author	Contents
0.1	2012/02/13	Kevin Hung	First draft version.
0.2	2012/03/16	Kevin Hung	For PM
0.3	2012/09/07	Kevin Hung	Add pin number & DDR_PHY(DLL) power issue (ES version)
0.4	2012/09/28	Kevin Hung	Change AVDD_MPLL1.0V→ 1.5V Exchange function pin-out about SN_SHUTTER and SN_FLASH Exchange Microphone R-ch and L-ch Remove HV description
0.5	2012/11/29	Roy Lo	1. Update GPIO pull up/down spec 2. Change RESET, HIS, I/Oz pull up/down resistor symbol. 3. Add I/OSS driving and pull up/down DC characteristics 4. Add I/Os2 driving spec. 5. Change I/O 2.5V spec to 2.8V spec. 6. Add RESET pin Schmitt trigger level spec 7. change TV_RADJ's resistor 470→430 Ohm
0.5	2012/12/20	Roy Lo	Update DDRIII I/O driving/sinking spec.
0.5	2013/01/18	Kevin Hung	Remove DR_CS#, modify N4/K3 pin define for Ver. A/B
0.5	2013/03/11	Joel	Update CPU & DRAM max. operating frequency
0.6	2013/05/13	Kevin Hung	Modify default status of MC14 internal resistor from p/u → p/d
0.6	2013/05/14	Kevin Hung	Exchange N4/K3 pin define for Ver. B/C
0.7	2013/06/14	Kevin Hung	Add NT96656 in this common version
0.8	2013/07/30	Kevin Hung	Separate from common version

Features

- **High Performance 32-bit CPU**
  - MIPS32 24Kec with ASE DSP extension
  - MMU embedded
  - 16KB instruction and 16KB data cache
  - Embedded ICE makes firmware debugging easier
  - CPU operating frequency up to 432MHz, on the fly programmable
- **Power Management Features**
  - Firmware configurable operating frequency of each functional block to meet best power budget
  - Internal power domain partition
- **Integrated Clock Generator**
  - Internal PLL with spread spectrum capability
  - 12MHz system/USB oscillator
  - 32768Hz RTC oscillator
- **Scalable Memory Bus Architecture**
  - 16-bit DDR2 / DDR3 SDRAM bus, supporting up to 2Gb DDR SDRAM
  - DRAM operating frequency up to 373MHz without ODT
  - Tunable DDR frequency on the fly for power saving
- **Sensor Interface Engine**
  - Support up to 50M pixels CCD/CMOS image sensor
  - Support high speed serial interface like sub-LVDS/Mipi/HiSPi up to 10 channels for most commercial CMOS sensors including Sony, Panasonic, Aptina, Samsung, Sharp and Omnivision, etc. (8 channels for dual MIPI version)
  - Support parallel sensor interface for most commercial CCD sensors including Sony, Panasonic, Sharp and CMOS sensors including Aptina and Omnivision
  - Support BT.601/656 video input
  - Support dual sensors input (dual MIPI version only)
  - Support 12-bit (serial) sensor data input
  - Support high speed serial interface sensor pixel rate up to 576MPixels/sec
  - Support continuous shot up to 10 fps for 16MP sensor
  - Support parallel interface sensor pixel clock up to 108MHz
  - Support movie CCD, and horizontal division CCD of SONY

- Support multiple field, line interleaved CCD of Sharp
- Support smear reduction for CCD sensor
- Built-in color pattern generation
- Sensor black level clamping
- Efficient defect concealment algorithm
- Raw image sub-sample for video & high ISO image
- Flexible image analysis flow for AE, AWB and AF purpose
- Programmable histogram analysis
- Automatic flicker detection
- R/G/B Gamma LUT for sensor linearization correction
- In-pipeline lens shading compensation technology
- In-pipeline color shading compensation technology
- In-pipeline geometric distortion correction technology
- In-pipeline color aberration correction technology
- Support CMOS sensor spatial crosstalk cancellation
- Support in-frame dark frame subtraction with smart defect detection algorithm
- Support rolling shutter correction for CMOS sensor
- Mechanical shutter control
- Flash light control

- **Image Processing Engine**
  - Proprietary advanced anti-alias Bayer CFA color interpolation
  - Flexible edge rendering, control and enhancement
  - Powerful noise reduction technology for still and video recording
  - Support motion compensated temporal filtering (MCTF) for efficient video noise reduction
  - Support temporal noise reduction with ghost reduction
  - R/G/B Gamma LUT
  - High precision color correction matrix for sRGB or specific color requirement
  - Brightness/contrast and hue/saturation adjustment
  - Specific color control technology (Patent)
  - 3D color conversion for specific color preference tuning
  - False color suppression
  - Support wide dynamic range (WDR) for local illumination enhancement
- **Image Manipulation Engine**
  - High quality scaling engine for seamless digital zooming from 1/16x to 16x

- Support thumbnail image generation
- Forward/inverse color space transform

- **Face Detection Engine**
  - Very high speed face detection and tracking
  - High accuracy under different light source
  - Programmable target data base
- **Digital Image Stabilizer**
  - Remove unintended hand movement from an image sequence
  - Single frame compensation for video (Total compensation)
  - Accumulate frame compensation for video (Smart compensation)
  - Motion refresh rate 60Hz
  - Interface search range up to ±32
  - Programmable total compensation range
  - Accommodate resolution 1080p
  - Adjustable number of motion vectors for motion estimation. Maximum 1024 motion vectors per process (16 regions x 64 blocks/region).
- **LCD/TV Display**
  - Support dual display including LCD panel and HDMI/TV display simultaneously
  - High performance scaling up/down engine, programmable gamma correction, color transform and color management for LCD or TV display
  - Separate OSD for LCD panel and TV
  - Support digital LCD interface for AUO, Casio, CMI (all digital panels will be supported)
  - Support 16-bit RGB parallel interface (RGB565 or Delta RGB) LCD panel up to 1024x1024 resolution
  - Support MIPI DSI for mobile display
  - Support 90° rotation/flip/mirror
  - Support PAL / NTSC video encoder (CVBS format)
  - Integrated 1 internal 10-bit video DACs
  - Support digital interface BT.601/656/1120 output port
  - 3.3V / 1.8V LCD / Digital video out
- **HDMI**
  - Support HDMI v1.3a
  - Support DDC with maximum 100khz access rate for CEA-861-D format
  - Support CEC

- Support 16 bits PCM 32 KHz, 44.1 KHz, 48KHz for maximum 2 channels audio output

- **Graphic Engine**
  - Copy and paste
  - Geometric operation including mirror, flip and rotation
  - Arithmetic operation including addition, subtraction, color keying, logic operation and alpha blending
  - Support warping function
  - Support anti-alias affine transform
  - Support hardware acceleration for multi-frame processing
- **Cipher**
  - 64-bit DES, 3DES, and AES-128
  - Both encryption and decryption
  - Big and little endian of input data
- **H.264/AVC CODEC**
  - Support encoder BP/MP, level 4.1
  - Support encoder HP, level 4.2
  - Support real-time capability for 1080p30, 720p60, 480p120
  - Support full frame still capture while video recording
  - H.264 high/main profile
  - 1 reference picture for P-frame, 2 reference pictures for B-frame
  - Support video format MP4, AVI, MOV
  - Support bit rate control
  - Automatic frame sync for high frame rate
- **Motion Estimation**
  - [-124.75,+124.75] search range in horizontal component
  - [-28.75, +28.75] search range in vertical component
  - MB mode: 16x16, 16x8, 8x16, 8x8, skip, and direct (B-frame)
- **F/W Audio CODEC**
  - AAC encode / decode (32KHz, 48KHz @ 192kbps)
  - ADPCM encode / decode
  - Noise cancellation for background noise, motor operation, and wind
- **H/W Audio CODEC**
  - stereo 16-bits ADC audio recording
  - stereo 16-bits DAC audio playback

- Programmable ALC / Noise Gate l
- Audio sampling rate : 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48kHz
- Support dual microphone inputs
- On-chip speaker driver / stereo headphone drive

- **JPEG CODEC**
  - Supports Motion JPEG 30fps@1080P30 video clip/playback function
  - Max. pixel clock 120Mpixel / sec
  - Support ISO/IEC 10918-1 baseline JPEG compression/decompression.
  - Still image maximum resolutions will be up to 65536x65536 pixels
  - Support input format: 422, 420, 411, 400, 211
  - JPEG supports downloadable Quantization and Huffman tables
  - Support Exchangeable Image File format (EXIF 2.2.3 and newer)
  - Support MPO file format for 3D image
- **Digital Audio Interface**
  - Support I^2S codec interface
  - Audio clock generator
- **Dual Graphic-based OSD**
  - Support 8-bit palette and ARGB(4565 or 8565) OSD architecture
  - 256 colors simultaneously out of true color at 8-bit palette OSD
  - 8 levels of opacity for 8-bit palette OSD
  - Programmable width & height to meet LCD/TV's resolution exactly
  - Picture in picture function
  - Dedicated 16 face frames for face detection function
- **Storage Memory Controller**
  - Secure Digital card and SDIO
  - Support SD 3.0
  - Support UHS-I: UHS50, UHS104 (Max. freq. 108MHz)
  - Support eMMC and hot boot
  - Support eyeFi for wireless connection
  - Multi-Media card
  - SLC NAND type flash
- **USB**
  - Fully compliant with USB2.0 device/host
  - High speed (480Mbps) supported

- Optionally switchable to be fully compliant with USB 1.1
- Support Control / Isochronous / Interrupt and Bulk transfer
- Support PC camera mode

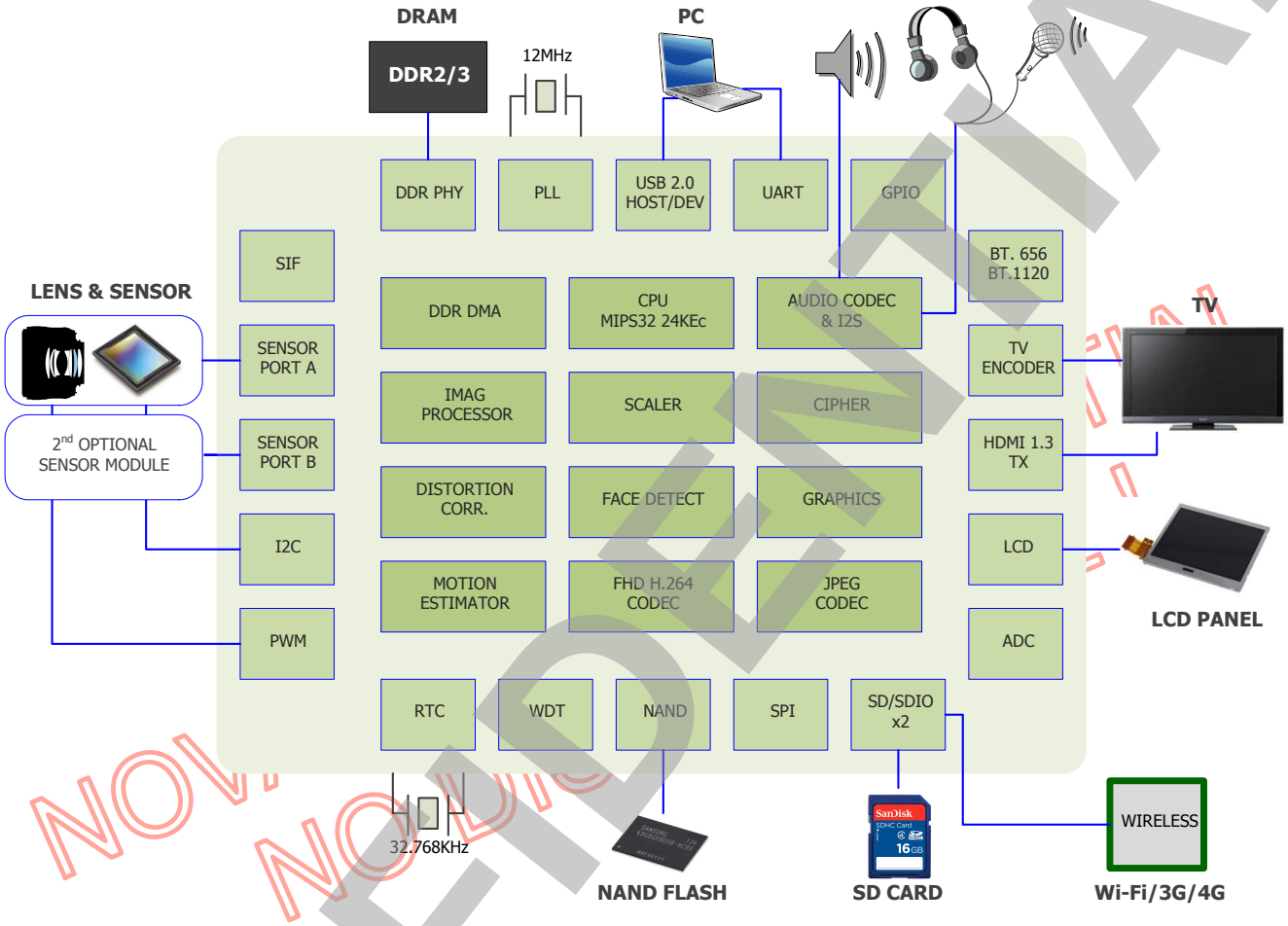
- **Timers**
  - RTC can be powered by separate backup battery and operating from 1.5V to 3.6V
  - Watch dog timer
  - 16 programmable HW timers support resolution up to 3MHz and 32 bits counter
- **Peripheral Interface**
  - Support I^2C interface
  - Support 20 channels PWM including built-in 16 (4 sets) pattern generators for µ-Stepping motor control.
  - Support GPIO and flexible PWM interface with micro-stepping
  - Support programmable 3-wired serial interface
  - Support SPI for gyroscope reading
  - Support UART interface
  - Support 8 channels of 10-bit ADC with touch panel interface (2 channels), the max. sample rate up to 12.5 KHz per channel
- **On-chip Boot Strap Loader**
  - Built-in on-chip mask ROM
  - User program can be stored in NAND-type flash and external static memory is not necessary
  - On-chip mask ROM can be disabled
  - System can boot from SPI flash, NAND flash, memory cards, eMMC and USB
- **Triple Voltage Power Supply**
  - 1.05V core logic voltage
  - 1.8V / 1.5V DDRII/DDRIII SDRAM interface voltage
  - 3.3V I/O interface and analog circuit voltage
- **Package**

  NT96655BG: 305 ball TFBGA, 13x13 mm^2

General Description

NT9665xBG is a high image quality, high performance, power saving and cost effective digital still camera (DSC) and digital video camera (DV) controller with excellent digital still image capturing and video streaming capabilities. It is targeted for the application of VGA to 50M pixel DSC/DV resolutions. It can be easily adapted to many high speed CMOS and conventional CCD image sensors with on chip programmable interface timing approach. The controller provides sophisticated video processing methods with built-in hardware acceleration pipeline. This is essential for achieving high performance for per-shot, shot-to-shot, and continuous shooting pictures. The controller provides flexible mechanism for auto white balance, auto exposure and auto-focusing in order to better tradeoff hardware and software efforts over the performance. Embedded H.264 video CODEC supports video recording up to full-HD 1080p30. The HDMI 1.3 Tx is also equipped for HDTV output. Rich storage interfaces are supported to make it ideal for the storage of still pictures and video streaming data. The USB2.0 high speed interface can upload/download the audio/video data efficiently to/from PC.

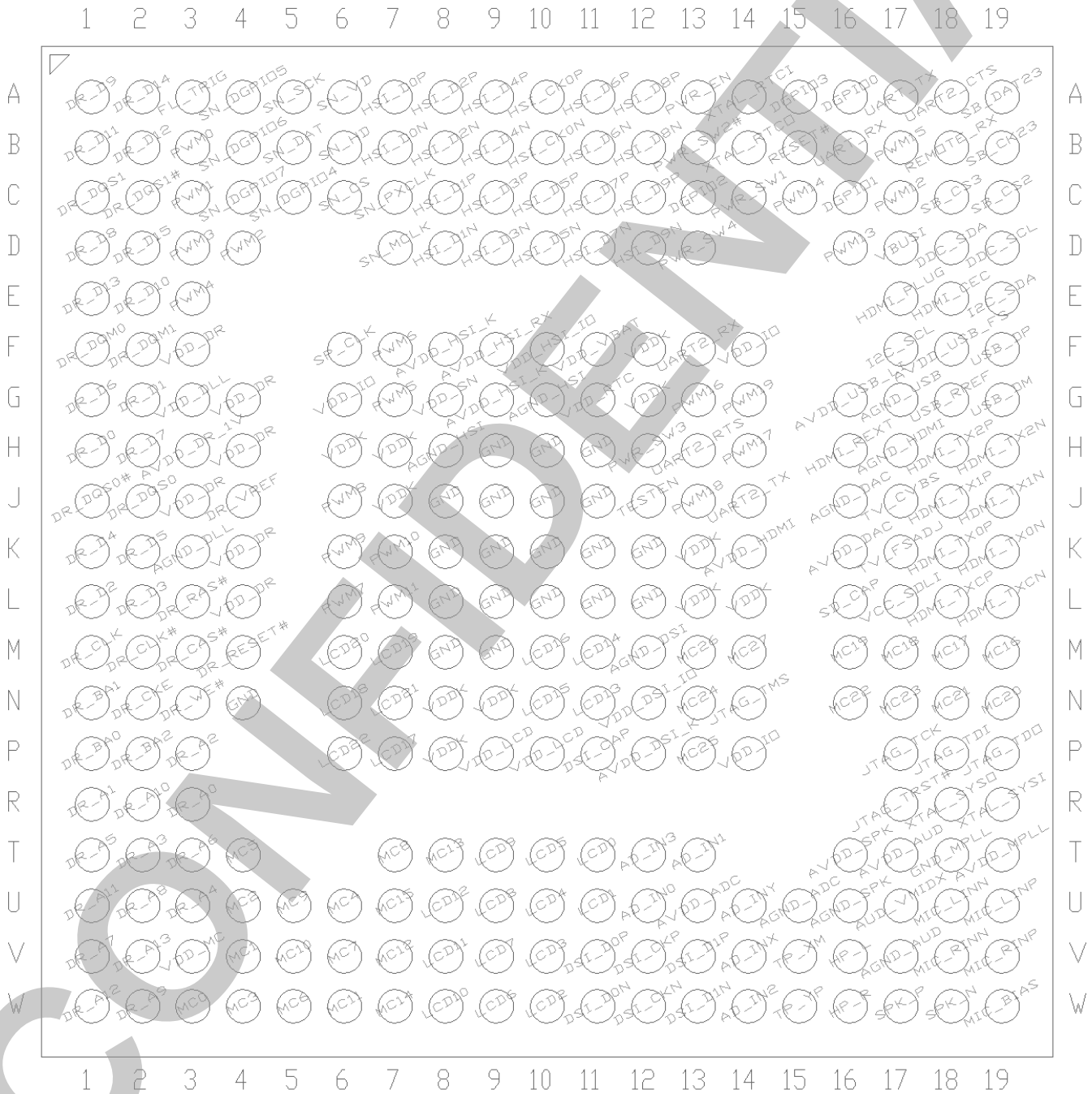
Block Diagram



Pin Configuration

1.

TFBGA-305



Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
A1	DR_D9	E19	I2C_SDA	K11	GND	R3	DR_A0
A2	DR_D14	F1	DR_DQM0	K12	GND	R17	JTAG_TRST#
A3	FL_TRIG	F2	DR_DQM1	K13	VDDK	R18	XTAL_SYSO
A4	SN_DGPIO5	F3	VDD_DR	K14	AVDD_HDMI	R19	XTAL_SYSI
A5	SN_SCK	F6	SP_CLK	K16	AVDD_DAC	T1	DR_A5
A6	SN_VD	F7	PWM6	K17	TV_FSADJ	T2	DR_A3
A7	HSI_D0P	F8	AVDD_HSI_K	K18	HDMI_TX0P	T3	DR_A6
A8	HSI_D2P	F9	AVDD_HSI_RX	K19	HDMI_TX0N	T4	MC5
A9	HSI_D4P	F10	VDD_HSI_IO	L1	DR_D2	T7	MC8
A10	HSI_CK0P	F11	VDD_VBAT	L2	DR_D3	T8	MC13
A11	HSI_D6P	F12	VDDK	L3	DR_RAS#	T9	LCD9
A12	HSI_D8P	F13	UART2_RX	L4	VDD_DR	T10	LCD5
A13	PWR_EN	F14	VDD_IO	L6	PWM7	T11	LCD0
A14	XTAL_RTCI	F17	I2C_SCL	L7	PWM11	T12	AD_IN3
A15	DGPIO3	F18	AVDD_USB_FS	L8	GND	T13	AD_IN1
A16	DGPIO0	F19	USB_DP	L9	GND	T16	AVDD_SPK
A17	UART_TX	G1	DR_D6	L10	GND	T17	AVDD_AUD
A18	UART2_CTS	G2	DR_D1	L11	GND	T18	GND_MPLL
A19	SB_DAT23	G3	AVDD_DLL	L12	GND	T19	AVDD_MPLL
B1	DR_D11	G4	VDD_DR	L13	VDDK	U1	DR_A11
B2	DR_D12	G6	VDD_IO	L14	VDDK	U2	DR_A8
B3	PWM0	G7	PWM5	L16	SD_CAP	U3	DR_A4
B4	SN_DGPIO6	G8	VDD_SN	L17	VDD_SDLI	U4	MC2
B5	SN_DAT	G9	AVDD_HSI_K	L18	HDMI_TXCP	U5	MC9
B6	SN_HD	G10	AGND_HSI	L19	HDMI_TXCN	U6	MC4
B7	HSI_D0N	G11	VDD_RTC	M1	DR_CLK	U7	MC15
B8	HSI_D2N	G12	VDDK	M2	DR_CLK#	U8	LCD12
B9	HSI_D4N	G13	PWM16	M3	DR_CAS#	U9	LCD8
B10	HSI_CK0N	G14	PWM19	M4	DR_RESET#	U10	LCD4
B11	HSI_D6N	G16	AVDD_USB_LI	M6	LCD20	U11	LCD1
B12	HSI_D8N	G17	AGND_USB	M7	LCD19	U12	AD_IN0
B13	PWR_SW2#	G18	USB_RREF	M8	GND	U13	AVDD_ADC
B14	XTAL_RTCO	G19	USB_DM	M9	GND	U14	AD_INY
B15	RESET#	H1	DR_D0	M10	LCD16	U15	AGND_ADC
B16	UART_RX	H2	DR_D7	M11	LCD14	U16	AGND_SPK
B17	PWM15	H3	AVDD_DR_1V	M12	AGND_DSI	U17	AUD_VMIDX
B18	REMOTE_RX	H4	VDD_DR	M13	MC26	U18	MIC_LINN
B19	SB_CK23	H6	VDDK	M14	MC27	U19	MIC_LINP
C1	DR_DQS1	H7	VDDK	M16	MC19	V1	DR_A7
C2	DR_DQS1#	H8	AGND_HSI	M17	MC18	V2	DR_A13
C3	PWM1	H9	GND	M18	MC17	V3	VDD_MC
C4	SN_DGPIO7	H10	GND	M19	MC16	V4	MC1
C5	SN_DGPIO4	H11	GND	N1	DR_BA1	V5	MC10
C6	SN_CS	H12	PWR_SW3	N2	DR_CKE	V6	MC7
C7	SN_PXCLK	H13	UART2_RTS	N3	DR_WE#	V7	MC12
C8	HSI_D1P	H14	PWM17	N4	GND	V8	LCD11
C9	HSI_D3P	H16	HDMI_REXT	N6	LCD18	V9	LCD7
C10	HSI_D5P	H17	AGND_HDMI	N7	LCD21	V10	LCD3
C11	HSI_D7P	H18	HDMI_TX2P	N8	VDDK	V11	DSI_D0P
C12	HSI_D9P	H19	HDMI_TX2N	N9	VDDK	V12	DSI_CKP
C13	DGPIO2	J1	DR_DQS0#	N10	LCD15	V13	DSI_D1P
C14	PWR_SW1	J2	DR_DQS0	N11	LCD13	V14	AD_INX
C15	PWM14	J3	VDD_DR	N12	VDD_DSI_IO	V15	TP_XM
C16	DGPIO1	J4	DR_VREF	N13	MC24	V16	HP_L
C17	PWM12	J6	PWM8	N14	JTAG_TMS	V17	AGND_AUD
C18	SB_CS3	J7	VDDK	N16	MC22	V18	MIC_RINN
C19	SB_CS2	J8	GND	N17	MC23	V19	MIC_RINP
D1	DR_D8	J9	GND	N18	MC21	W1	DR_A12
D2	DR_D15	J10	GND	N19	MC20	W2	DR_A9

D3	PWM3	J11	GND	P1	DR_BA0	W3	MC0
D4	PWM2	J12	TESTEN	P2	DR_BA2	W4	MC3
D7	SN_MCLK	J13	PWM18	P3	DR_A2	W5	MC6
D8	HSI_D1N	J14	UART2_TX	P6	LCD22	W6	MC11
D9	HSI_D3N	J16	AGND_DAC	P7	LCD17	W7	MC14
D10	HSI_D5N	J17	TV_CVBS	P8	VDDK	W8	LCD10
D11	HSI_D7N	J18	HDMI_TX1P	P9	VDD_LCD	W9	LCD6
D12	HSI_D9N	J19	HDMI_TX1N	P10	VDD_LCD	W10	LCD2
D13	PWR_SW4	K1	DR_D4	P11	DSI_CAP	W11	DSI_D0N
D16	PWM13	K2	DR_D5	P12	AVDD_DSI_K	W12	DSI_CKN
D17	VBUSI	K3	AGND_DLL	P13	MC25	W13	DSI_D1N
D18	DDC_SDA	K4	VDD_DR	P14	VDD_IO	W14	AD_IN2
D19	DDC_SCL	K6	PWM9	P17	JTAG_TCK	W15	TP_YP
E1	DR_D13	K7	PWM10	P18	JTAG_TDI	W16	HP_R
E2	DR_D10	K8	GND	P19	JTAG_TDO	W17	SPK_P
E3	PWM4	K9	GND	R1	DR_A1	W18	SPK_N
E17	HDMI_PLUG	K10	GND	R2	DR_A10	W19	MIC_BIAS
E18	HDMI_CEC						

Pin Descriptions

I = input port with Schmitt trigger

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking and Schmitt input

mvI/O = multi voltage bi-direction port with Schmitt input

HSI = high speed serial interface with multi voltage input port

I/Osw = bi-directional port with strong driving/sinking and wide Schmitt input range

I/Ow = bi-directional port with wide Schmitt input range

I/Os = bi-directional port with strong driving/sinking

I/Os2 = bi-directional port with strong driving/sinking

I/Oss = bi-directional port with strong driving/sinking

I/Oz = bi-directional port with large pull/down resistor

I/O_{5VT} = bi-directional port with normal driving/sinking and Schmitt input

OD = open drain output with normal sinking

I/OD = bi-directional port, open drain output

LVD = low voltage detect function pin

p/u = internal pull-up

p/d = internal pull-down

AI = analog input port

AI_{5VT} = analog 5V tolerant input port

AO = analog output port

AI/O = analog bi-directional port

H = output high

L = output low

P = power or ground

Note: * means this pin has interrupted function.

1. NT96655BG 305 pins

Total: 305 pins

Alternative GPIO: 133 pins

1.1. System interface (9)

Pin No.	Name	Type	Reset	Descriptions
R19	XTAL_SYSI	AI	-	Crystal input for system oscillator. (12MHz)
R18	XTAL_SYSO	AO	-	Output for system oscillator.
B15	RESET#	LVD	p/u	System Reset. Connect a capacitor to ground for reset time control.
J12	TESTEN	I	I p/d	Test mode enable. Keep low for normal operation.
R17	JTAG_TRST# / P_GPIO[31]*	IO	I p/u	JTAG test logic reset(active low).
N14	JTAG_TMS / P_GPIO[32]*	IO	I p/d	JTAG test mode select.
P17	JTAG_TCK / P_GPIO[33]*	IO	I p/d	JTAG test clock input.
P18	JTAG_TDI / P_GPIO[34]*	IO	I p/d	JTAG test data input.
P19	JTAG_TDO / P_GPIO[35]*	IO	I p/d	JTAG test data output.

1.2. RTC & Power Button Controller (7)

Pin No.	Name	Type	Default	Descriptions
A14	XTAL_RTCI	AI	-	Crystal input for real time clock oscillator. (32.768KHz).
B14	XTAL_RTCO	AO	-	Output for real time clock oscillator.
C14	PWR_SW1*	AI	I p/d	Power on/off signal input. (ON/OFF switch use)
B13	PWR_SW2*#	AI	I p/u	Power on/off signal input. (falling edge trigger)
H12	PWR_SW3	I_{5VTZ}	I p/d	Power on/off signal input. (5V tolerance Input for VBUSI use)
D13	PWR_SW4	AI	I p/d	Power on/off signal input. (Bettery in use)
A13	PWR_EN	AO	-	Power enable signal output.

* PWR_SW can trigger interrupt (share RTC interrupt). If this pin isn't used, Novatek recommends connecting this pin to GND.

1.3. DRAM interface (47)

Pin No.	Name	Type	Reset	Descriptions
M4	DR_RESET#	O	-	Reset signal output for DDR3 DRAM.
M1	DR_CLK	O	-	DRAM differential clock output.
M2	DR_CLK#	O	-	
N2	DR_CKE	O	-	DRAM clock enable.

M3	DR_CAS#	O	-	DRAM control signals
L3	DR_RAS#			
N3	DR_WE#			
J4	DR_VREF	AI	-	DRAM reference voltage input.
P1	DR_BA0	O	-	DRAM bank select.
N1	DR_BA1			
P2	DR_BA2			
R3	DR_A0	O	-	DRAM address bus.
R1	DR_A1			
P3	DR_A2			
T2	DR_A3			
U3	DR_A4			
T1	DR_A5			
T3	DR_A6			
V1	DR_A7			
U2	DR_A8			
W2	DR_A9			
R2	DR_A10			
U1	DR_A11			
W1	DR_A12			
V2	DR_A13			
F1	DR_DQM0	O	-	DRAM data mask: DQM0 corresponds to DQ0-DQ7 and DQM1 corresponds to DQ8-DQ15.
F2	DR_DQM1			
J2	DR_DQS0	I/O	-	DRAM data strobe. DQS0 corresponds to DQ0-DQ7 and DQS1 corresponds to DQ8-DQ15.
J1	DR_DQS0#			
C1	DR_DQS1			
C2	DR_DQS1#			
H1	DR_D0	I/O	-	DRAM data bus input/output, lower byte. (Each bits of lower byte may be permuted to make routing simpler).
G2	DR_D1			
L1	DR_D2			
L2	DR_D3			
K1	DR_D4			
K2	DR_D5			
G1	DR_D6			
H2	DR_D7			
D1	DR_D8	I/O	-	DRAM data bus input/output, upper byte. (Each bits of upper byte may be permuted to make routing simpler)
A1	DR_D9			
E2	DR_D10			
B1	DR_D11			
B2	DR_D12			
E1	DR_D13			
A2	DR_D14			
D2	DR_D15			

1.4. Sensor interface (33)

Pin No.	Name	Type	Reset	Descriptions
B7	HSI_D0N / S_GPI[0]	HSI	I p/d	High speed differential sensor interface and parallel interface. (when sensor interface is configured as high speed differential sensor interface, the clock lane should be a dedicated differential lane. And each data lanes may be permuted in established group, refer to below table)
A7	HSI_D0P / S_GPI[1]			
D8	HSI_D1N / S_GPI[2]			
C8	HSI_D1P / S_GPI[3]			
B8	HSI_D2N / S_GPI[4]			
A8	HSI_D2P / S_GPI[5]			
D9	HSI_D3N / S_GPI[6]			
C9	HSI_D3P / S_GPI[7]			
B9	HSI_D4N / S_GPI[8]			
A9	HSI_D4P / S_GPI[9]			
B10	HSI_CK0N / S_GPI[10]			
A10	HSI_CK0P / S_GPI[11]			
D10	HSI_D5N / S_GPI[12]			
C10	HSI_D5P / S_GPI[13]			
B11	HSI_D6N / S_GPI[14]			
A11	HSI_D6P / S_GPI[15]			
D11	HSI_D7N / S_GPI[16]			
C11	HSI_D7P / S_GPI[17]			
B12	HSI_D8N / S_GPI[18]			
A12	HSI_D8P / S_GPI[19]			
D12	HSI_D9N / S_GPI[20]			
C12	HSI_D9P / S_GPI[21]			

D7	SN_MCLK / S_GPIO[24]	mvI/Os	I p/d	Programmable Clock output for sensor
C7	SN_PXCLK / S_GPIO[25]	mvI/Os	I p/d	Sensor Pixel Clock Input
A6	SN_VD / S_GPIO[26]	mvI/O	I p/d	Sensor Vertical Sync input / output
B6	SN_HD / S_GPIO[27]	mvI/O	I p/d	Sensor Horizontal Sync input / output
C6	SN_CS / SPI3_CS / P_GPIO[56]	mvIOs	I p/u	General serial interface 0 or Serial Peripheral Interface 3 Chip Select
A5	SN_SCK / SPI3_CLK / I2C_SCL / P_GPIO[57]	mvIOD	I p/u	General serial interface 0 or Serial Peripheral Interface 3 clock output. I2C-BUS clock output(Open Drain IO structure)
B5	SN_DAT / SPI3_DO / I2C_SDA / P_GPIO[58]	mvIOD	I p/u	General serial interface 0 or Serial Peripheral Interface 3 data output. I2C-BUS data input / output(Open Drain IO structure)
C5	SN_DGPIO4*	mvIO	I p/d	General purpose Input / output
A4	SN_DGPIO5*	mvIO	I p/d	General purpose Input / output
B4	SPI3_DI / SN_FLASH / SN_DGPIO6*	mvIO	I p/d	Serial Peripheral Interface 3 data input. Flash Signal input from sensor
C4	SN_SHUTTER / SN_DGPIO7*	mvIO	I p/d	Shutter signal input from sensor

Note*: The pin can trigger interrupt.

Note1 : The input voltage of HSI corresponds to GVDD_SN.

Note2 : The mvI/O voltage of Sensor interface corresponds to VDD_SN.

Name	LVDS		HiSPi		MIPI CSI		Parallel (12 bits)		CCIR601 (16 bits)		CCIR601 (8 bits)	
S_GPI[0]	HSI_D0N	I	SLVS_D0N	I	CSI_D0N	I	SN_D0	I				
S_GPI[1]	HSI_D0P	I	SLVS_D0P	I	CSI_D0P	I	SN_D1	I				
S_GPI[2]	HSI_D1N	I	SLVS_D1N	I	CSI_D1N	I	SN_D2	I				
S_GPI[3]	HSI_D1P	I	SLVS_D1P	I	CSI_D1P	I	SN_D3	I				
S_GPI[4]	HSI_D2N	I	SLVS_D2N	I	CSI_D2N	I	SN_D4	I	CCIR_Y0	I		
S_GPI[5]	HSI_D2P	I	SLVS_D2P	I	CSI_D2P	I	SN_D5	I	CCIR_Y1	I		
S_GPI[6]	HSI_D3N	I	SLVS_D3N	I	CSI_D3N	I	SN_D6	I	CCIR_Y2	I		
S_GPI[7]	HSI_D3P	I	SLVS_D3P	I	CSI_D3P	I	SN_D7	I	CCIR_Y3	I		
S_GPI[8]	HSI_D4N	I					SN_D8	I	CCIR_Y4	I		
S_GPI[9]	HSI_D4P	I					SN_D9	I	CCIR_Y5	I		
S_GPI[10]	**HSI_CK0N**	**I**	**SLVS_CKN**	**I**	**CSI_CKN**	I	SN_D10	I	CCIR_Y6	I		
S_GPI[11]	**HSI_CK0P**	**I**	**SLVS_CKP**	**I**	**CSI_CKP**	I	SN_D11	I	CCIR_Y7	I		
S_GPI[12]	HSI_D5N	I							CCIR_C0	I	CCIR_YC0	I
S_GPI[13]	HSI_D5P	I							CCIR_C1	I	CCIR_YC1	I
S_GPI[14]	HSI_D6N	I							CCIR_C2	I	CCIR_YC2	I
S_GPI[15]	HSI_D6P	I							CCIR_C3	I	CCIR_YC3	I
S_GPI[16]	HSI_D7N	I							CCIR_C4	I	CCIR_YC4	I
S_GPI[17]	HSI_D7P	I							CCIR_C5	I	CCIR_YC5	I
S_GPI[18]	HSI_D8N	I							CCIR_C6	I	CCIR_YC6	I

S_GPI[19]	HSI_D8P	I							CCIR_C7	I	CCIR_YC7	I
S_GPI[20]	HSI_D9N	I							CCIR_VD	I	CCIR_VD	I
S_GPI[21]	HSI_D9P	I							CCIR_HD	I	CCIR_HD	I
S_GPI[24]	SN_MCLK	O	SN_MCLK	O	SN_MCLK	O	SN_MCLK	O				
S_GPI[25]	SN_PXCLK	I					SN_PXCLK	I				
S_GPI[26]	SN_VD	I/O					SN_VD	I/O				
S_GPI[27]	SN_HD	I/O					SN_HD	I/O				
SN_DGPIO4									CCIR_CLK	I	CCIR_CLK	I

1.5. Memory Card interface (29)

Pin No.	Name	Type	Reset	Descriptions
L16	SD_CAP	P	-	Internal Supply Voltage decoupling for SDIO interface. (3.3/1.8V switchable, default 3.3V)
W3	MC0 / C_GPIO[0]	mvI/O	I p/u	Memory Card interface(see below table)
V4	MC1 / C_GPIO[1]	mvI/O	I p/u	
U4	MC2 / C_GPIO[2]	mvI/O	I p/u	
W4	MC3 / C_GPIO[3]	mvI/O	I p/u	
U6	MC4 / C_GPIO[4]	mvI/O	I p/u	
T4	MC5 / C_GPIO[5]	mvI/O	I p/u	
W5	MC6 / C_GPIO[6]	mvI/O	I p/u	
V6	MC7 / C_GPIO[7]	mvI/O	I p/u	
T7	MC8 / C_GPIO[8]	mvI/O	I p/u	
U5	MC9 / C_GPIO[9]	mvI/O	I p/u	
V5	MC10 / C_GPIO[10]	mvI/O	I p/u	
W6	MC11 / C_GPIO[11]	mvI/O	I p/u	
V7	MC12 / C_GPIO[12]	mvI/O	I p/d	
T8	MC13 / C_GPIO[13]	mvI/O	I p/d	
W7	MC14 / C_GPIO[14]	mvI/O	I p/d	
U7	MC15 / C_GPIO[15]*	mvI/O	I p/u	
M19	MC16 / C_GPIO[16]	I/Os	I p/d	
M18	MC17 /	I/O	I p/u	

	C_GPIO[17]		
M17	MC18 / C_GPIO[18]	I/O	I p/u
M16	MC19 / C_GPIO[19]	I/O	I p/u
N19	MC20 / C_GPIO[20]	I/O	I p/u
N18	MC21 / C_GPIO[21]*	I/O	I p/u
N16	MC22 / C_GPIO[22]*	I/Os	I p/d
N17	MC23 / C_GPIO[23]*	I/O	I p/u
N13	MC24 / C_GPIO[24]*	I/O	I p/u
P13	MC25 / C_GPIO[25]*	I/O	I p/u
M13	MC26 / C_GPIO[26]*	I/O	I p/u
M14	MC27 / C_GPIO[27]*	I/O	I p/u

Note*: The pin can trigger interrupt.

Note1: The mvI/O voltage of MC0~15 corresponds to VDD_MC.

Note2: The IO voltage of MC16~21 corresponds to SD_CAP, it could be switched between 3.3/1.8V by the register.

Memory card interface pinmux table

Name	NAND Flash		SD/MMC/eMMC		SD		SPI flash		SPI		I2S	
MC0	NAND_D0	I/O	eMMC_D0	I/O			SPI_DO/D0	I/O				
MC1	NAND_D1	I/O	eMMC_D1	I/O			SPI_DI/D1	I/O				
MC2	NAND_D2	I/O	eMMC_D2	I/O			SPI_CLK	O				
MC3	NAND_D3	I/O	eMMC_D3	I/O			SPI_WP/D2	I/O				
MC4	NAND_D4	I/O	eMMC_D4	I/O			SPI_HOLD/D3	I/O				
MC5	NAND_D5	I/O	eMMC_D5	I/O								
MC6	NAND_D6	I/O	eMMC_D6	I/O								
MC7	NAND_D7	I/O	eMMC_D7	I/O								
MC8	NAND_CS0#	O					SPI_CS#	O				
MC9	NAND_CS1#	O	eMMC_CLK	O								
MC10	NAND_WE#	O										
MC11	NAND_RE#	O	eMMC_CMD	I/O								
MC12	NAND_CLE	O										
MC13	NAND_ALE	O										
MC14	NAND_WP#	O										
MC15	NAND_RDY	I										
MC16					SD_CLK	O						
MC17					SD_CMD	I/O						
MC18					SD_D0	I/O						
MC19					SD_D1	I/O						
MC20					SD_D2	I/O						
MC21					SD_D3	I/O						

MC22			SDIO_CLK	O					SPI_CLK	O	I2S_MCLK	O
MC23			SDIO_CMD	I/O					SPI_CS#	O	I2S_BCLK	I/O
MC24			SDIO_D0	I/O					SPI_DI	I	I2S_SYNC	O
MC25			SDIO_D1	I/O					SPI_DO	O	I2S_DO	O
MC26			SDIO_D2	I/O							I2S_DI	I
MC27			SDIO_D3	I/O								

1.6. LCD interface (23)

Pin No.	Name	Type	Reset	Descriptions
T11	LCD0 / L_GPIO[0] / BS0	mvI/O	I p/d	LCD Signal Bus / BS2..0 : BOOT_SRC The boot source setting description: 0x0: NAND with RS ECC 0x1: Boot card (Select by BOOT_CARD) 0x2: eMMC (SDIO2_2) 0x3: USB full speed 0x4: SPI flash 0x5: USB high speed 0x6: NAND with Hamming ECC 0x7: BMC (SPI)
U11	LCD1 / L_GPIO[1] / BS1	mvI/O	I p/d	
W10	LCD2 / L_GPIO[2] / BS2	mvI/O	I p/d	
V10	LCD3 / L_GPIO[3] / BS3	mvI/O	I p/d	LCD Signal Bus / BS3 : Reserved for F/W(MPLL control flow) BS6..3 is for IC debugging setting. Please keep low at reset signal rising edge.
U10	LCD4 / L_GPIO[4] / BS4	mvI/O	I p/d	LCD Signal Bus / BS4 : BOOT_CARD Boot card select 0: SD 1: SDIO (SDIO2_2)
T10	LCD5 / L_GPIO[5] / BS5	mvI/O	I p/d	LCD Signal Bus / BS5 : EJTAG_SEL EJTAG select 0: GPIO (TRST, TMS, TCK, TDI, TDO are GPIO) 1: EJTAG
W9	LCD6 / L_GPIO[6] / BS6	mvI/O	I p/d	LCD Signal Bus / BS6 : MPLL_CLK_SEL Select clock source of PLL. 0: APLL clock output (From APLL clock) 1: Bypass APLL (From external clock)
V9	LCD7 / L_GPIO[7] / BS7	mvI/O	I p/d	LCD Signal Bus / BS7 : EMMC_BUSWIDTH eMMC boot bus width 0: 4 bits data bus 1: 8 bits data bus
U9	LCD8 / L_GPIO[8]	mvI/O	I p/d	LCD Signal Bus
T9	LCD9 / L_GPIO[9]	mvI/O	I p/d	
W8	LCD10 / L_GPIO[10]	mvI/O	I p/d	
V8	LCD11 / L_GPIO[11]	mvI/O	I p/d	

U8	LCD12 / L_GPIO[12] / BS8	mvI/O	I p/d	LCD Signal Bus / BS8 : EMMC_BOOTMODE eMMC boot mode 0: single rate + backward timing 1: dual rate + high speed timing
N11	LCD13 / L_GPIO[13] / BS9	mvI/O	I p/d	LCD Signal Bus/ BS9 : EMMC_DDR_DATA_ORDER eMMC DDR data order 0: Odd byte (1st byte) first 1: Even byte (2nd byte) first
M11	LCD14 / L_GPIO[14] / BS10	mvI/O	I p/d	LCD Signal Bus/ BS10 : MIPS_DEBUG_MODE_SEL Enable NT9665x enters CPU debug mode. Internal CPU state will be outputted to debug port on storage interface (MC[18..0]) 0: Normal mode 1: CPU debug mode BS10 for IC debugging setting. Please keep low at reset signal rising edge.
N10	LCD15/ L_GPIO[15]	mvI/O	I p/d	LCD Signal Bus
M10	LCD16 / L_GPIO[16]	mvI/O	I p/d	
P7	LCD17 / L_GPIO[17]	mvI/O	I p/d	
N6	LCD18 / L_GPIO[18]*	mvI/O	I p/d	
M7	LCD19 / L_GPIO[19]*	mvI/O	I p/d	
M6	LCD20 / L_GPIO[20]	mvI/O	I p/d	
N7	LCD21 / L_GPIO[21]	mvI/O	I p/d	
P6	LCD22 / L_GPIO[22]	mvI/O	I p/d	

Note1: The mvI/O voltage of LCD interface corresponds to VDD_LCD.

LCD interface pinmux table

Name	CCIR(8 bits)		Serial RGB		CCIR(16 bits)		i80/M68		CCIR & RGB (secondary panel)		MPU Serial (secondary panel)	
LCD0	CCIR_YC0	O	RGB_D0	O	CCIR_Y0	O	MPU_D0	I/O				
LCD1	CCIR_YC1	O	RGB_D1	O	CCIR_Y1	O	MPU_D1	I/O				
LCD2	CCIR_YC2	O	RGB_D2	O	CCIR_Y2	O	MPU_D2	I/O				
LCD3	CCIR_YC3	O	RGB_D3	O	CCIR_Y3	O	MPU_D3	I/O				
LCD4	CCIR_YC4	O	RGB_D4	O	CCIR_Y4	O	MPU_D4	I/O				
LCD5	CCIR_YC5	O	RGB_D5	O	CCIR_Y5	O	MPU_D5	I/O				
LCD6	CCIR_YC6	O	RGB_D6	O	CCIR_Y6	O	MPU_D6	I/O				
LCD7	CCIR_YC7	O	RGB_D7	O	CCIR_Y7	O	MPU_D7	I/O				
LCD8	CCIR_CLK	O	RGB_CLK	O	CCIR_CLK	O	MPU_TE	I				
LCD9	CCIR_VD	O	RGB_VD	O	CCIR_VD	O	MPU_CS#	O				
LCD10	CCIR_HD	O	RGB_HD	O	CCIR_HD	O	MPU_RS	O				
LCD11					CCIR_DE	O	MPU_WR#	O				

LCD12					CCIR_C0	O	MPU_RD#	O	RGB_YC0	O			
LCD13					CCIR_C1	O	MPU_D8	I/O	RGB_YC1	O	MPU_SDO	O	
LCD14					CCIR_C2	O	MPU_D9	I/O	RGB_YC2	O	MPU_SDI	I	
LCD15					CCIR_C3	O	MPU_D10	I/O	RGB_YC3	O	MPU_CS	O	
LCD16					CCIR_C4	O	MPU_D11	I/O	RGB_YC4	O	MPU_RS	O	
LCD17					CCIR_C5	O	MPU_D12	I/O	RGB_YC5	O	MPU_CLK	O	
LCD18					CCIR_C6	O	MPU_D13	I/O	RGB_YC6	O	MPU_SDIO	I/O	
LCD19					CCIR_C7	O	MPU_D14	I/O	RGB_YC7	O	MI_TE	I	
LCD20	**LCD_CS**	O					MPU_D15	I/O	RGB_CLK	O			
LCD21	**LCD_CLK**	O					MPU_D16	I/O	RGB_VD	O			
LCD22	**LCD_DAT**	O					MPU_D17	I/O	RGB_HD	O			

1.7. PWM (20)

Pin No.	Name	Type	Reset	Descriptions
B3	PWM0 / ME_SHUT0 / P_GPIO[36]	I/O	I p/d	PWM output pin. Mechanical Shutter control output. Micro-stepping control module 1.
C3	PWM1 / ME_SHUT1 / P_GPIO[37]	I/O	I p/d	
D4	PWM2 / P_GPIO[38]	I/O	I p/d	
D3	PWM3 / P_GPIO[39]	I/O	I p/d	
E3	PWM4 / P_GPIO[40]	I/O	I p/d	PWM output pin. Micro-stepping control module 2. Serial Peripheral Interface
G7	PWM5 / P_GPIO[41]	I/O	I p/d	
F7	PWM6 / P_GPIO[42]	I/O	I p/d	
L6	PWM7 / P_GPIO[43]	I/O	I p/d	
J6	PWM8 / P_GPIO[44]	I/O	I p/d	PWM output pin. Micro-stepping control module 3.
K6	PWM9 / P_GPIO[45]	I/O	I p/d	
K7	PWM10 / P_GPIO[46]	I/O	I p/d	
L7	PWM11 / P_GPIO[47]	I/O	I p/d	
C17	PWM12 / P_GPIO[48]	I/O	I p/d	PWM output pin. Micro-stepping control module 4.
D16	PWM13 / P_GPIO[49]	I/O	I p/d	
C15	PWM14 / P_GPIO[50]	I/O	I p/d	
B17	PWM15 / P_GPIO[51]	I/O	I p/d	
G13	PWM16 /	I/O	I p/d	PWM output pin.

	ME_SHUT0 / P_GPIO[52]			Mechanical Shutter control output.
H14	PWM17 / ME_SHUT1 / P_GPIO[53]	I/O	I p/d	
J13	PWM18 / P_GPIO[54]*	I/O	I p/d	PWM output pin.
G14	PWM19 / P_GPIO[55]*	I/O	I p/d	PWM output pin.

Name	PWM		M-shutter		u-stepping		SPI					
PWM0	PWM0	O	ME_SHUT0	O	uSTP1_A	O						
PWM1	PWM1	O	ME_SHUT1	O	uSTP1_B	O						
PWM2	PWM2	O			uSTP1_C	O						
PWM3	PWM3	O			uSTP1_D	O						
PWM4	PWM4	O			uSTP2_A	O	SPI3_CLK	O				
PWM5	PWM5	O			uSTP2_B	O	SPI3_CS#	O				
PWM6	PWM6	O			uSTP2_C	O	SPI3_DO	O				
PWM7	PWM7	O			uSTP2_D	O	SPI3_DI	O				
PWM8	PWM8	O			uSTP3_A	O						
PWM9	PWM9	O			uSTP3_B	O						
PWM10	PWM10	O			uSTP3_C	O						
PWM11	PWM11	O			uSTP3_D	O						
PWM12	PWM12	O			uSTP4_A	O						
PWM13	PWM13	O			uSTP4_B	O						
PWM14	PWM14	O			uSTP4_C	O						
PWM15	PWM15	O			uSTP4_D	O						
PWM16	PWM16	O	ME_SHUT0	O								
PWM17	PWM17	O	ME_SHUT1	O								
PWM18	PWM18	O										
PWM19	PWM19	O										

1.8. Peripheral I/O (19)

Pin No.	Name	Type	Reset	Descriptions
E19	I2C_SDA / P_GPIO[0]*	I/OD	I p/u	I2C-BUS clock output(Open Drain IO structure)
F17	I2C_SCL / P_GPIO[1]*	I/OD	I p/u	I2C-BUS data input / output(Open Drain IO structure)
C19	SB_CS2 / SPI3_CS / P_GPIO[7]*	I/O	I p/u	Serial Interface Chip Select 2 Serial Peripheral Interface 3 chip select output
C18	SB_CS3 / SPI3_DI / P_GPIO[8]*	I/O	I p/u	Serial Interface Chip Select 3 Serial Peripheral Interface 3 data input
B19	SB_CK23 / SPI3_CLK / P_GPIO[9]*	I/O	I p/d	Serial Interface Clock 2 & 3 Serial Peripheral Interface 3 clock output
A19	SB_DAT23 / SPI3_DO /	I/O	I p/d	Serial Interface Data 2 & 3 Serial Peripheral Interface 3 data output

	P_GPIO[10]*			
A17	UART_TX / P_GPIO[15]	I/O	O	UART Transmit
B16	UART_RX / P_GPIO[16]*	I/O	I p/u	UART Receive
J14	UART2_TX / SPI2_CS / P_GPIO[17]*	I/O	I p/u	UART2 Transmit Serial Peripheral Interface 2 chip select output
F13	UART2_RX / SPI2_CLK / P_GPIO[18]*	I/O	I p/u	UART2 Receive Serial Peripheral Interface 2 clock output
H13	UART2_RTS / SPI2_DO / P_GPIO[19]*	I/O	I p/u	UART2 Request To Send Serial Peripheral Interface 2 data output
A18	UART2_CTS / SPI2_DI / P_GPIO[20]*	I/O	I p/u	UART2 Clear To Send Serial Peripheral Interface 2 data input
B18	REMOTE_RX / PICNT3 / P_GPIO[25]*	I/Os2	I p/u	Infrared Remote-control Received Data Pulse Counter 3 input
A3	FL_TRIG / S_GPIO[28]	I/Os	I p/d	Flash Light Trigger Control
F6	SP_CLK / PICNT4 / S_GPIO[29]*	I/Oss	I p/d	Clock Output for Micro-stepping Motor Control Pulse Counter 4 input
A16	PICNT1 / DGPIO0*	I/Osw	I p/d	Pulse Counter 1 input
C16	PICNT2 / DGPIO1*	I/Osw	I p/d	Pulse Counter 2 input
C13	SD_CD# / DGPIO2*	I/Osw	I p/u	Card Detect input pin
A15	SD_WP# / DGPIO3*	I/Osw	I p/u	Write protect input pin

1.9. ADC interface (8)

Pin No.	Name	Type	Reset	Descriptions
U12	AD_IN0	AI	-	General ADC 0 Input with buffer.
T13	AD_IN1*	AI	-	General ADC 1 Input with configurable trigger function
W14	AD_IN2*	AI	-	General ADC 2 Input with configurable trigger function
T12	AD_IN3	AI	-	General ADC 3 Input with buffer.
V14	AD_INX	AI	-	General ADC X Input and Touch Panel Control Interface
U14	AD_INY	AI	-	General ADC Y Input and Touch Panel Control Interface
W15	TP_YP	AI	-	Touch Panel Control Interface
V15	TP_XM	AI	-	Touch Panel Control Interface

1.10. Audio Codec(10)

Pin No.	Name	Type	Reset	Descriptions
W19	MIC_BIAS	AO	-	Microphone working bias output.
V19	MIC_RINP	AI	-	Right channel microphone differential input positive side.
V18	MIC_RINN	AI	-	Right channel microphone differential input negative side.
U19	MIC_LINP	AI	-	Left channel microphone differential input positive side.
U18	MIC_LINN	AI	-	Left channel microphone differential input negative side.
U17	VMIDX	AO	-	Decoupling for audio codec reference voltage. Connect 4.7uF capacitor to ground.
W16	HP_R	AO	-	Right channel headphone output. (or Line out)
V16	HP_L	AO	-	Left channel headphone output. (or Line out)
W17	SPK_P	AO	-	Speaker Output of Right Channel
W18	SPK_N	AO	-	Speaker Output of Left Channel

1.11. TV interface (2)

Pin No.	Name	Type	Reset	Descriptions
J17	TV_CVBS	AO	-	Video Data Output Composite video output.
K17	TV_FSADJ	AI	-	Full Screen Adjust Pin TV DAC Full-scale adjust control pin. A 430 Ω/1% resistor connected between this pin and GND controls the full-scale output current on the TV_CVBS output.

1.12. MIPI DSI (7)

Pin No.	Name	Type	Reset	Descriptions
P11	DSI_CAP	P	-	Internal Supply Voltage decoupling for DSI LP mode circuit.
V12	DSI_CKP	AO	-	MIPI DSI differential clock lane output
W12	DSI_CKN	AO	-	
V11	DSI_D0P	AO	-	MIPI DSI differential data lane input / output
W11	DSI_D0N	AO	-	
V13	DSI_D1P	AO	-	
W13	DSI_D1N	AO	-	

1.13. HDMI (13)

Pin No.	Name	Type	Reset	Descriptions
L18	HDMI_TXCP	AO	-	TMDS Low Voltage Differential Signal Output Clock
L19	HDMI_TXCN			
K18	HDMI_TX0P	AO	-	TMDS Low Voltage Differential Signal Output Data
K19	HDMI_TX0N			
J18	HDMI_TX1P			
J19	HDMI_TX1N			
H18	HDMI_TX2P			

H19	HDMI_TX2N			
H16	HDMI_REXT	AI	-	Voltage Swing Adjust. Connect 1.2KΩ/1% resistor to HDMI GND
E18	HDMI_CEC / P_GPIO[27]*	I/O_{5VT}	I p/u	Consumer Electronics Control. CEC is 5V tolerance input.
D18	DDC_SDA / P_GPIO[28]	I/OD_{5VT}	I p/u	Display Data Channel SDA. DDCSDA is 5V tolerance input.
D19	DDC_SCL / P_GPIO[29]	I/OD_{5VT}	I p/u	Display Data Channel SCL. DDCSCL is 5V tolerance input.
E17	HDMI_PLUG / P_GPIO[30]*	I/O_{5VT}	I p/d	Hot Plug Detect. HOTPLUG is 5V tolerance input.

1.14. USB device interface (4)

Pin No.	Name	Type	Reset	Descriptions
D17	VBUSI*	I_{5VTZ}	I p/d	USB V_{BUS} Input. This pin is 5V tolerance input
F19	USB_DP	AI/O	-	USB FS/HS Differential Data Plus (D+)
G19	USB_DM	AI/O	-	USB FS/HS Differential Data Minus (D-)
G18	USB_RREF	AI	-	USB reference resistor. Connect 12KΩ/1% resistor to GND

1.15. Power (74)

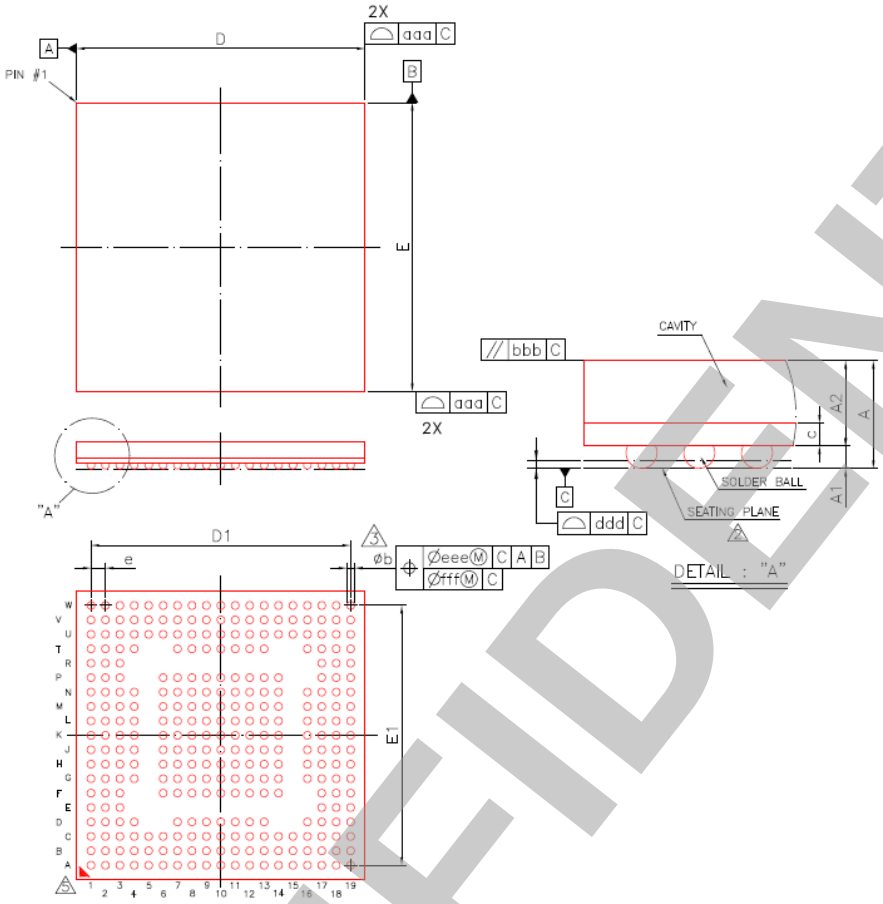
Pin No.	Name	Type	Descriptions
F12, G12, H6, H7, J7, K13, L13, L14, N8, N9, P8	VDDK(11)	P	Core Power
F14, G6, P14	VDD_IO(3)	P	I/O Pad Power
H9, H10, H11, J8, J9, J10, J11, N4, K8, K9, K10, K11, K12, L8, L9, L10, L11, L12, M8, M9	GND(20)	P	Digital Ground
F3, H4, L4, G4, K4, J3	VDD_DR(6)	P	DRAM I/O power. (1.8V for DDRII; 1.5V for DDRIII.)
H3	AVDD_DR_1V	P	Analog 1.0V power for DDR PHY
G3	AVDD_DLL(1)	P	DLL power.
K3	AGND_DLL(1)	P	Gorund for DLL
G11	VDD_RTC(1)	P	RTC Power
F11	VDD_VBAT(1)	P	Battery input for power button controller
V3	VDD_MC(1)	P	Multi-level IO power for Memory Card
F8, G9	AVDD_HSI_K	P	Analog 1.0V power for HSI core power
F9	AVDD_HSI_RX	P	Analog 3.3V power for HSI receiver
F10	VDD_HSI_IO	P	Multi-level input power of HSI
G10, H8	AGND_HSI(2)	P	Ground for High Speed Interface

G8	VDD_SN	P	Multi-level IO Power for sensor interface
P9, P10	VDD_LCD(2)	P	Multi-level IO power for LCD interface
L17	VDD_SDLI	P	LDO's input power for Card IO
P12	AVDD_DSI_K	P	Analog power for MIPI DSI core
N12	VDD_DSI_IO	P	LDO's input power for MIPI DSI LP IO
M12	AGND_DSI	P	Ground for MIPI DSI
U13	AVDD_ADC	P	Analog 3.3V power for ADC
U15	AGND_ADC	P	Ground for ADC
K16	AVDD_DAC	P	Analog 3.3V power for TV DAC
J16	AGND_DAC	P	Ground for TV DAC
T17	AVDD_AUD	P	Analog 3.3V power for Audio Codec
V17	AGND_AUD	P	Ground for Audio Codec
T16	AVDD_SPK	P	Analog 3.3V power for Speaker Amplifier
U16	AGND_SPK	P	Ground for Speaker Amplifier
K14	AVDD_HDMI	P	Analog HDMI interface Power
H17	AGND_HDMI	P	Ground for HDMI interface
G16	AVDD_USB_LI	P	LDO's input power for USB PHY
F18	VDD_USB_FS	P	USB Full Speed Transceiver Power
G17	AGND_USB	P	Ground for USB
T19	AVDD_MPLL	P	Multiple PLL analog Power
T18	AGND_MPLL	P	PLL analog Power

Package Outline

1.

TFBGA-305



Symbol	Dimension In mm			Dimension In Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	12.90	13.00	13.10	0.508	0.512	0.516
E	12.90	13.00	13.10	0.508	0.512	0.516
D1	---	11.70	---	---	0.461	---
E1	---	11.70	---	---	0.461	---
e	---	0.65	---	---	0.026	---
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		19/19			19/19	

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERENCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

Electrical Characteristics

1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage of 1.0V Core power	V_{DDK}	-0.3 ~ +1.2	V
Supply Voltage of DRAM I/O	V_{DD_DR}	-0.3 ~ +2.1	V
Supply Voltage of 3.3V Digital I/O	V_{DD_IO}, V_{DD_RTC}, V_{DD_VBAT}, V_{DD_SDLI}, $V_{DD\_DSI\_IO}$	-0.3 ~ +3.8	V
Supply Voltage of multi-level I/O	V_{DD_MC}, $V_{DD\_HSI\_IO}$, V_{DD_SN}, V_{DD_LCD}	-0.3 ~ +3.8	V
Supply Voltage of 1.0V analog block	$AV_{DD\_DR\_1V}$, $AV_{DD\_HSI\_K}$, $AV_{DD\_DSI\_K}$,	-0.3 ~ +1.2	V
Supply Voltage of 1.5/1.8V analog block	*AV_{DD_DLL}, AV_{DD_MPLL}, AV_{DD_HDMI}, $AV_{DD\_USB\_LI}$	-0.3 ~ +2.1	V
Supply Voltage of 3.3V analog block	$AV_{DD\_HSI\_RX}$, $AV_{DD\_USB\_FS}$, AV_{DD_ADC}, AV_{DD_DAC}, AV_{DD_AUD}, AV_{DD_SPK},	-0.3 ~ +3.8	V
Input/Output Voltage	I/O	-0.3 ~ V_{DD_IO} +0.3	V
Input Voltage(5V Tolerant)	I/O_{5VT}	-0.3 ~ +5.8	V
Operating Ambient Temperature	T_{OPR}	-10 ~ 70	^0C
Storage Temperature	T_{STG}	-55 ~ 125	^0C

*

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

2. ESD performance

Model	Standard	Classification	Note
Human Body Mode(HBM)	MIL-STD-883G Method 3015.7	Class : 2	2K~4KV
Machine Mode(MM)	JEDEC Specification EIA/JESD22-A115	Class : B	200~400V
CDM Mode(CDM)	JEDEC Specification JESD22-C101		

3. Latch-up Immunity

Model	Standard	Classification	Note
Latch up	JEDEC Specification JESD-78A	Class : I	±200mA

4. Recommended Operating Conditions

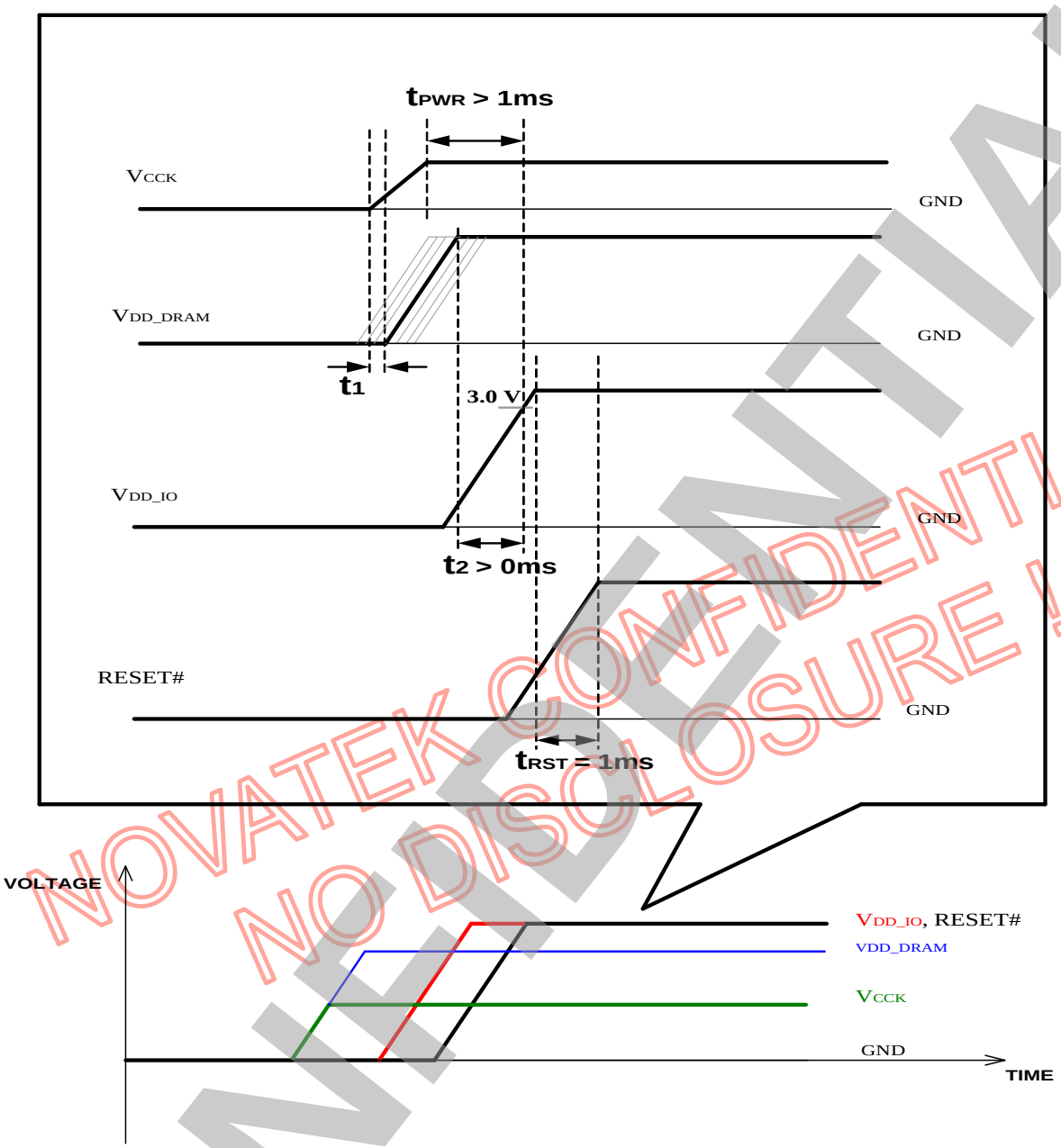
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DDK}	Core Logic Operating Voltage	1.0	1.05	1.1	V	
V_{DD_DR}	DDRII DRAM Interface Operating Voltage	1.7	1.8	1.9	V	DDRII DRAM
V_{DD_DR}	DDRIII DRAM Interface Operating Voltage	1.425	1.5	1.575	V	DDRIII DRAM
V_{DD_IO}	General I/O Interface Operating Voltage	3.0	3.3	3.6	V	
V_{DD_RTC}	RTC Operating Voltage	1.5	-	3.6	V	
V_{DD_RTC}	RTC Maintenance Voltage	1	-	3.6	V	
V_{DD_VBAT}	Power Controller Operating Voltage	1.5	-	3.6	V	
V_{DD_SDLI}	I/O of SD Card Operating Voltage	3.0	3.3	3.6	V	
$V_{DD\_DSI\_IO}$	LDO of MIPI DSI Operating Voltage	3.0	3.3	3.6	V	
V_{DD_MC}	I/O of Memory Card Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
$V_{DD\_HSI\_IO}$	Input of High Speed Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
V_{DD_SN}	I/O of Sensor Interface	1.62	3.3	3.6	V	1.8V~3.3V

	Operating Voltage					
V_{DD_LCD}	I/O of LCD Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
$AV_{DD\_DR\_1V}$	Core Logic of DDR PHY Operating Voltage	1.0	1.05	1.1	V	
$AV_{DD\_HSI\_K}$	Core Logic of High Speed Interface Operating Voltage	0.9	1.0	1.1	V	
$AV_{DD\_DSI\_K}$	Core Logic of MIPI DSI Operating Voltage	0.9	1.0	1.1	V	
AV_{DD_MPLL}	MPLL Operating Voltage	1.425	1.5	1.9	V	
AV_{DD_DLL}	DLL Operating Voltage	1.425	1.5	1.9	V	LV version
AV_{DD_HDMI}	Transceiver of HDMI Operating Voltage	1.425	1.5	1.9	V	
$AV_{DD\_USB\_LI}$	LDO of USB PHY Operating Voltage	1.425	1.5	1.9	V	
$AV_{DD\_HSI\_RX}$	Receiver of High Speed Interface Operating Voltage	3.0	3.3	3.6	V	
$AV_{DD\_USB\_FS}$	Transceiver of USB Full Speed Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_ADC}	ADC Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_DAC}	Video DAC Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_AUD}	Audio Codec Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_SPK}	Speaker Amplifier Operating Voltage	3.0	3.3	3.6	V	

5. AC/DC Characteristics

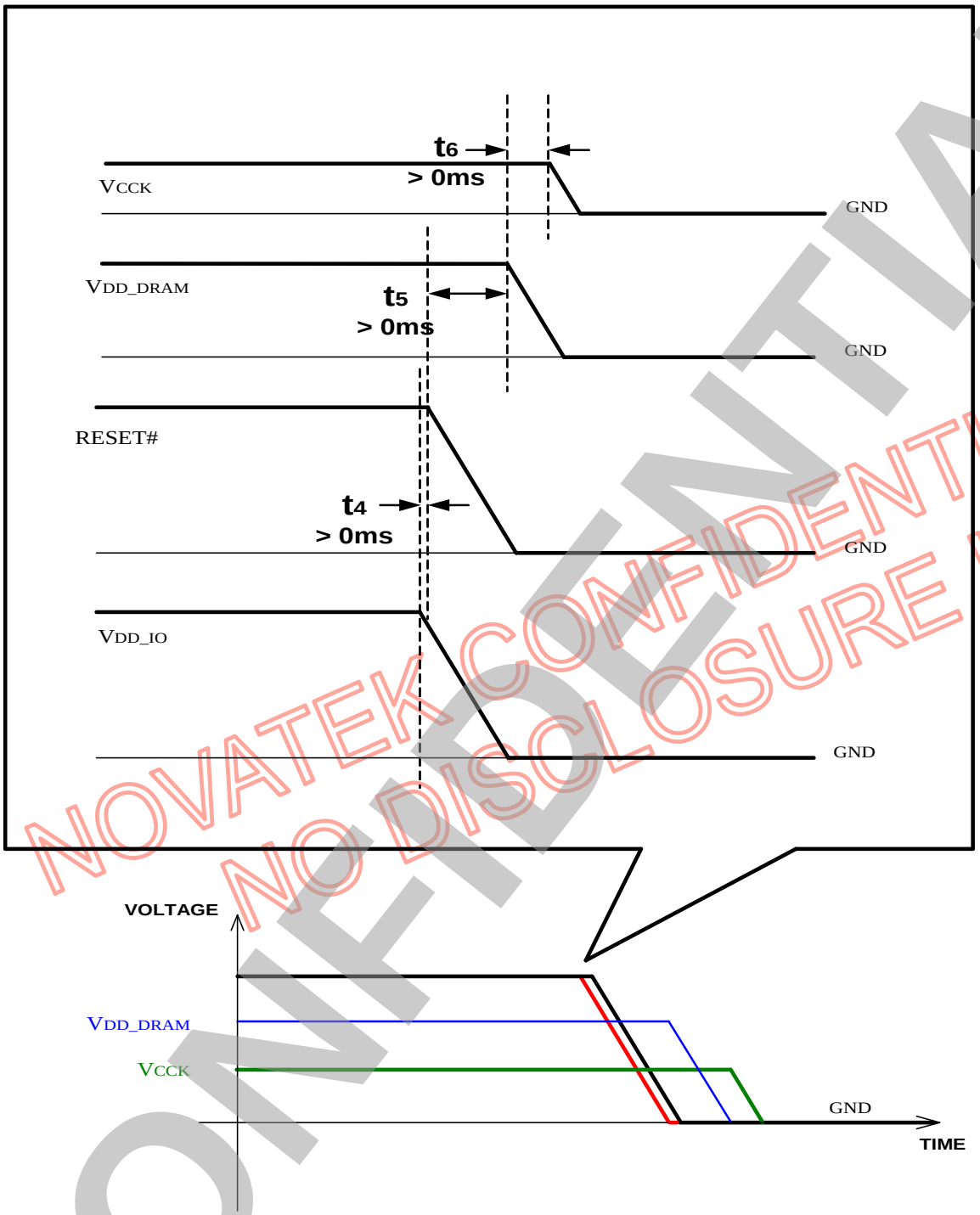
5.1. Power on Sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Power on sequence and Reset						
T_{RST}	RESET# sustained time	1	-	-	ms	after power being stable
T_{PWR}	Core power prior to I/O power time	1	-	-	ms	



POWER-ON SQUENCE

Note： Even $t_1 \geqq 0$ ms or $t_1 < 0$ ms is acceptable, but it is necessary to make sure $t_2 > 0$ ms .



POWER-OFF SEQUENCE

Note :

Novatek recommends that $t_4 > 0$ ms, $t_5 > 0$ ms, and $t_6 > 0$ ms for a stable system application. But they are not the required restrictions for Novatek's DSP.

5.2. General I/O

(V_{DDK}=1.0V, Temp=25^{0}C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
P_{RUN}	Operating Power Consumption	-	TBD	--	mW	Preview
I/O General characteristic						
V_{IH}	Input High Voltage (I/O)	2.0	-	-	V	V_{DD} = 3.3/2.5/1.8V
		1.7	-	-	V	
		1.2	-	-	V	
V_{IL}	Input Low Voltage (I/O)	-	-	0.8	V	V_{DD} = 3.3/2.5/1.8V
		-	-	0.7	V	
		-	-	0.6	V	
V_{T+}	Schmitt Trigger Positive Going Threshold (I/O)	-	1.73	2.0	V	V_{DD} = 3.3/2.5/1.8V
		-	1.38	1.6	V	
		-	1.08	1.2	V	
V_{T-}	Schmitt Trigger Negative Going Threshold (I/O)	1.1	1.26	-	V	V_{DD} = 3.3/2.5/1.8V
		0.8	1.00	-	V	
		0.6	0.72	-	V	
V_{HYST}	Hysteresis voltage	200	-	500	mV	
V_{OH}	Output High Voltage	V_{DD}-0.4	-	-	V	
V_{OL}	Output Low Voltage	-	-	0.4	V	
I_{OH}	Output Driving Current (V_{DD} = 3.3V)	2.5	-	-	mA	V_{OH} = V_{DD}-0.4V, @ 2.5/5/7.5/10 mA setting
		5	-	-	mA	
		7.5	-	-	mA	
		10	-	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 3.3V)	2.5	-	-	mA	V_{OL} = GND+0.4V, @ 2.5/5/7.5/10 mA setting
		5	-	-	mA	
		7.5	-	-	mA	
		10	-	-	mA	
I_{OH}	Output Driving Current (V_{DD} = 2.8V)	2	-	-	mA	V_{OH} = V_{DD}-0.4V, @ 2.5/5/7.5/10 mA setting
		4	-	-	mA	
		6	-	-	mA	
		8	-	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 2.8V)	2	-	-	mA	V_{OL} = GND+0.4V, @ 2.5/5/7.5/10 mA setting
		4	-	-	mA	
		6	-	-	mA	
		8	-	-	mA	
I_{OH}	Output Driving Current (V_{DD} = 1.8V)	1.5	-	-	mA	V_{OH} = V_{DD}-0.4V, @ 2.5/5/7.5/10 mA setting
		3	-	-	mA	
		4.5	-	-	mA	
		6	-	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 1.8V)	1.5	-	-	mA	V_{OL} = GND+0.4V, @ 2.5/5/7.5/10 mA setting
		3	-	-	mA	

		4.5	-	-	mA	
		6	-	-	mA	
$I_{ILeakage}$	Input Leakage Current	-10	±1	+10	uA	GND ≤ V_{IN} ≤ V_{DD}, input w/o R_{PU}/R_{PD}
I_{HIZ}	Output Tri-state Leakage Current	-10	±1	+10	uA	
R_{PU}	Internal Pull-up Resistor	-	28.5	-	KΩ	V_{IN}=GND, V_{DD} = 3.3/2.8/1.8V
		-	37.5	-	KΩ	
		-	56.5	-	KΩ	
R_{PD}	Internal Pull-down Resistor	-	28.5	-	KΩ	V_{IN}=V_{DD} V_{DD} = 3.3/2.8/1.8V,
		-	37.5	-	KΩ	
		-	56.5	-	KΩ	
I/O_{5VT} (5V tolerance I/O Schmitt input range)						
V_{T+}	Schmitt Trigger Positive Going Threshold (I/O_{5VT})	-	1.7	2.0	V	IO voltage @ 3.3V
V_{T-}	Schmitt Trigger Negative Going Threshold (I/O_{5VT})	1.0	1.40	-	V	
HSI (High Speed Interface Schmitt input range and pull-down resistor)						
V_{T+}	Schmitt Trigger Positive Going Threshold (HSI)	-	1.7	2.0	V	V_{DD} = 3.3/2.8/1.8V
		-	1.5	1.8	V	
		-	1.0	1.2	V	
V_{T-}	Schmitt Trigger Negative Going Threshold (HSI)	1.1	1.4	-	V	V_{DD} = 3.3/2.8/1.8V
		0.9	1.2	-	V	
		0.6	0.8	-	V	
R_{PD}	Internal Pull-down Resistor	-	100	-	KΩ	V_{IN}=V_{DD} V_{DD} = 3.3/2.8/1.8V,
		-	135	-	KΩ	
		-	400	-	KΩ	
I/Oz (large pull-down resistor)						
R_{PD_Z}	Internal Pull-down Resistor	-	1	-	MΩ	V_{IN}=GND, V_{DD}=3.3V
I/Ow (wide Schmitt input range)						
V_{T+}	Schmitt Trigger Positive Going Threshold (I/Ow)	-	1.7	2.0	V	V_{DD}=3.3V
V_{T-}	Schmitt Trigger Negative Going Threshold (I/Ow)	0.8	1.1	-	V	
V_{HYST}	Hysteresis voltage	500	-	750	mV	
I/O_s (strong driving/sinking output capacity)						
I_{OH}	Output Driving Current (V_{DD} = 3.3V)	5	-	-	mA	V_{OH} = V_{DD}-0.4V, @ 5/10/15/20 mA setting
		10	-	-	mA	
		15	-	-	mA	
		20	-	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 3.3V)	5	-	-	mA	V_{OL} = GND+0.4V, @ 5/10/15/20 mA setting
		10	-	-	mA	
		15	-	-	mA	
		20	-	-	mA	
I_{OH}	Output Driving Current	4	-	-	mA	V_{OH} = V_{DD}-0.4V,

	(V_{DD} = 2.8V)	8	-	-	mA	@ 5/10/15/20 mA setting
		12	-	-	mA	
		16	-	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 2.8V)	4	-	-	mA	V_{OL} = GND+0.4V, @ 5/10/15/20 mA setting
		8	-	-	mA	
		12	-	-	mA	
		16	-	-	mA	
I_{OH}	Output Driving Current (V_{DD} = 1.8)	3	-	-	mA	V_{OH} = V_{DD}-0.4V, @ 5/10/15/20 mA setting
		6	-	-	mA	
		9	-	-	mA	
		12	-	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 1.8)	3	-	-	mA	V_{OL} = GND+0.4V, @ 5/10/15/20 mA setting
		6	-	-	mA	
		9	-	-	mA	
		12	-	-	mA	
I/O_{s2} (strong driving/sinking output capacity)						
I_{OH}	Output Driving Current (V_{DD} = 3.3V)	12.5	-	-	mA	V_{OH} = V_{DD}-0.4V, @ 5/10/15/20 mA setting
		15	-	-	mA	
		17.5	-	-	mA	
		20	-	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 3.3V)	12.5	-	-	mA	V_{OL} = GND+0.4V, @ 5/10/15/20 mA setting
		15	-	-	mA	
		17.5	-	-	mA	
		20	-	-	mA	
I/O_{ss} (double strong driving/sinking output capacity)						
I_{OH}	Output Driving Current (V_{DD} = 3.3V)	12.5	-	-	mA	V_{OH} = V_{DD}-0.4V
		15	-	-	mA	
		17.5	-	-	mA	
		20	-	-	mA	
		25	-	-	mA	
		-	30	-	mA	
		-	35	-	mA	
		-	40	-	mA	
I_{OL}	Output Sinking Current (V_{DD} = 3.3V)	12.5	-	-	mA	V_{OL} = GND+0.4V
		15	-	-	mA	
		17.5	-	-	mA	
		20	-	-	mA	
		25	-	-	mA	
		-	30	-	mA	
		-	35	-	mA	
		-	40	-	mA	
R_{PU_SS}	Internal Pull-up Resistor	-	14	-	KΩ	V_{IN}=GND
R_{PD_SS}	Internal Pull-down Resistor	-	14	-	KΩ	V_{IN}=V_{DD}

5.3. Specific function I/O(RTC, Reset, LVD and PBC)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RTC						
T_{START_UP}	RTC 32768Hz crystal start up time	-	250	-	ms	V_{DD_RTC}=3.0V
I_{RTC}	Operating current of RTC	-	1	-	uA	V_{DD_RTC}=2.5V
V_{DD_RTCO}	Operating voltage of RTC	1.5	-	3.6	V	V_{DD_VBAT} >= 2.2V
V_{DD_RTCM}	Maintenance voltage of RTC	1	-	3.6	V	no V_{DD_VBAT}
RESET# & Low Voltage Detector						
R_{PU_RST}	Pull-Up Resistor of RESET#	80	100	130	KΩ	V_{DD}=3.3V
R_{PD_RST}	Pull-Down Resistor of RESET#	-	600	-	Ω	V_{DD}=3.3V
V_{DET}	Detect level of LVD	-	2.65	2.9	V	
V_{HYST}	Hysteresis voltage of LVD	-	90	-	mV	
V_{T+_RESET}	Schmitt Trigger Positive Going Threshold (RESET)	-	2.4	-	V	
V_{T-_RESET}	Schmitt Trigger Negative Going Threshold (RESET)	-	1.8	-	V	
Power Button Controller						
V_{T+}	Schmitt Trigger Positive Going Threshold (PWR_SW1,PWR_SW2, PWR_SW3,PWR_SW4)	-	1.5	1.8	V	V_{DD_RTC}=3.0V
V_{T-}	Schmitt Trigger Negative Going Threshold (PWR_SW1,PWR_SW2, PWR_SW3,PWR_SW4)	1	1.3	-	V	V_{DD_RTC}=3.0V
V_{PFD+}	PFD Positive Going Threshold Voltage (Core power)	-	0.85	0.9	V	V_{DD_VBAT} = 2.2~3.6V
V_{PFD-}	PFD Negative Going Threshold Voltage (Core power)	0.75	0.8	-	V	V_{DD_VBAT} = 2.2~3.6V
I_{PD1}	Pull-Down Current (PWR_SW1)	-	10	-	uA	V_{DD_RTC}=3.0V
I_{PU2}	Pull-Up Current (PWR_SW2)	-	10	-	uA	V_{DD_RTC}=3.0V
I_{PD3}	Pull-Down Current (PWR_SW3)	-	3	-	uA	V_{DD_RTC}=3.0V
I_{PD4}	Pull-Down Current (PWR_SW4)	-	1	-	uA	V_{DD_RTC}=3.0V
R_{OH}	Resistor of PWR_EN Output High	1100	1300	1500	Ω	V_{OH}=2.9V, V_{DD_RTC}=3.3V
R_{OL}	Resistor of PWR_EN	180	250	220	Ω	V_{OL}=0.4V, V_{DD_RTC}=3.3V

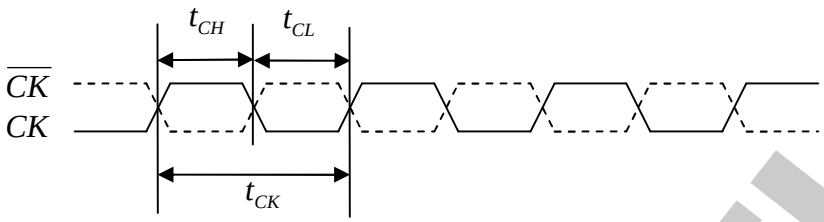
	Output Low					
V_{OH}	PWR_EN Output High Voltage	V_{BAT} - 0.2	-	-	V	@ I_{OH} = 100uA
V_{OL}	PWR_EN Output Low Voltage	-	-	0.1	V	@ I_{OL} = -100uA
Note						

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
R_{EN-CL}	PWR_EN Current Limit resistor	-	1K	-	Ohm	
V_{OH}	PWR_EN Output High Voltage	V_{BAT} - 0.2	-	-	V	@ I_{OH} = 100uA
V_{OL}	PWR_EN Output Low Voltage	-	-	0.1	V	@ I_{OL} = -100uA
R_{EN-CL}	PWR_EN Current Limit resistor	-	1K	-	Ohm	

5.4. DRAM

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DDRII DRAM						
DC specification						
V_{REF}	DRAM I/O Reference Voltage	0.49* V_{DD_DR}	-	0.51* V_{DD_DR}	V	
$V_{IH(DC)}$	DRAM I/O DC Input High (Logic 1) Voltage	V_{REF} +0.125	-	V_{DD_DR} +0.3	V	
$V_{IL(DC)}$	DRAM I/O DC Input Low (Logic 0) Voltage	-0.3	-	V_{REF} -0.125	V	
$V_{IH(AC)}$	DRAM I/O AC Input High (Logic 1) Voltage	V_{REF} +0.250	-	-	V	
$V_{IL(AC)}$	DRAM I/O AC Input Low (Logic 0) Voltage	-	-	V_{REF} -0.250	V	
I_{OH}	DRAM I/O Output Driving Current	4.6	-	-	mA	
I_{OL}	DRAM I/O Output Sinking Current	4.6	-	-	mA	
$I_{ILeakage}$	Input Leakage Current	-	-	±2	uA	GND ≤ V_{IN} ≤ V_{DD}, input w/o R_{PU}/R_{PD}
Differential input logic Level						
$V_{IN(DC)}$	DC differential signal voltage	-0.3	-	V_{DD_DR} +0.3	V	
$V_{ID(DC)}$	DC differential input voltage	0.25	-	V_{DD_DR} +0.6	V	
$V_{ID(AC)}$	AC differential input voltage	0.5	-	V_{DD_DR} +0.6	V	
$V_{IX(AC)}$	AC differential cross point voltage	0.5* V_{DD_DR} -0.175	-	0.5* V_{DD_DR} +0.175	V	

$V_{OX(AC)}$	AC differential output cross point voltage	0.5* V_{DD_DR} -0.125	-	0.5* V_{DD_DR} +0.125	V	
AC specification						
t_{CH}	clock high pulse width	0.45	0.5	0.55	t_{CK}	
t_{CL}	clock low pulse width	0.45	0.5	0.55	t_{CK}	
DDRIII DRAM						
DC specification						
V_{REF}	DRAM I/O Reference Voltage	0.49* V_{DD_DR}	-	0.51* V_{DD_DR}	V	
$V_{IH(DC)}$	DRAM I/O DC Input High (Logic 1) Voltage	V_{REF} +0.100	-	V_{DD_DR}	V	
$V_{IL(DC)}$	DRAM I/O DC Input Low (Logic 0) Voltage	V_{SS}	-	V_{REF} -0.100	V	
$V_{IH(AC)}$	DRAM I/O AC Input High (Logic 1) Voltage	V_{REF} +0.175	-	Note1	V	
$V_{IL(AC)}$	DRAM I/O AC Input Low (Logic 0) Voltage	Note1	-	V_{REF} -0.175	V	
I_{OH}	DRAM I/O Output Driving Current	4	-	-	mA	V_{DD_DR} =1.5V, V_{OH} = V_{DD_DR}-0.3V
I_{OL}	DRAM I/O Output Sinking Current	4	-	-	mA	V_{DD_DR} =1.5V, V_{OL} = V_{DD_DR}+0.3V
$I_{ILeakage}$	Input Leakage Current	-	-	±2	uA	GND ≤ V_{IN} ≤ V_{DD}, input w/o R_{PU}/R_{PD}
Differential input logic level						
$V_{IH(Diff)}$	Differential input high voltage	0.200	-	Note2	V	
$V_{IL(Diff)}$	Differential input low voltage	Note2	-	-0.200	V	
$V_{IHDiff(AC)}$	Differential input high AC voltage	2 * ($V_{IH(AC)}$ - V_{REF})	-	Note2	V	
$V_{ILDiff(AC)}$	Differential input low AC voltage	Note2	-	2 * (V_{REF} -$V_{IL(AC)}$)	V	
V_{IX}	Differential input cross point relative to VDD/2 for CK, CK#	-150	-	150	mV	
AC specification						
t_{CH}	clock high pulse width	0.45	0.5	0.55	t_{CK}	
t_{CL}	clock low pulse width	0.45	0.5	0.55	t_{CK}	
Note	1. refer to “Overshoot and Undershoot Specifications” 2. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications”					



SDR/DDR SDRAM clock high pulse and low

5.5. High speed serial interface(MIPI CSI, LVDS, HiSPi)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Input Impedance						
Z_{ID}	Impedance of Differential Terminator	80	100	125	Ohm	(check resistor's accuracy)
LVDS/HiSPi(Sub-LVDS/HiVCM) **HS Receiver DC Specifications**						
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	600	900	1200	mV	
V_{IDTH}	Differential input high threshold	-	-	70	mV	("Z" : 25mV)
V_{IDTL}	Differential input low threshold	-70	-	-	mV	("Z" : -25mV)
V_{IHHS}	Single-ended input high voltage	-	-	1500	mV	(1200+300)
V_{ILHS}	Single-ended input low voltage	400	-	-	mV	
HiSPi(SLVS) **HS Receiver DC Specifications**						
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	150	200	250	mV	
V_{IDTH}	Differential input high threshold	-	-	70	mV	("Z" : 25mV)
V_{IDTL}	Differential input low threshold	-70	-	-	mV	("Z" : -25mV)
V_{IHHS}	Single-ended input high voltage	-	-	490	mV	(360+130))
V_{ILHS}	Single-ended input low voltage	-10	-	-	mV	(120-130)
MIPI **HS Receiver DC Specifications**						
$V_{CMRX(DC)}$	Common-mode voltage HS	70	-	330	mV	Note 1,2

	receive mode					
V_{IDTH}	Differential input high threshold	-	-	70	mV	
V_{IDTL}	Differential input low threshold	-70	-	-	mV	
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	Note 1
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	Note 1
Note	1. Excluding possible additional RF interface of 100mV peak sine wave beyond 450MHz. 2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variation below 450MHz.					
MIPI **LP Receiver DC specifications**						
V_{IH}	Logic 1 input voltage	880	-	-	mV	
V_{IL}	Logic 0 input voltage, not in ULP State	-	-	500	mV	
V_{HYST}	Input Hysteresis	25	-	-	mV	
General Purpose Input DC specifications						
V_{T+}	Schmitt Trigger Positive Going Threshold	-	1.6	2.0	V	V_{DD_GPI} = 3.3V
V_{T-}	Schmitt Trigger Negative Going Threshold	0.8	1.2	-	V	V_{DD_GPI} = 3.3V
R_{PD}	Pull Down Resistance	-	100K	-	Ohm	V_{DD_GPI} = 3.3V
V_{HYST}	Input Hysteresis	300	-	-	mV	V_{DD_GPI} = 3.3V
LVDS/HiSPi **Receiver AC Specifications**						
C_{CM}	Common-mode termination	-	10	-	pF	(5pF option)
MIPI **HS Receiver AC Specifications**						
F_{CLK}		40	-	500	MHz	160MHz Tx T hs_exit > 16 HSCLK
ΔV_{CMRX_HF}	Common-mode interference beyond 450MHz	-	-	100	mV	Note 2
ΔV_{CMRX_LF}	Common-mode interference 50MHz-450MHz	-50	-	50	mV	Note 1,4
C_{CM}	Common-mode termination	-	10	60	pF	Note 3 (5pF option)
Note	1. Excluding 'static' ground shift of 50mV 2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs. 3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification. 4. Voltage difference compared to DC average common-mode potential.					
MIPI **LP Receiver AC specifications**						

e_{SPIKE}	Input pulse rejection	-	-	300	V·ps	Note 1,2,4
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	Note 4
V_{INT}	Peak interference amplitude	-	-	200	mV	
f_{INT}	Interference frequency	450	-	-	MHz	
Note	1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. 2. An impulse less than this will not change the receiver state. 3. In addition to the required glitch rejection, implements shall ensure rejection of known RF-interferences. 4. An input pulse greater than this shall toggle the output.					

5.6. ADC

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{DD_ADC}	Supply Voltage		3.0	3.3	3.6	V	
RES	ADC Effective Resolution		-	9	-	Bits	10bits SAR ADC structure (≦125KSPS
V_{IN}	Input signal level		0	-	V_{DD_ADC}	V	
INL	Integral nonlinearity		-	±1	-	LSB	
DNL	Differential nonlinearity		-	±0.5	-	LSB	
C_{IN}	Input capacitance		-	20	-	pF	Except ADC_IN0,ADC_IN3
$C_{IN-buffer}$	Input capacitance of buffer		-	1	-	pF	ADC_IN0,ADC_IN3
R_{SW}	Touch panel switch on resistance	P	-	15	-	Ω	
		N		15		Ω	
R_{PU}	Programmable resistor range	Max	-	65	-	KΩ	MOS switch parasitic resistance is about 1kOhm.
		Min	-	2	-	KΩ	
R_{RPS}	Programmable resistor step size		-	1	-	KΩ	
I_P	Current source	Max	-	200	-	uA	
		Min	-	100	-	uA	
V_{T+}	Touch Panel Pen Down Schmitt Trigger Positive Going Threshold		-	1.8	-	V	
V_{T-}	Touch Panel Pen Down Schmitt Trigger Negative Going Threshold		-	1.4	-	V	

5.7. Audio Codec

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Microphone						
V_{MIC_BIAS}	Mic Bias Output Level	-	2.0	-	V	

V_{IN}	Input Full Scale Level	-	1	-	Vp-p	0dB gain
SNR	Signal to Noise Ratio	-	68	-	dBA	0dB gain, A-weighting
THD+N	Total Harmonic Distortion Plus Noise Ratio	-	-65	-	dBA	0dB gain, A-weighting
R_{IN}	Input Resistance	-	2.38	-	KΩ	PGA gain set to +25.5 dB
		-	24	-	KΩ	PGA gain set to 0 dB
		-	44.2	-	KΩ	PGA gain set to -21 dB
G_{PGA}	Programmable Gain Amplifier Range	-21	-	+25.5	dB	32 steps
G_{STEP}	Programmable Gain Amplifier Step Size	-	1.5	-	dB	
G_{Boost}	Boost Gain	-	20	-	dB	0/10/15/20 dB
Headphone or Line Out						
V_{OUT}	Line output full scale	-	0.698	-	V_{RMS}	
SNR	Signal to noise ratio	-	85	-	dBA	
THD+N	Total harmonic distortion plus noise ratio	-	-80	-	dBA	
Speaker BTL Output @ 8Ω						
SNR	Signal to Noise Ratio	-	90	-	dB	A-weighting
THD+N	Total Harmonic Distortion Plus Noise Ratio	-	TBD	-	dB	A-weighting
G_{PGA}	Programmable Gain Amplifier Range	-31.6	-	+6	dB	32 steps
G_{STEP}	Programmable Gain Amplifier Step Size	-	1.17	-	dB	
P_{SPK}	BTL Speaker Output Power	-	280	-	mW	THD @ 10%
		-	180	-	mW	THD @ 1%
Note	1. The SNR of audio output is measured according to AES17-1998 CL 9.3					

5.8. TV encoder

(R_{LOAD} = 37.5Ω, Conversion rate = 27MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RES	Video DAC Effective Resolution	-	10	-	bits	10-Bits I-Steering DAC structure
INL	Integral Nonlinearity, INL	-	±1	-	LSB	
DNL	Differential Nonlinearity, DNL	-	±0.5	-	LSB	
I_{CODE}	Output Current-DAC Code 1023 (Iout FS)	-	34.08	-	mA	R_{load} = 37.5 Ohm
V_{CODE}	Out Voltage-DAC Code 1023	-	1.28	-	V	R_{load} = 37.5 Ohm
VLE	Video Level Error	-5	-	+5	%	
V_{OC}	Output Compliance Range	0	-	1.4	V	
F_{CLK}	Conversion rate	-	27	-	MHz	

5.9. MIPI DSI Tx

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
MIPI D-PHY DC specifications						
HS Transmitter						
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV	Note. 1
$\|\Delta V_{CMTX(1,0)}\|$	VCMTX mismatch when output is Differential-1 or Differential-0	-	-	5	mV	Note. 2
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV	Note. 1
$\|\Delta V_{OD}\|$	VOD mismatch when output is Differential-1 or Differential-0	-	-	10	mV	Note. 2
V_{OHHS}	HS output high voltage			360	mV	Note. 1
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance Mismatch	-	-	10	%	
Note	1. Value when driving into load impedance anywhere in the Z_{ID} range. 2. It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity.					
LP Transmitter						
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	VOH
V_{OL}	Thevenin output low level	-50	-	50	mV	VOL
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω	Note. 1,2
Note	1. See Figure 42 and Figure 43. in MIPI D-PHY specification. 2. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.					
LP Receiver						
V_{IH}	Logic 1 input voltage	880	-	-	mV	
V_{IL}	Logic 0 input voltage, not in ULP State	-	-	500	mV	
V_{IL_ULPS}	Logic 0 input voltage, ULP State	-	-	300	mV	
V_{HYST}	Input Hysteresis	25	-	-	mV	
Note	1. See Figure 42 and Figure 43. in MIPI D-PHY specification. 2. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.					

Contention Detector (LP-CD)						
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	
MIPI D-PHY AC specifications						
HS Transmitter						
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz	-	-	15	mV RMS	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz	-	-	25	mV PEAK	
$t_{R\ and}\ t_F$	20%-80% rise time and fall time	-	-	0.3	UI	Note. 1
		150	-	-	ps	
Note	1. UI is equal to 1/(2*fh). See section 7.3 for the definition of fh					
LP Transmitter						
T_{RLP}/T_{FLP}	15%-85% rise time and fall time	-	-	25	ns	Note. 1
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns	Note. 1, 5, 6
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock: First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	-	-	ns	Note. 4
	Pulse width of the LP exclusive-OR clock: All other pulses	20	-	-	ns	Note 4
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90	-	-	ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	-	-	500	mV/ns	Note 1, 3, 7, 8
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	Note 1, 3, 7, 8
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	Note 1, 3, 7, 8
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	Note 1, 3, 7, 8
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	Note 1, 2, 3
	Slew rate @ CLOAD = 0	30	-	-	mV/ns	Note 1, 3, 9

	to 70pF (Rising Edge Only)					
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST – 700)	-	-	mV/ns	Note. 1, 10, 11
C_{LOAD}	Load capacitance	0	-	70	pF	Note 1
Note	1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. 2. When the output voltage is between 400 mV and 930 mV. 3. Measured as average across any 50 mV segment of the output signal transition. 4. This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in section 8.2.2. 5. The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive. 6. With an additional load capacitance CCM between 0 and 60pF on the termination center tap at RX side of the Lane 7. This value represents a corner point in a piecewise linear curve. See Figure 45 and Figure 46. 8. When the output voltage is in the range specified by V_{PIN}(absmax). 9. When the output voltage is between 400 mV and 700 mV. 10. Where $V_{O,INST}$ is the instantaneous output voltage, V_{DP} or V_{DN}, in millivolts. 11. When the output voltage is between 700 mV and 930 mV.					
LP Receiver						
e_{SPIKE}	Input pulse rejection	-	-	300	V·ps	Note 1,2,3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	Note 4
V_{INT}	Peak interference amplitude	-	-	200	mV	
f_{INT}	Interference frequency	450	-	-	MHz	
Note	1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. 2. An impulse less than this will not change the receiver state. 3. In addition to the required glitch rejection, implements shall ensure rejection of known RF-interferences. 4. An input pulse greater than this shall toggle the output.					
Pin Characteristic Specifications						
V_{PIN}	Pin signal voltage range	-50	-	1350	mV	
I_{LEAK}	Pin leakage current	-10	-	10	uA	
V_{GNDSH}	Ground shift	-50	-	50	mV	
V_{PIN}	Transient pin voltage level	-0.15	-	1.45	V	

(absmax)						
T_{VPIN} (absmax)	Maximum transient time above VPIN(max) or below VPIN(min)	-	-	20	ns	
Note	1. When the pad voltage is in the signal voltage range from $V_{GNDSH,MIN}$ to VOH + $V_{GNDSH,MAX}$ and the Lane Module is in LP receive mode. 2. The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range. 3. This value includes ground shift.					

Figure. D-PHY signaling level

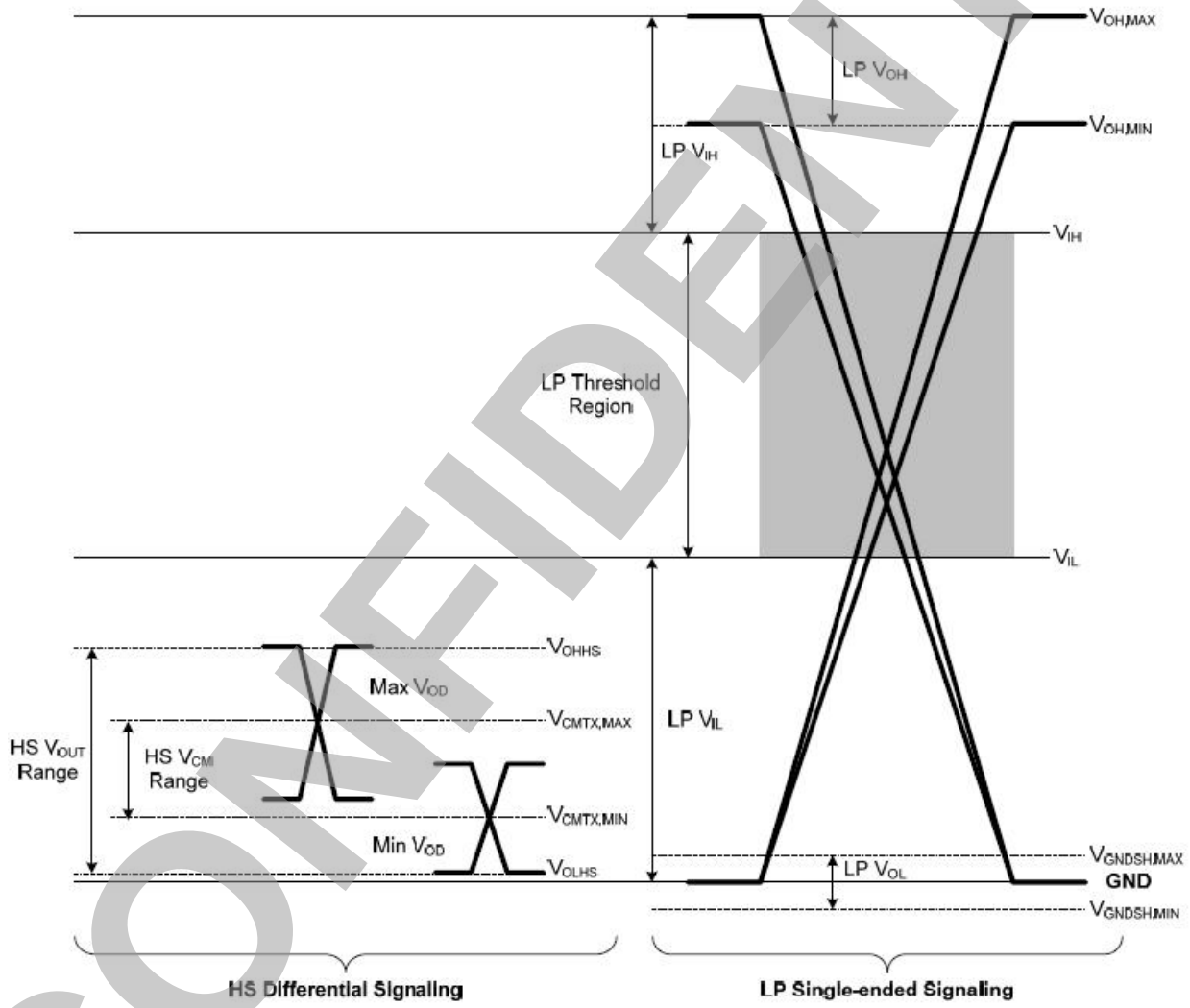
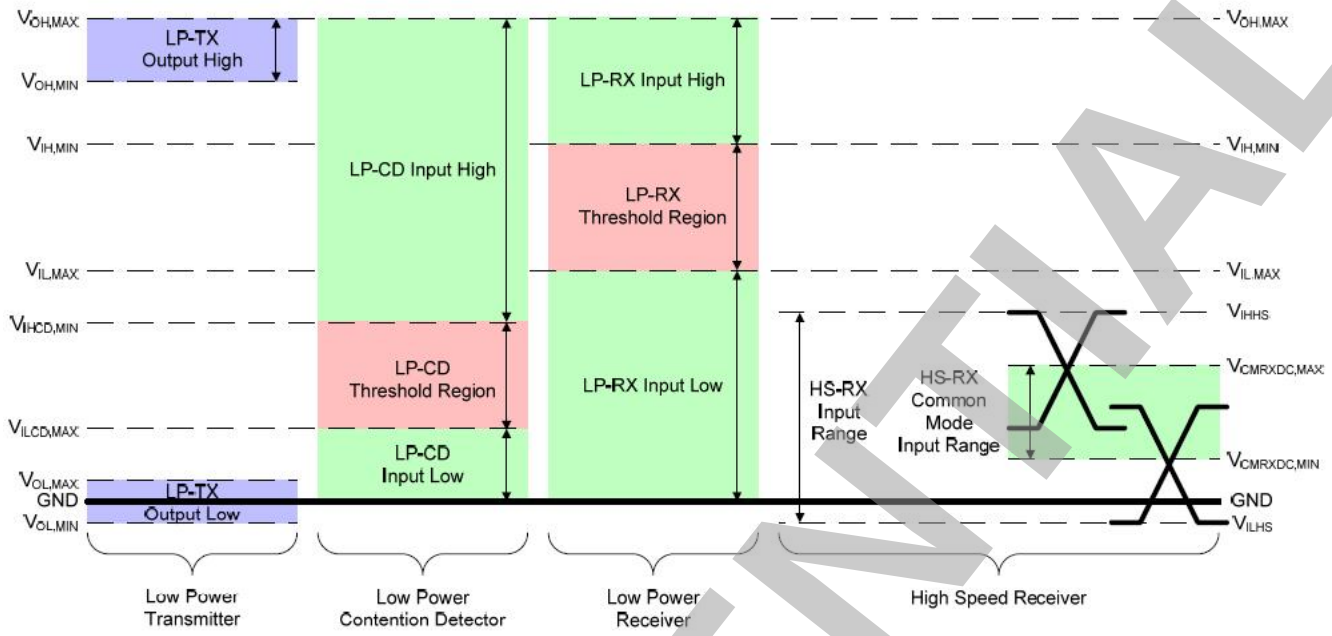


Figure. Signaling and contention Voltage levels



5.10. HDMI Tx

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Transmitter DC Specifications						
V_{OFF}	Single-ended standby output voltage	3.125	3.3	3.475	V	
V_{SWING}	Single-ended output swing voltage	400	500	600	mV	
V_H	Single-ended high level output voltage	2.935	3.3	3.475	V	
V_L	Single-ended low level output voltage	2.435	2.8	3.065	V	
Transmitter AC Specifications						
	Rise/fall time	75	-	-	ps	
	Intra-Pair Skew at source connector	-	-	0.15	T_{bit}	
	Inter-Pair Skew at source connector	-	-	0.20	$T_{char.}$	
	Clock duty cycle	40	50	60	%	
	TMDS Differential Clock Jitter	-	-	0.25	T_{bit}	
Hot Plug Detection Signal						
V_{IH}	Input High Voltage (HDMI PLUG)	2.0	-	-	V	Max 5.3V
V_{IL}	Input Low Voltage	-	-	0.8	V	

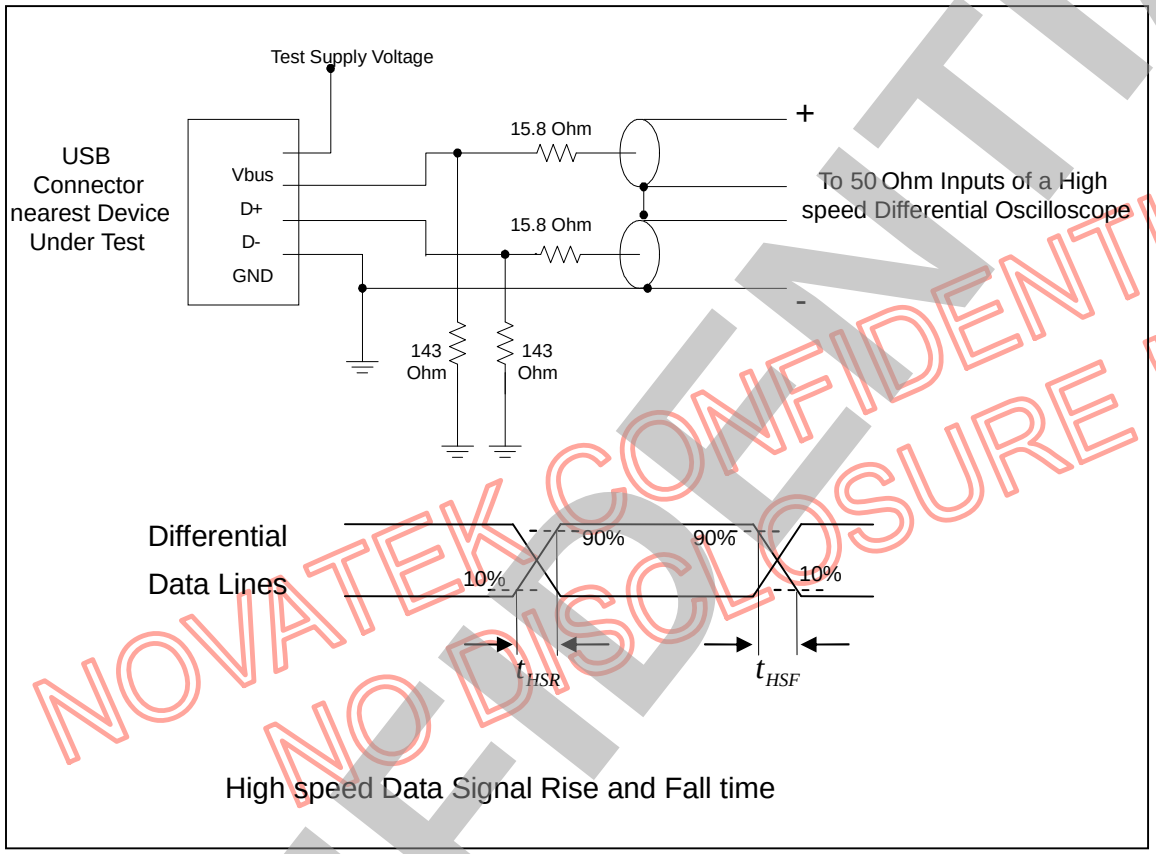
	(HDMI_PLUG)					
Note						

5.11. USB

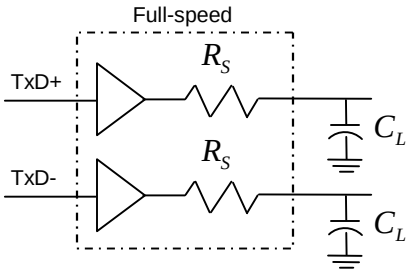
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
High Speed DC Specifications						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	300	-	-	mV	$\|V_{I(DP)}-V_{I(DM)}\|$ measured at the connection as application circuit
V_{HSCM}	High speed data signaling common mode voltage range	-50	-	500	mV	
V_{HSSQ}	High speed squelch detection threshold	-	-	100	mV	squelch detected
		150	-	-	mV	no squelch detected
V_{HSDSC}	High speed disconnection detection threshold	625	-	-	mV	disconnection detected
		-	-	525	mV	disconnection not detected
Output Levels						
V_{HSOI}	High speed idle level output voltage (differential)	-10	-	10	mV	
V_{HSOL}	High speed low level output voltage (differential)	-10	-	10	mV	
V_{HSOH}	High speed high level output voltage (differential)	-360	-	400	mV	
V_{CHRPJ}	Chirp-J output voltage (differential)	700	-	1100	mV	
V_{CHIRPK}	Chirp-K output voltage (differential)	-900	-	-500	mV	
Resistance						
R_{DRV}	Driver output impedance	3	6	9	Ω	equivalent resistance used as internal chip only
		40.5	45	49.5	Ω	overall resistance including external resistor
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU	3.0	-	3.6	V	
Full Speed DC Specifications						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	0.2	-	-	V	$\|V_{I(DP)}-V_{I(DM)}\|$
V_{CM}	Differential common mode voltage	0.8	-	2.5	V	
Input Levels (single-ended receivers)						

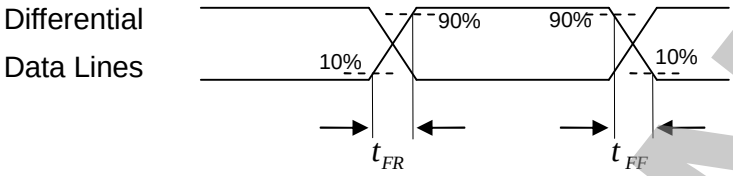
V_{SE}	Single ended receiver threshold	0.8	-	2.0	V	
Output Levels						
V_{OL}	Low-level output voltage	0	-	0.3	V	
V_{OH}	High-level output voltage	2.8	-	3.6	V	
High Speed AC Specifications						
Driver Characteristics						
$T_{HSDRATE}$	High speed TX data rate	479.76	-	480.24	Mbps	
$T_{HSRDRATE}$	High speed RX data rate	479.76	-	480.24	Mbps	
t_{HSR}	High speed differential rise time	500	-	-	ps	
t_{HSF}	High speed differential fall time	500	-	-	ps	
Driving timing						
	Driver waveform requirement	see eye pattern of template 1				Follow template1 described in USB2.0 spec
Receiver timing						
	Data source jitter and receiver jitter tolerance	see eye pattern of template 4				Follow template 4 described in USB2.0 spec
Full Speed AC Specifications						
Driver Characteristics						
$T_{FSDRATE}$	Full speed TX data rate	11.994	-	12.006	Mbps	
$T_{FSRDRATE}$	Full speed RX data rate	11.97	-	12.03	Mbps	
t_{FR}	Rise time	4	-	20	ns	CL=50pF; 10 to 90% of $\|V_{OH}-V_{OL}\|$
t_{FF}	Fall time	4	-	20	ns	CL=50pF; 90 to 10% of $\|V_{OH}-V_{OL}\|$
t_{FRMA}	Differential rise/fall time matching (t_{FR}/t_{FF})	90	-	110	%	Excluding the first transition from idle mode
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V	Excluding the first transition from idle mode
Driving timing						
	VI, FSE0, OE to DP, DN propagation delay	-	-	15	ns	for detailed description of VI, FSE0 and OE, please refer to USB1.1 spec
T_{FDEOP}	Source jitter for differential transition to SE0 transition	-2	-	5	ns	
T_{JR1}	Receiver jitter	-18.5	-	18.5	ns	To next transition
T_{JR2}	Receiver jitter	-9	-	9	ns	For paired transition
T_{FEOPT}	Source SE0 interval of EOP	160	-	175	ns	
T_{FEOPR}	Receiver SE0 interval of EOP	82	-	-	ns	
T_{FST}	Width of SE0 interval during differential transition	-	-	14	ns	

Receiver timing						
$t_{PLH(RCV)}$ $t_{PHL(RCV)}$	Receiver propagation delay (DP; DM to RCV)	-	-	15	ns	for detailed description of RCV, please refer to USB1.1 spec
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP, VON)	-	-	15	ns	
Note						

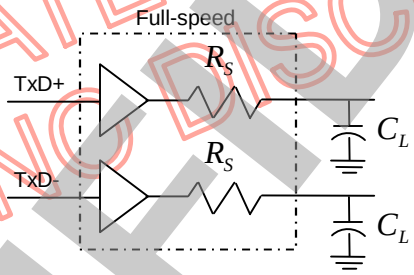


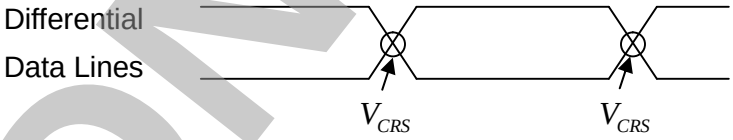
High speed Data Signal Rise and Fall time





Full speed Data Signal Rise and Fall time





Full speed Output Signal Crossover Voltage

5.12. USB Charging Port Detect

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DAT_REF}	Data Detect Voltage	0.25	-	0.4	V	
V_{DM_SRC}	D- Source Voltage	0.5	-	0.7	V	
V_{DP_SRC}	D+ Source Voltage	0.5	-	0.7	V	
V_{LGC}	Logic Threshold	0.8	-	2.0	V	
V_{LGC_HI}	Logic High	2.0	-	3.6	V	
V_{LGC_LOW}	Logic Low	0	-	0.8	V	
I_{DM_SINK}	D- Sink Current	25	-	175	uA	
I_{DP_SINK}	D+ Sink Current	25	-	175	uA	
I_{DP_SRC}	Data Contact Detect Current Source	7	-	13	uA	
R_{DM_DWN}	D- Pull-down resistance	14.25	-	24.8	kΩ	