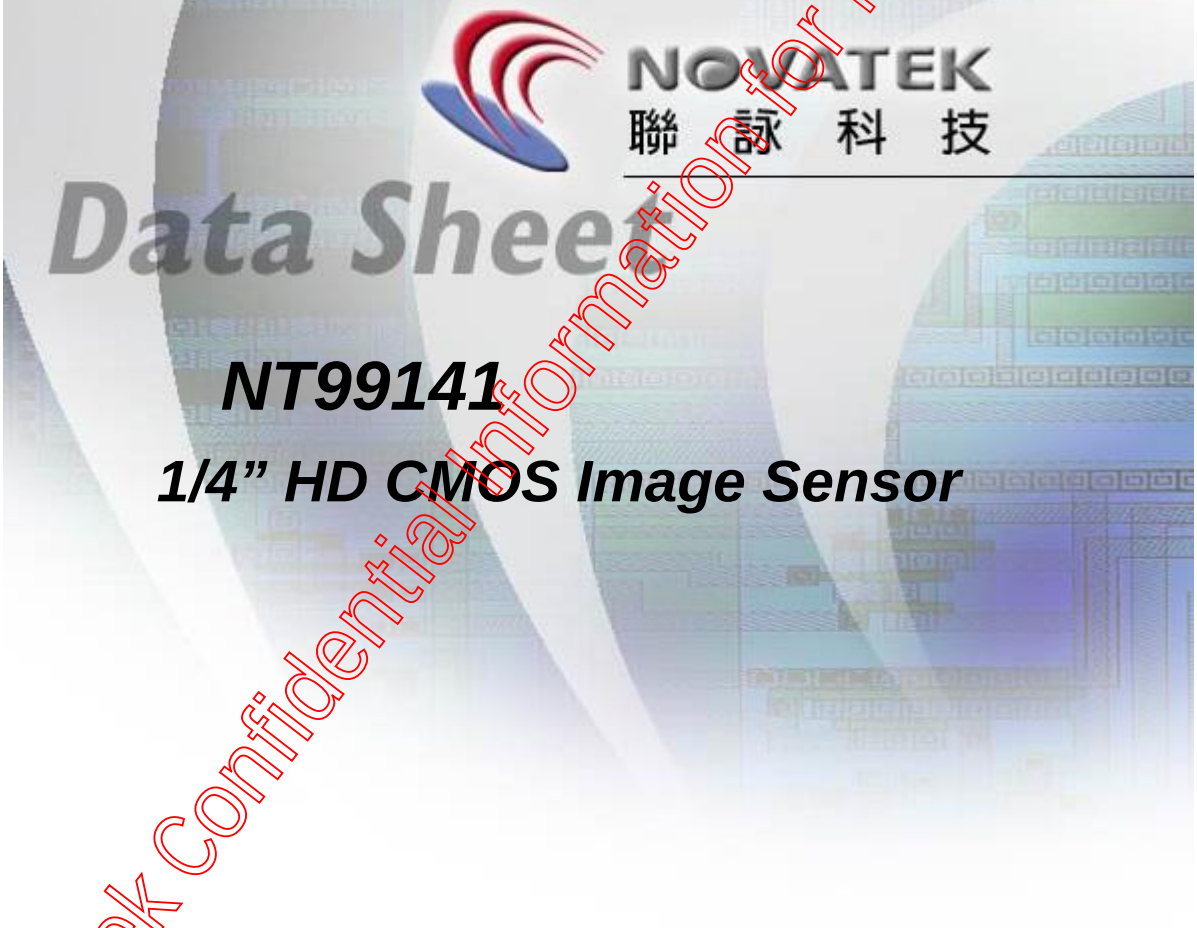


NT99141

1/4” HD CMOS Image Sensor

Table of Contents

Figures

1. Features

- Low dark current
- Auto black level calibration
- Two wire serial interface, 16-bit address and 8-bit data
- Support output format: YCbCr (4:2:2), RGB565, RGB555, RGB444, Raw, CCIR656, and JPEG also.
- Support image size: HD (1280 x 720), and any size from scaling down
- Lens shading correction
- Automatic control functions: Auto-Exposure control(AE), Auto-White Balance(AWB)
- Including: Sharpness, noise reduction, defect correction, gamma, color saturation adjust.
- Specical effects included.
- Embedded 1.5V regulator for core power
- Target module size: 8mm x 8mm
- Multi-Sensor Mode for 3D application.

2. Key Performance

Parameter		Value
Array Size		1284x 724
Power Supply	Digital	1.5V ± 5%
	Analog	3.0V ~ 3.6V
	I/O	1.7V ~ 3.6V
Pixel Size		3.0 μm x 3.0 μm
Image Area		3852 μm x 2172 μm
ADC Resolution		10 bits
Shutter		Electronic Rolling Shutter
Frame rate	640x360	60 fps
	HD (1280x720)	30 fps
Color Filter Arrays		RGB Bayer pattern
Maximum Data Rate		40Mp/s
Maximum Clock Rate		80MHz
Power Consumption		215 mW @ HD JPG
		Standby: < 10 uA

3. General Description

The NT99141 is such a high performance image sensor that by incorporating a 1284H x 724V image array, an on-chip 10 bits ADC, and embedded image signal processor all the required image signal processing functions - including sharpness, noise reduction, defect correction, gamma, and color saturation adjust - are in default supported, while its easy controllability and usability are maintained by the two-wire serial interface bus.

It is suitable for use in products such as cellular phones and PC cameras.

4. Block Diagram

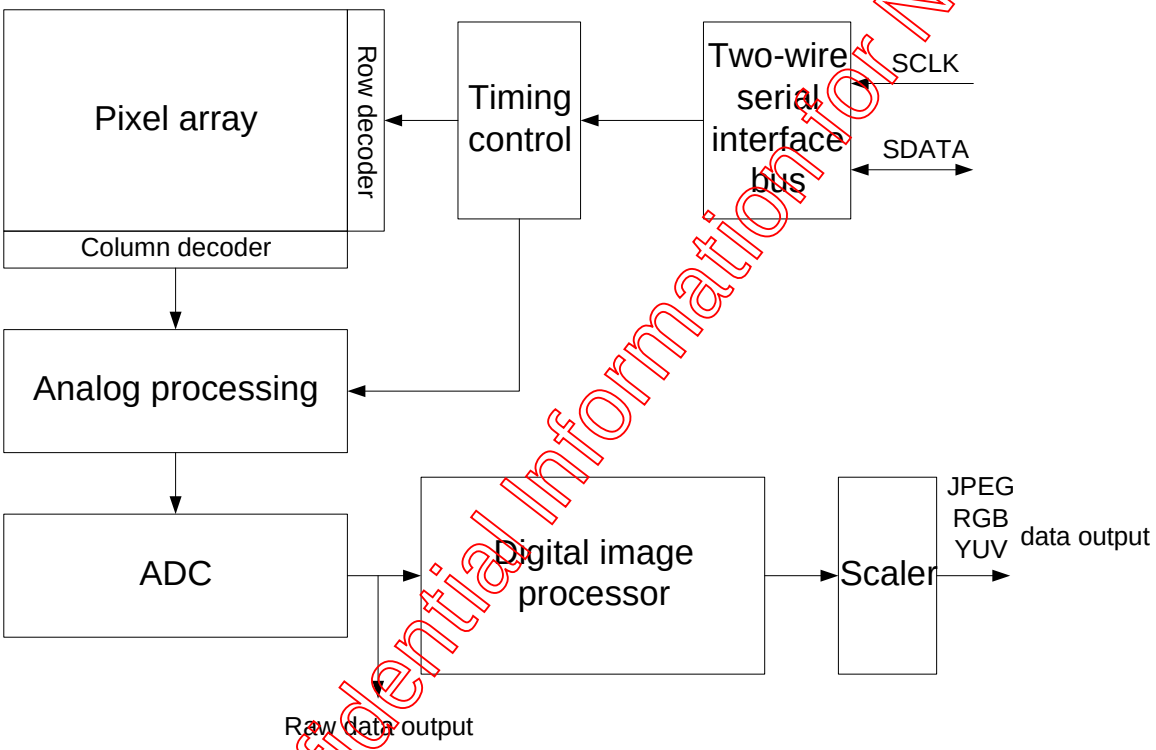


Fig. 1 Block Diagram

5. Pin Configuration

(Top view)

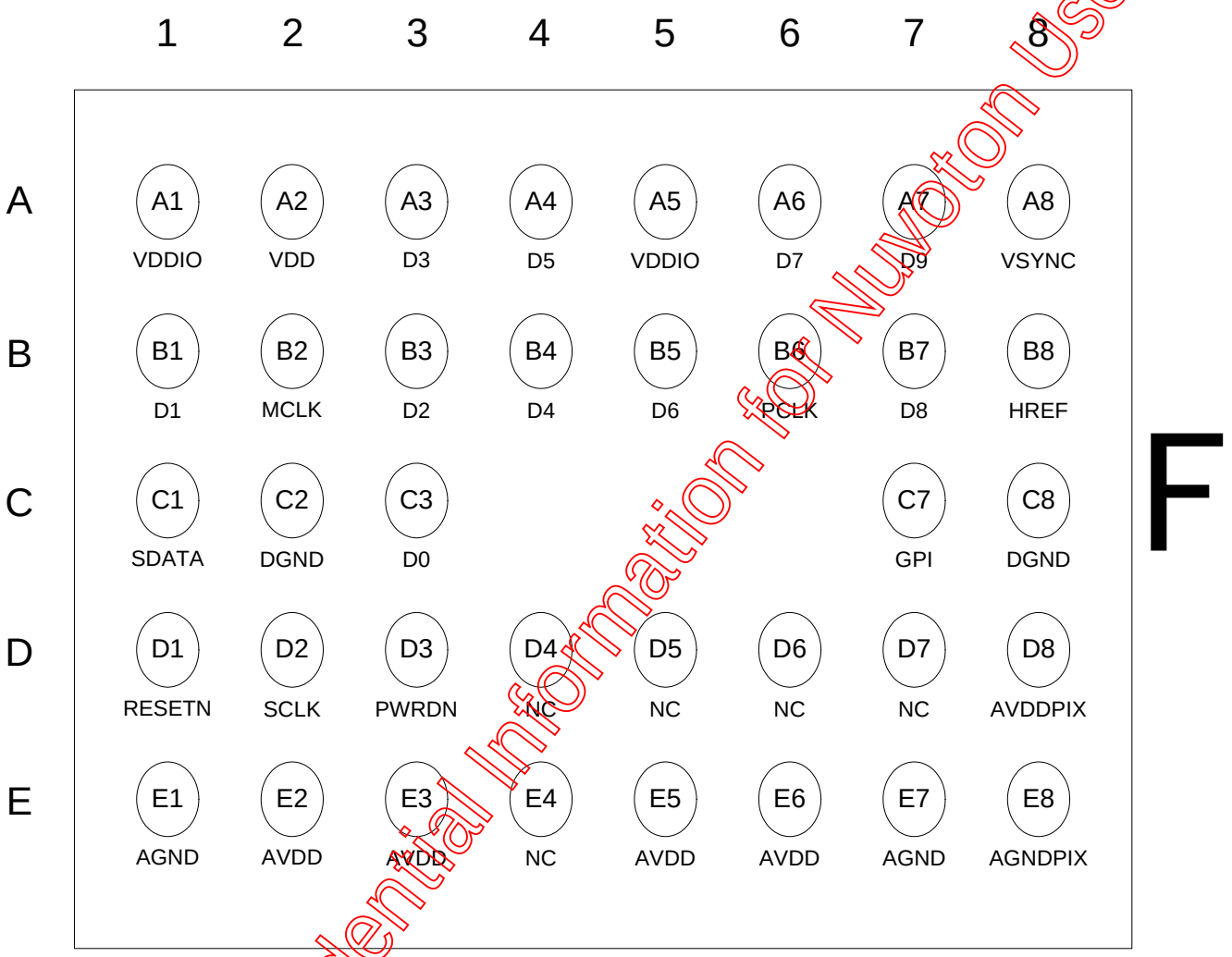


Fig. 2 Pin Configuration

6. Pin Descriptions

I = input port

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking

The Reset column below shows the pin's default state after a power reset.

Pin No.	Name	Type	Reset	Descriptions
A1	VDDIO	Power	-	Digital power for I/O
A2	VDD	Power	-	Digital core power
A3	D3	O	-	Data output 3
A4	D5	O	-	Data output 5
A5	VDDIO	Power	-	Digital power for I/O
A6	D7	O	-	Data output 7
A7	D9	O	-	Data output 9
A8	VSYNC	O	-	Vertical synchronization
B1	D1	O	-	Data output 1
B2	MCLK	I	-	System clock input
B3	D2	O	-	Data output 2
B4	D4	O	-	Data output 4
B5	D6	O	-	Data output 6
B6	PCLK	O	-	Pixel clock output
B7	D8	O	-	Data output 8
B8	HREF	O	-	Horizontal reference
C1	SDATA	I/O	-	Two-wire serial interface bus data I/O
C2	DGND	Ground	-	Digital ground
C3	D0	O	-	Data output 0
C7	GPI	I	-	Multi-sensor function
C8	DGND	Ground	-	Digital ground
D1	RESETN	I	-	Power on reset, active low 0: reset 1: normal
D2	SCLK	I	-	Two-wire serial interface bus clock input
D3	PWRDN	I	-	Power down mode select, active high 0: normal mode 1: power down mode
D4	NC	-	-	NC
D5	NC	-	-	NC
D6	NC	-	-	NC
D7	NC	-	-	NC
D8	AVDDPIX	Power	-	Pixel power
E1	AGND	Ground	-	Analog ground
E2	AVDD	Power	-	Analog power
E3	AVDD	Power	-	Analog power
E4	NC	-	-	NC
E5	AVDD	Power	-	Analog power
E6	AVDD	Power	-	Analog power
E7	AGND	Ground	-	Analog ground
E8	AGNDPIX	Ground	-	Pixel ground

Note: D[9:0] is 10-bit Raw output(D9: MSB, D0: LSB), D[9:2] is 8-bit YUV/RGB/JPEG output

7. Package Outline

	Symbol	Nominal	Min.	Max
			µm	
Package Body Dimension X	**A**	5406	5381	5431
Package Body Dimension Y	**B**	4334	4309	4359
Package Height	**C**	780	720	840
Ball Height	**C1**	160	130	190
Package Body Thickness	**C2**	620	575	665
Thickness of Glass surface to wafer	**C3**	445	425	465
Ball Diameter	**D**	300	270	330
Total Pin Count	**N**	37(5NC)		
Pin Count X axis	**N1**	8		
Pin Count Y axis	**N2**	5		
Pins Pitch X axis	**J1**	620		
Pins Pitch Y axis	**J2**	800		
Edge to Pin Center Distance along X	**S1**	533	503	563
Edge to Pin Center Distance along Y	**S2**	567	537	597

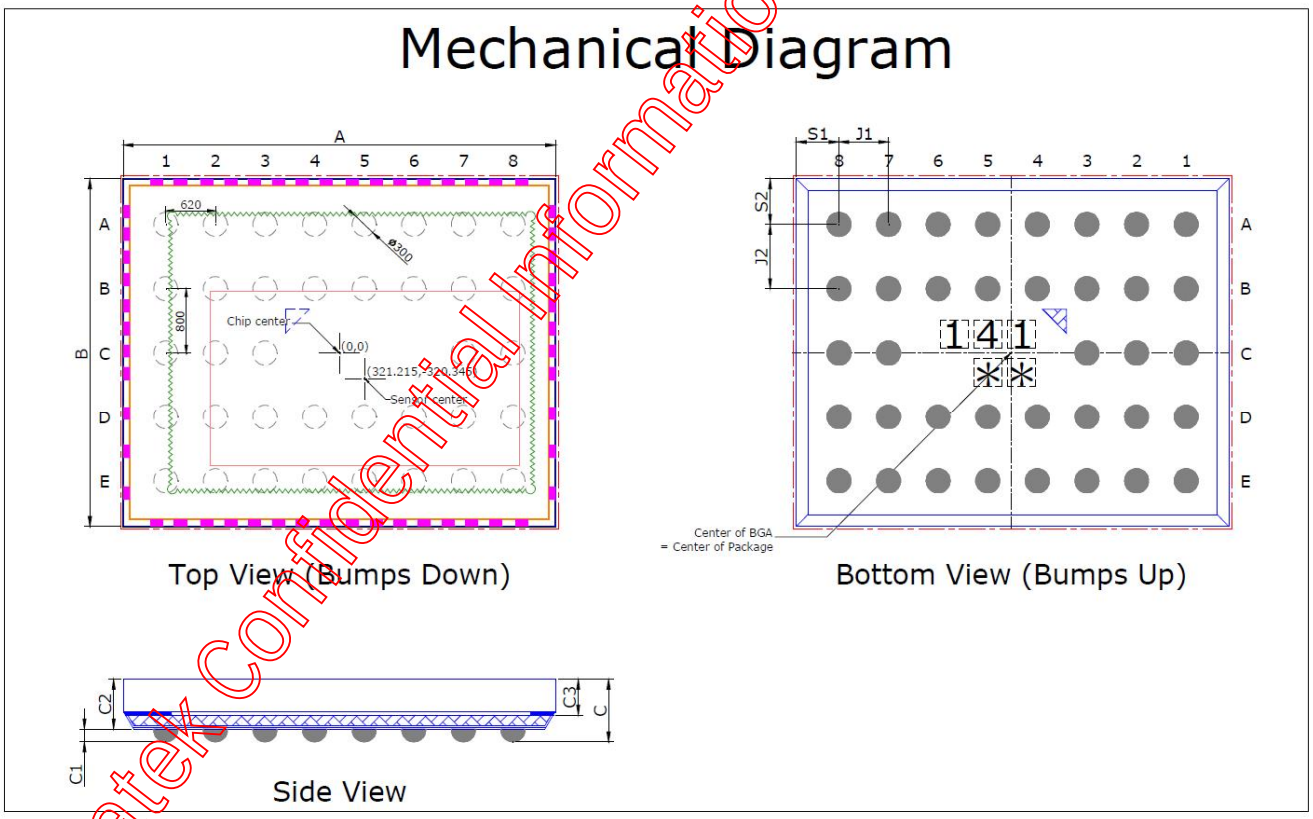


Fig. 3 Package Outline

8. Reference Circuit

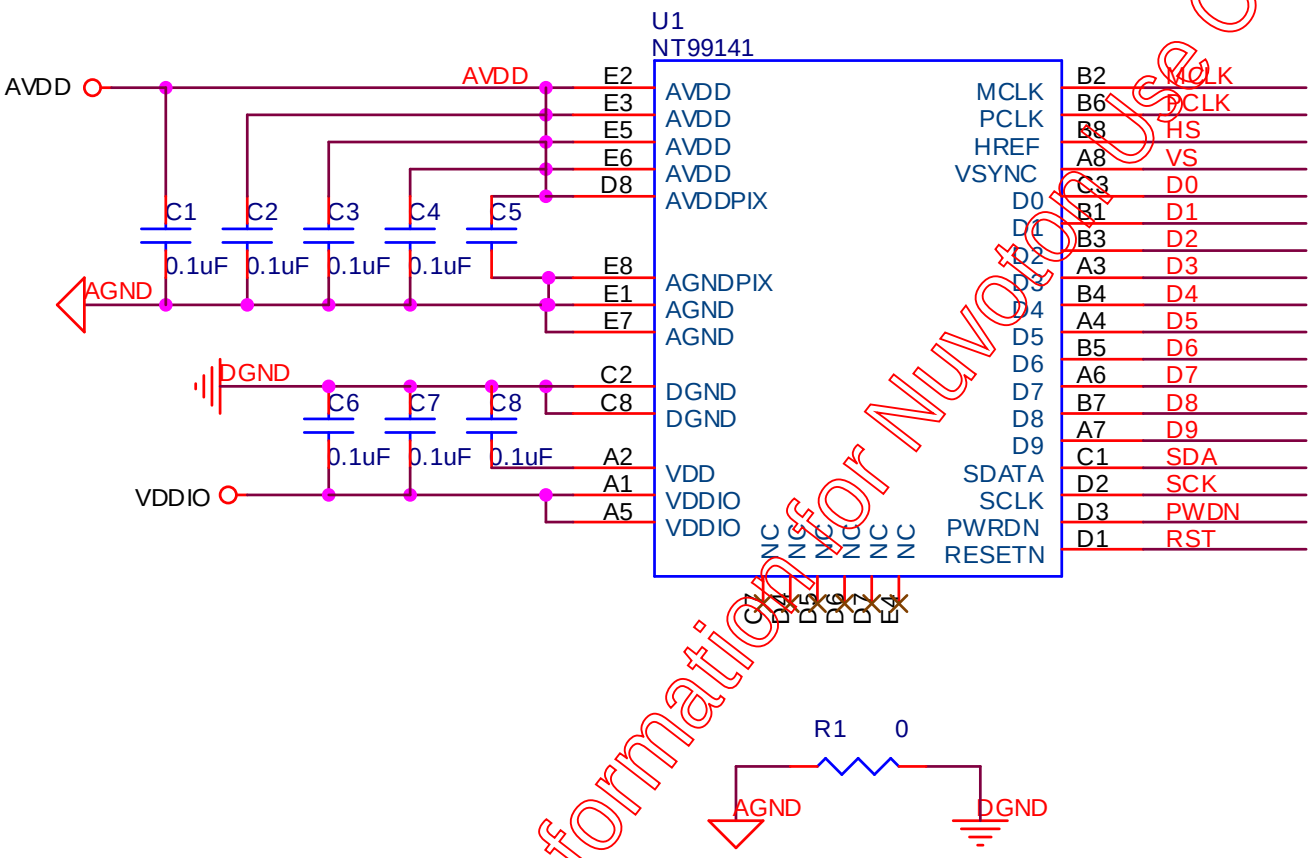


Fig. 4 Reference Circuit

NOTE: VDDIO should be 2.3V or higher when using the internal regulator for digital power VDD

9. Power Sequence

When power is applied to the NT99141, the following power sequences have to follow up.

9.1. Power On Sequence with Internal VDD

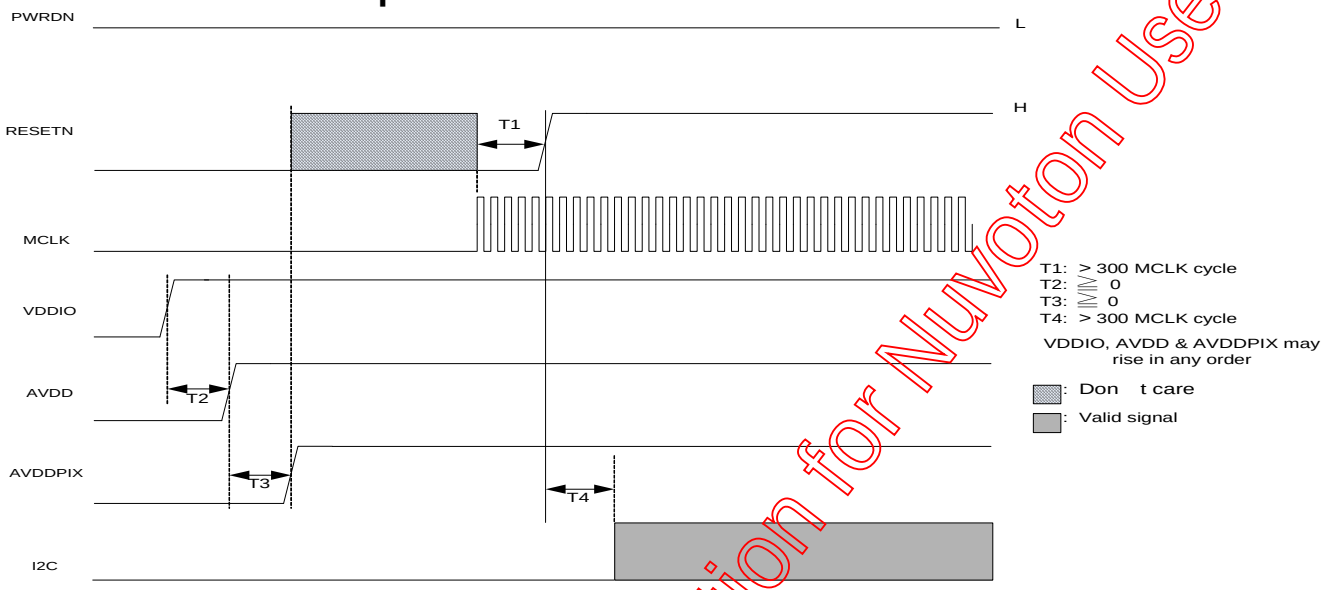


Fig. 5 Power On Sequence with Internal VDD

9.2. Power On Sequence with External VDD

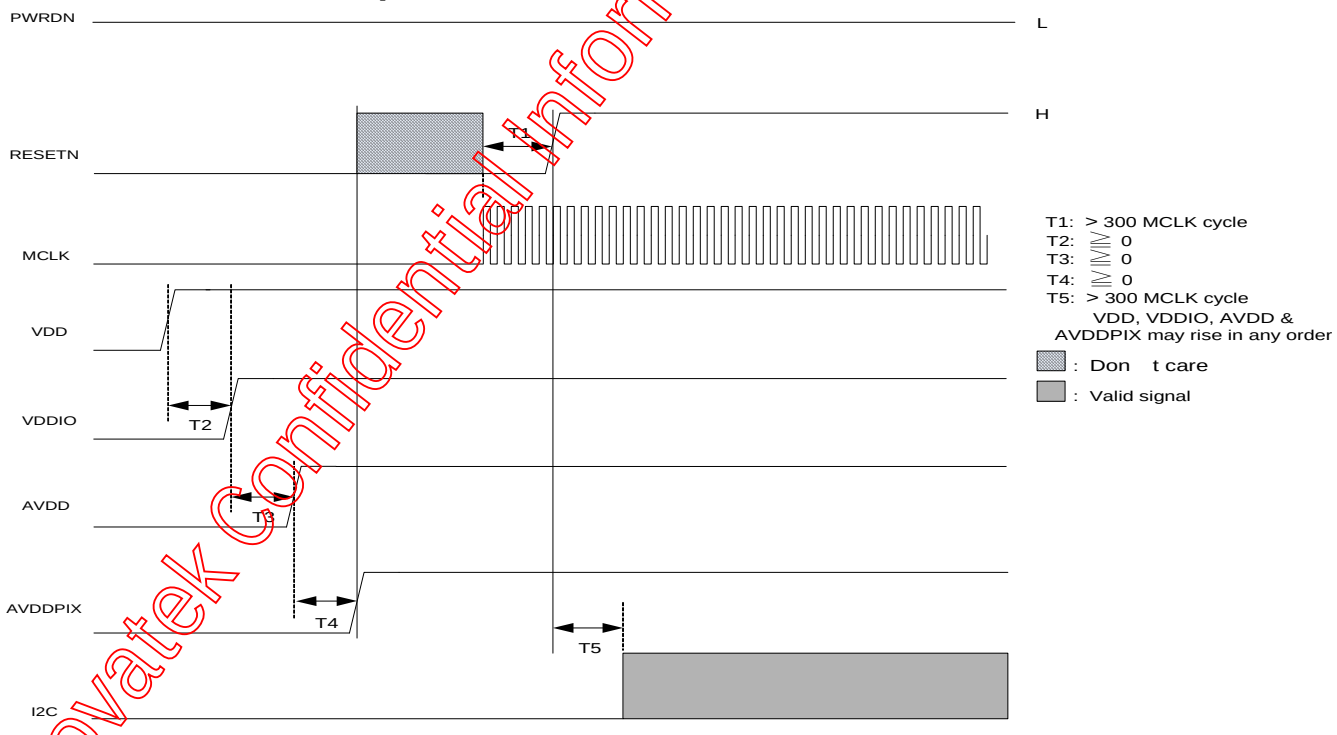


Fig. 6 Power On Sequence with External VDD

9.3. Power Off Sequence with Internal VDD

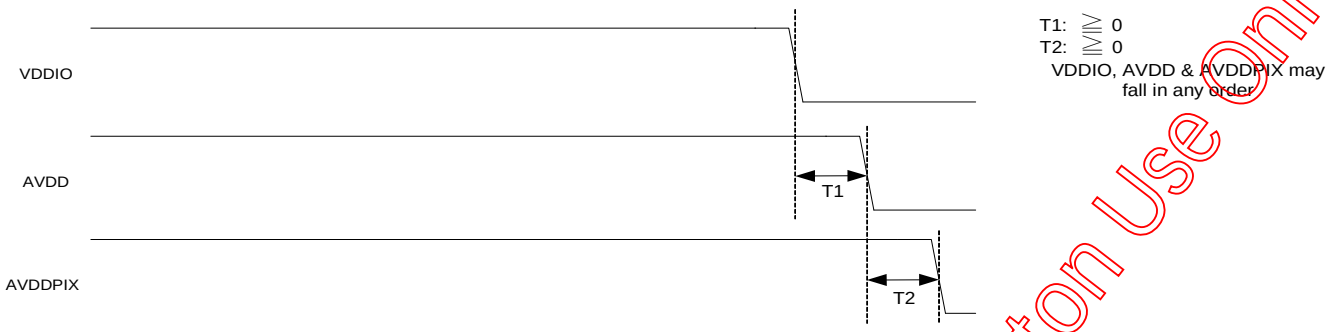


Fig. 7 Power Off Sequence with Internal VDD

9.4. Power Off Sequence with External VDD

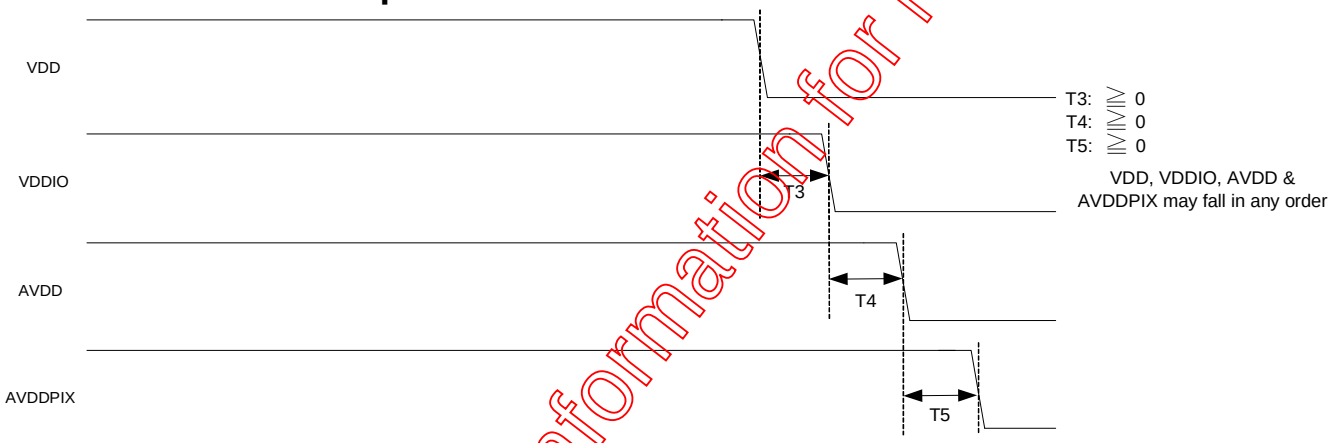


Fig. 8 Power Off Sequence with External VDD

9.5. Power Down Sequence

The NT99141 enter power down mode when PWRDN=”H”. The detail timing sequence, please see the below.

9.5.1. Power Down Sequence with Internal VDD

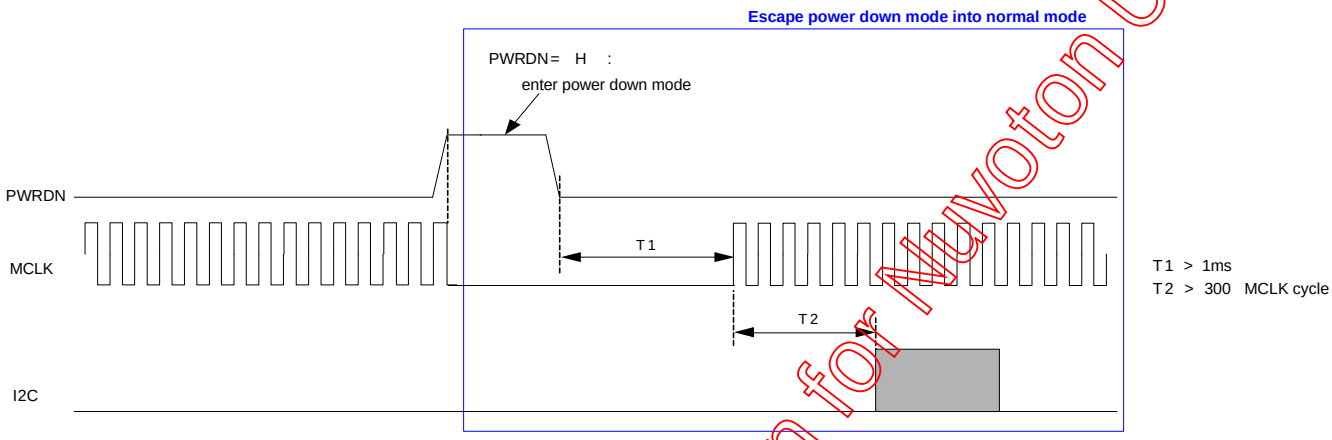


Fig. 9 Power Down Sequence with Internal VDD

9.5.2. Power Down Sequence with External VDD

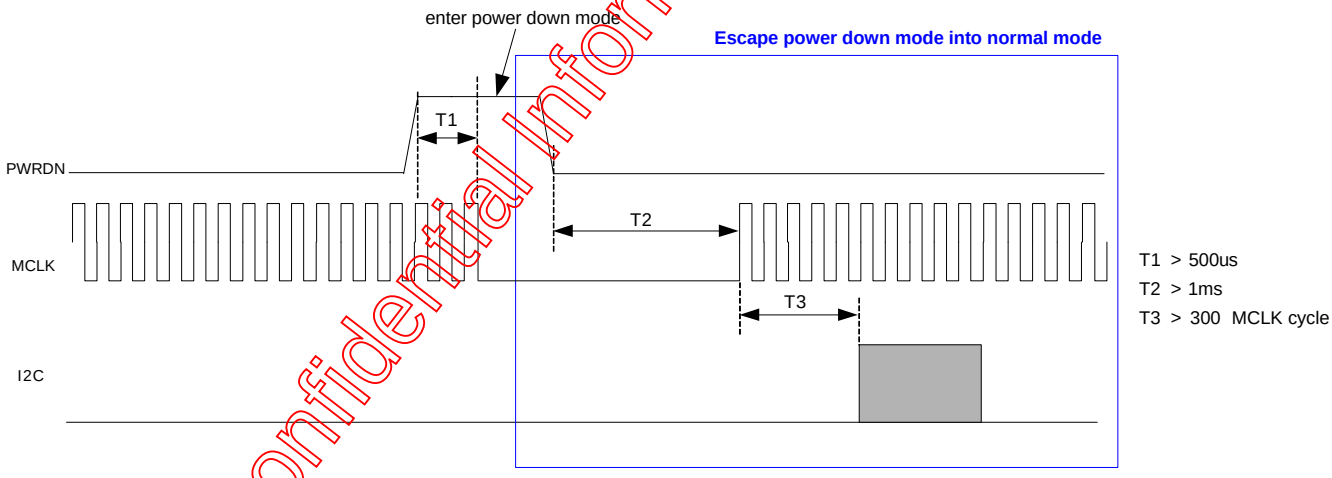


Fig. 10 Power Down Sequence with External VDD

10. Function Description

10.1. Pixel Array

The NT99141, a 1/4” CMOS image sensor with resolution of 1280H x 720V pixels, arranges its CFA (color filter array) as a Bayer pattern, as shown in Fig. 11.

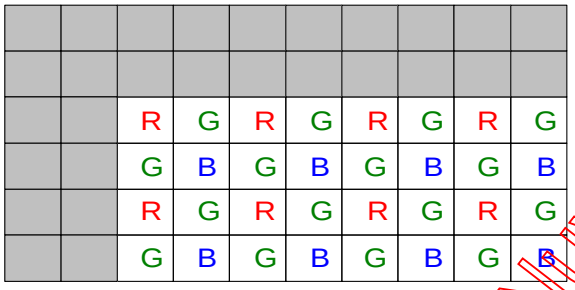


Fig. 11 Color Filter Array Layout

10.2. Default Readout Order

When the image of a scene is projected onto the active surface of the sensor, as shown in Fig. 12錯誤! 找不到參照來源。, the readout direction can be switched by setting the register 0x3022 bit[1:0] to modify the image in such a way that the image becomes mirrored in the horizontal and/or flipped in the vertical direction.

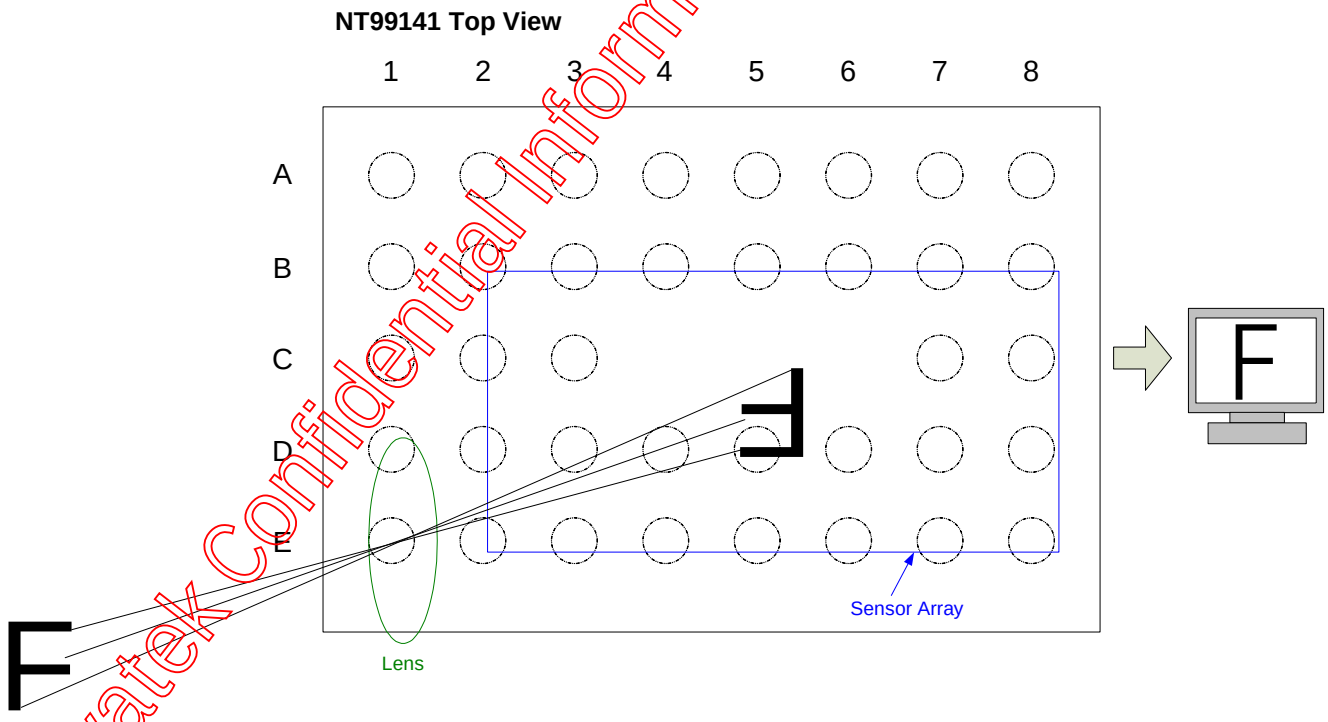


Fig. 12 Default Readout Order

10.3. Analog Gain Control

The amplifier gain can be programmed through the two-wire serial interface.

10.4. 10-Bit ADC

The pixel output signal is digitized using the on-chip 10 bits ADC.

10.5. Image Windowing

Users can program the window size through the two-wire serial interface bus. The NT99141 output data is synchronized with the PCLK output. When HREF is HIGH, individual pixel value is outputted on the 10-bit data bus (D0 ~ D9) at each PCLK period. The pixel clock runs at a frequency rate determined by the sensor's master input clock (MCLK) and internal PLL configuration, where the rising edge of the PCLK signal occurs at one-half of each pixel clock period after the transitions in HREF, VSYNC, and DOUT. (see the below: pixel data timing example / row timing and HREF, VSYNC signals)

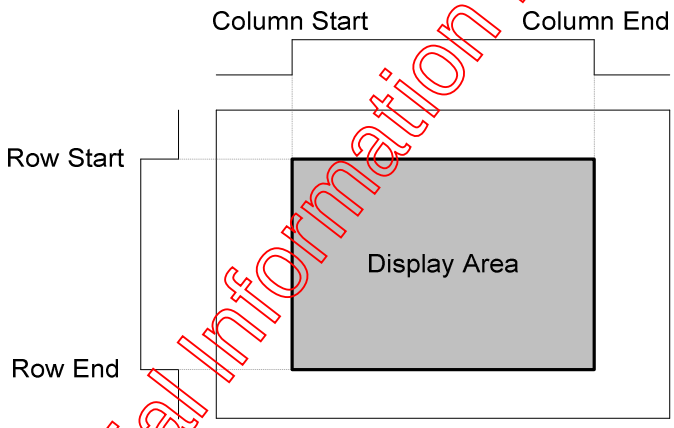


Fig. 13 Image Windowing

Pixel Data Timing Example: (HREF default setting: active high)

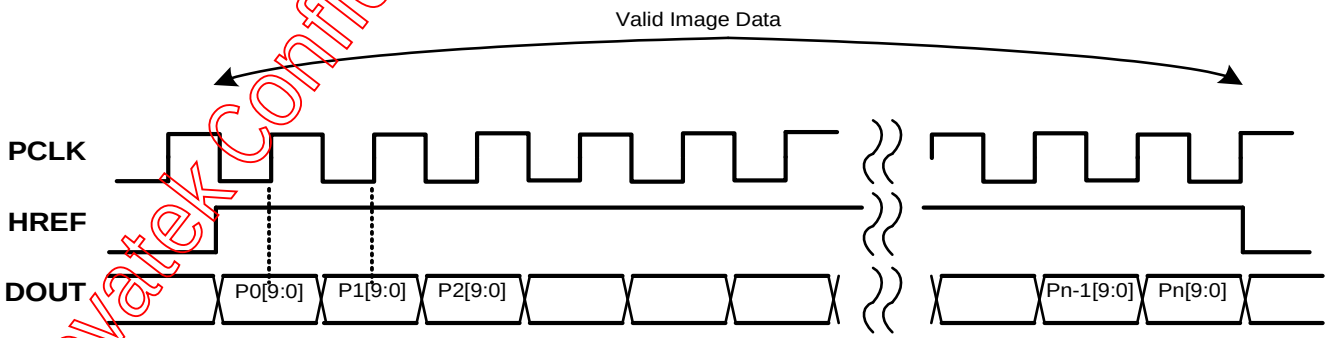


Fig. 14 HREF Timing

Row Timing and HREF / VSYNC signals: (VSYNC default setting: active high)

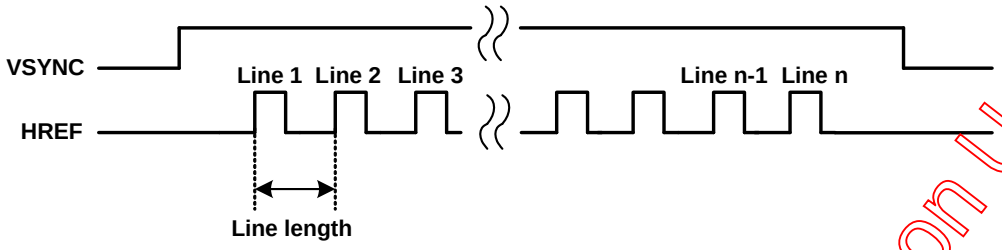


Fig. 15 VSYNC Timing

10.6. Output Format

- YCbCr

Mode	Byte	Byte	Byte	Byte
0x32F0[1] = 0 0x32F0[0] = 0	Cb_i	Y_i	Cr_i	Y_{i+1}
0x32F0[1] = 1 0x32F0[0] = 0	Cr_i	Y_i	Cb_i	Y_{i+1}
0x32F0[1] = 0 0x32F0[0] = 1	Y_i	Cb_i	Y_{i+1}	Cr_i
0x32F0[1] = 1 0x32F0[0] = 1	Y_i	Cr_i	Y_{i+1}	Cb_i

Fig. 16 Output Format -- YCbCr

- RGB565

Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	R7	R6	R5	R4	R3	G7	G6	G5
	2nd	G4	G3	G2	B7	B6	B5	B4	B3
0x32F0[1] = 1 0x32F0[0] = 0	1st	B7	B6	B5	B4	B3	G7	G6	G5
	2nd	G4	G3	G2	R7	R6	R5	R4	R3
0x32F0[1] = 0 0x32F0[0] = 1	1st	G4	G3	G2	B7	B6	B5	B4	B3
	2nd	R7	R6	R5	R4	R3	G7	G6	G5
0x32F0[1] = 1 0x32F0[0] = 1	1st	G4	G3	G2	R7	R6	R5	R4	R3
	2nd	B7	B6	B5	B4	B3	G7	G6	G5

Fig. 17 Output Format -- RGB565

- RGB555

Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	0	R7	R6	R5	R4	R3	G7	G6
	2nd	G5	G4	G3	B7	B6	B5	B4	B3
0x32F0[1] = 1 0x32F0[0] = 0	1st	0	B7	B6	B5	B4	B3	G7	G6
	2nd	G5	G4	G3	R7	R6	R5	R4	R3

Fig. 18 Output Format -- RGB555

- RGB444x

Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	R7	R6	R5	R4	G7	G6	G5	G4
	2nd	B7	B6	B5	B4	0	0	0	0
0x32F0[1] = 1 0x32F0[0] = 0	1st	B7	B6	B5	B4	G7	G6	G5	G4
	2nd	R7	R6	R5	R4	0	0	0	0

Fig. 19 Output Format -- RGB444x

- RGBx444

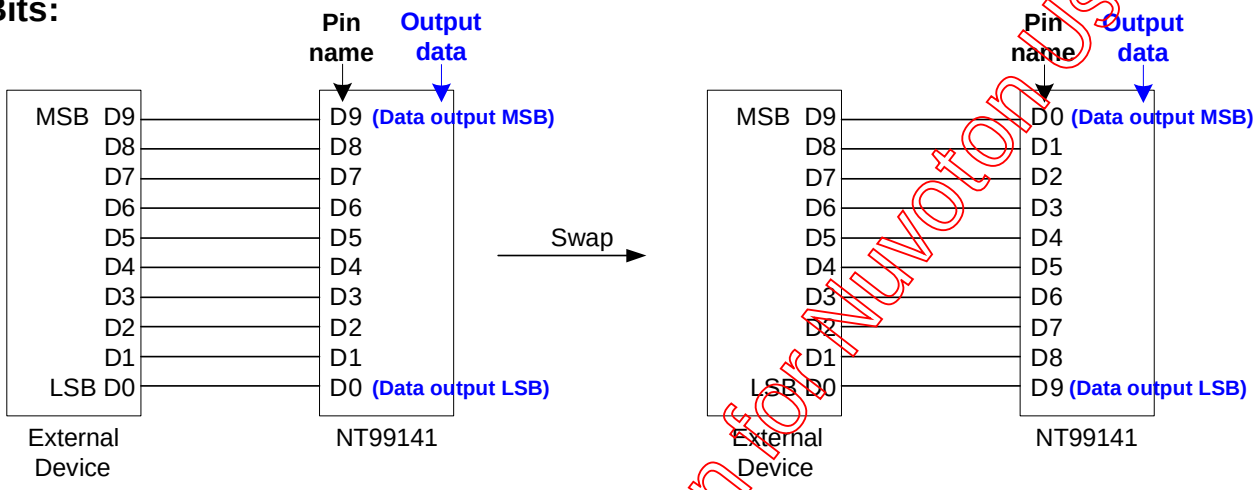
Mode	Byte	D9	D8	D7	D6	D5	D4	D3	D2
0x32F0[1] = 0 0x32F0[0] = 0	1st	0	0	0	0	R7	R6	R5	R4
	2nd	G7	G6	G5	G4	B7	B6	B5	B4
0x32F0[1] = 1 0x32F0[0] = 0	1st	G7	G6	G5	G4	B7	B6	B5	B4
	2nd	0	0	0	0	R7	R6	R5	R4

Fig. 20 Output Format -- RGBx444

10.7. MSB/LSB Swap

The MSB and LSB can be swapped by setting the control register. Fig. 21 shows some examples of connections with external devices.

10 Bits:



8 Bits:

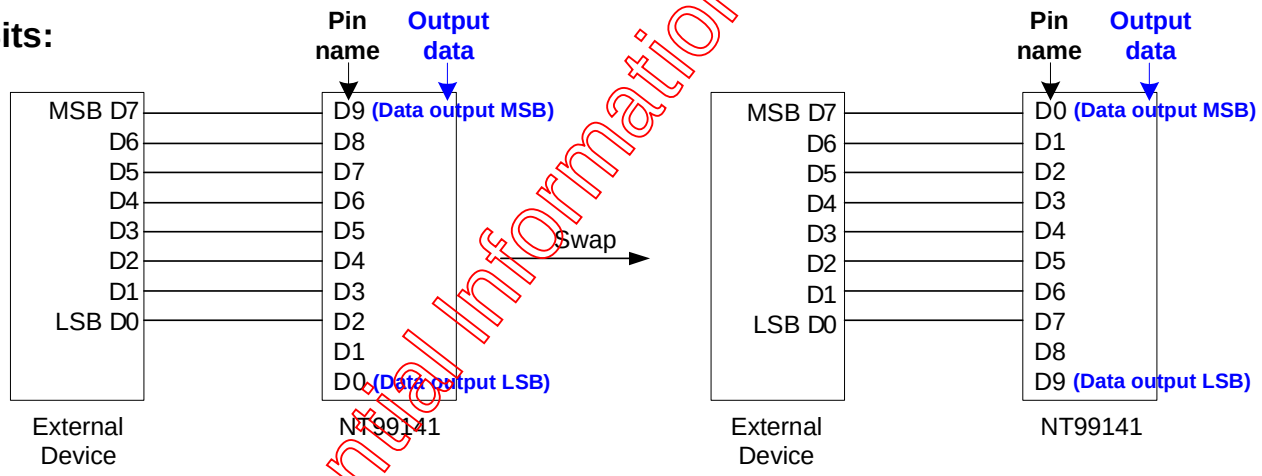


Fig. 21 Examples of Connections with External Devices

10.8. Special Effects

Normal

B/W

Sepia

Negative

Solarization

Fig. 22 Special Effects

10.9. Gamma Correction

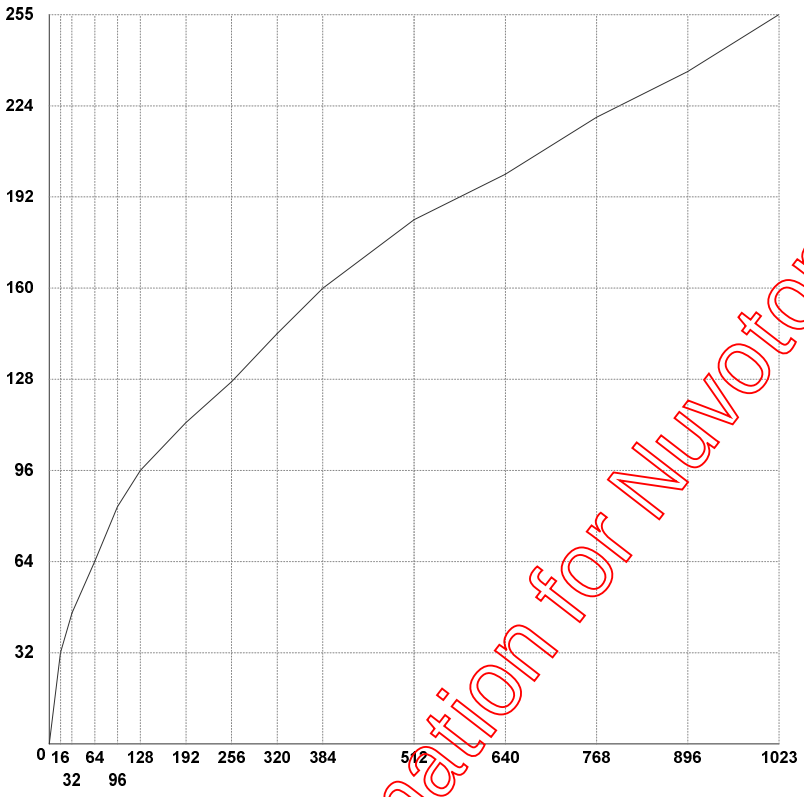


Fig. 23 Gamma Correction

10.10. Luminance Acculation Mode

16 zones with selectable weighting are available for luminance accumulation. Each zone can either weighted by 0, 1, 2 or 3, according to different scenes or requests.

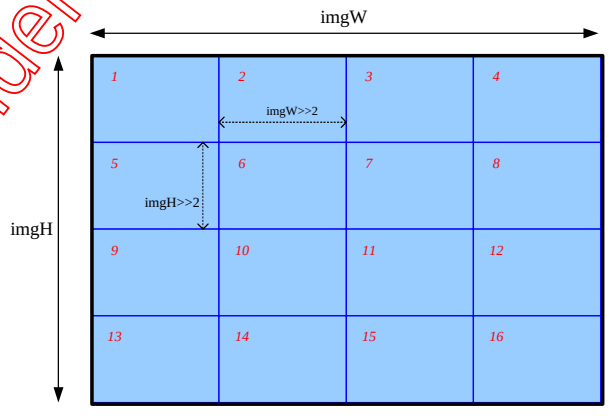


Fig. 24 Luminance Acculation Mode

11. Two-Wire Serial Interface Bus

User can control the register read/write through two-wire serial interface bus. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master device generates a clock MCLK that is an input to the sensor and used to synchronize data transfers. Data is transferred between master and slave on a bi-directional signal SDATA. SDATA must be pull up to VDDIO by a 1.5 k Ω resistor.

Data transfer on the two-wire serial interface bus are performed by a sequence of low level protocol elements:

- a (repeated) start condition
- a slave address / data direction byte
- an (a no) acknowledge bit
- a message byte
- a stop condition

The bus is idle when both SCLK and SDATA are “high”. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

◆ Start condition

A start condition is defined as a high-to-low transition on SDATA while SCLK is “high”. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

◆ Stop condition

A stop condition is defined as a low-to-high transition on SDATA while SCLK is high.

◆ Data transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes. One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is “low” and must be stable while SCLK is “high”.

◆ Slave address / Data direction byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a write, and a “1” indicates a read. The slave addresses used by the NT99141

are **0x54** (write address) and **0x55** (read address).

- Message byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the I2C specification and is defined as part of the MIPI and CSI.

- Acknowledge bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA “low”. As for data transfers, SDATA can change when SCLK is “low” and must be stable while SCLK is “high”.

- No-acknowledge bit

The no-acknowledge bit is generated when the receiver does not drive SDATA “low” during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

- Typical sequence

A typical read or write sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a write, the master then transfers the 16-bit register address to which the write should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a read, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a write request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave’s internal register address is auto-incremented after every 8 bits are transferred. The data transfer is stopped when the

master sends a no-acknowledge bit.

11.1. Single Read from Random Location

This sequence (Fig. 25) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit READ slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a noacknowledge bit followed by a stop condition. Fig. 25 shows how the internal register address maintained by the NT99141 is loaded and incremented as the sequence proceeds.

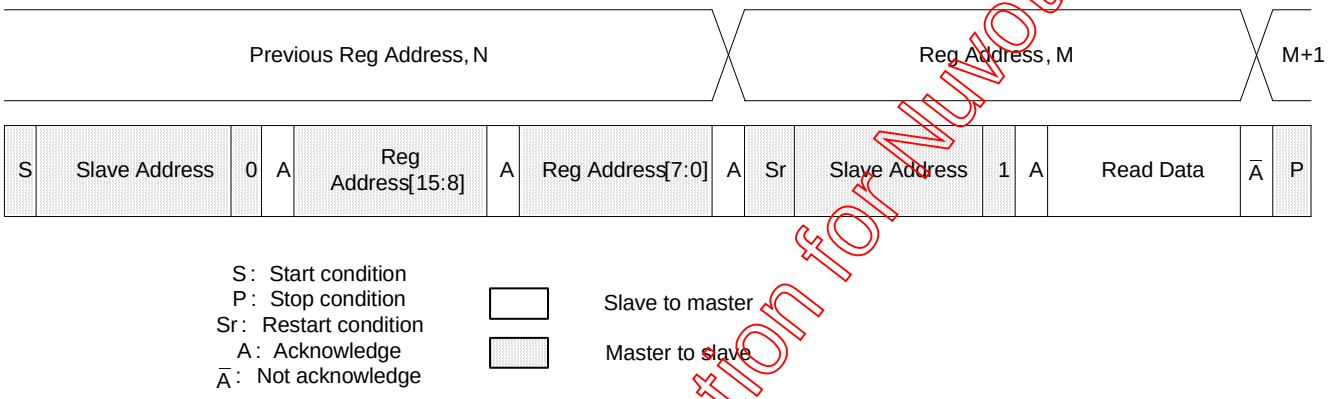


Fig. 25 Single read from random location

11.2. Single Read from Current Location

This sequence (see Fig. 26) performs a READ using the current value of the NT99141 internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

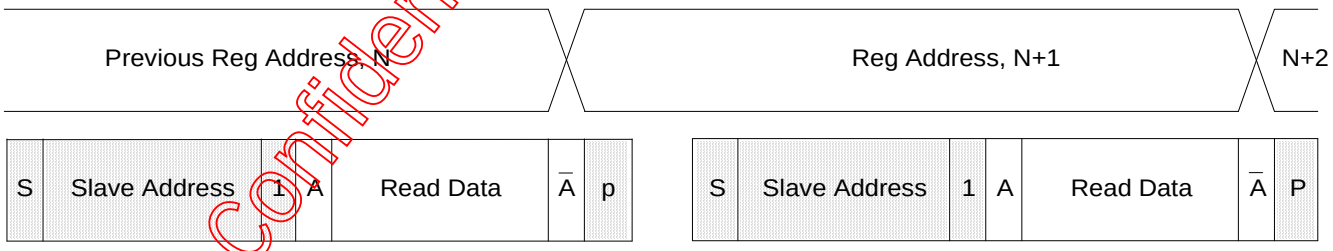


Fig. 26 Single read from current location

11.3. Sequential Read, Start from Random Location

This sequence (Fig. 27) starts in the same way as the single READ from random location (Fig. 25). Instead of

generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

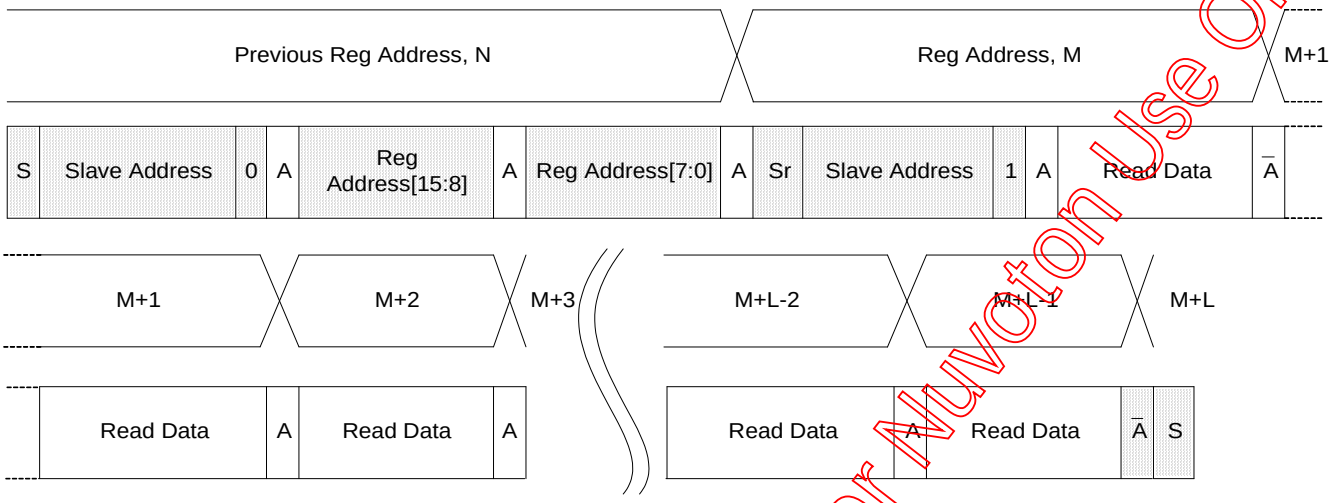


Fig. 27 Sequential read, start from random location

11.4. Sequential Read, Start from Current Location

This sequence (Fig. 28) starts in the same way as the single READ from current location (Fig. 26). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

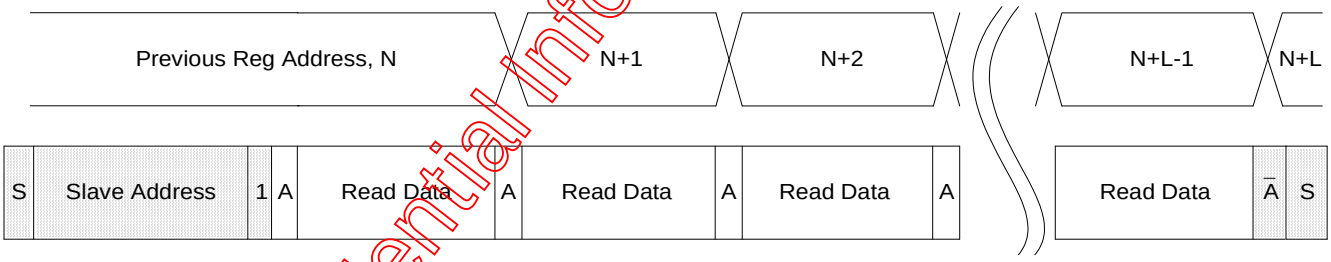


Fig. 28 Sequential read, start from current location

11.5. Single Write to Random Location

This sequence (Fig. 29) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

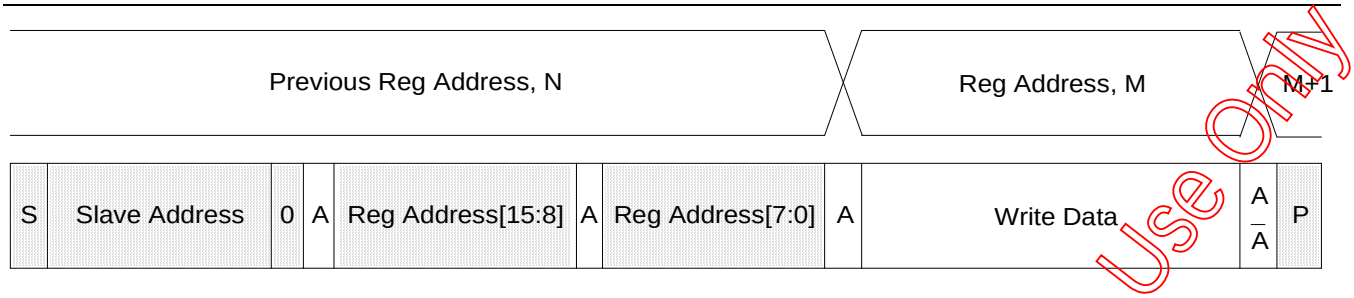


Fig. 29 Single write to random location

11.6. Sequential Write, Start at Random Location

This sequence (Fig. 30) starts in the same way as the single WRITE to random location (Fig. 29). Instead of generating a stop condition after the first byte of data has been transferred, the master continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

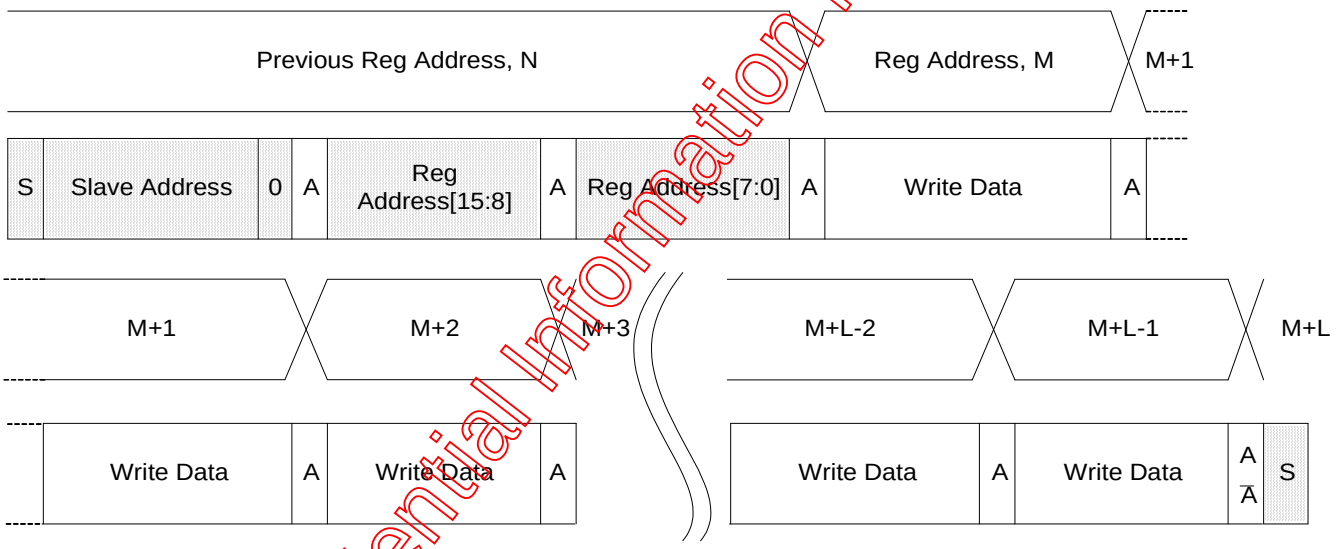


Fig. 30 Sequential write, start at random location

12. JPEG Output Timing

12.1. Valid Mode

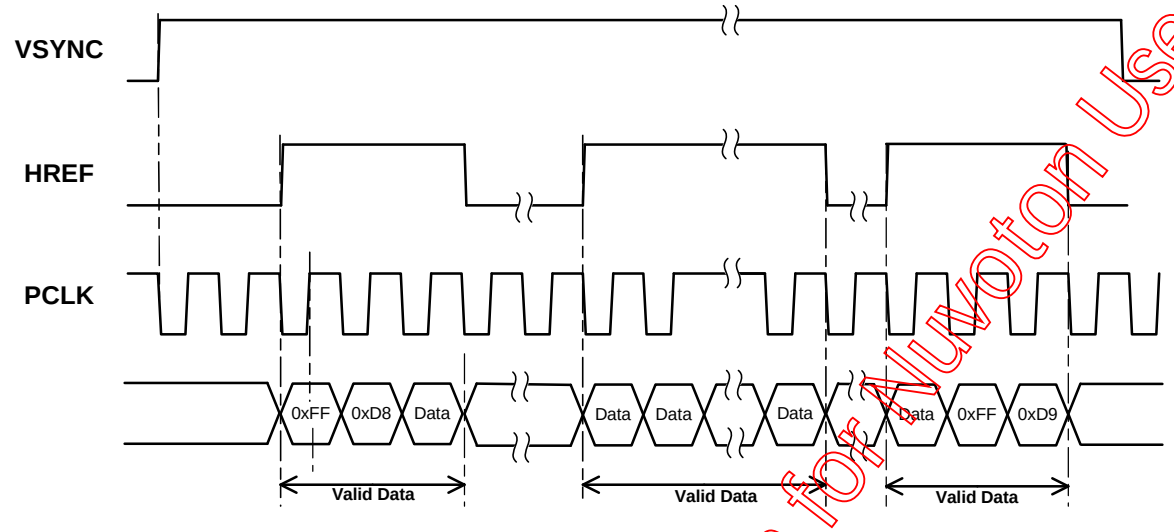


Fig. 31 JPG_Output_Mode = 0

12.2. Frame Mode 0

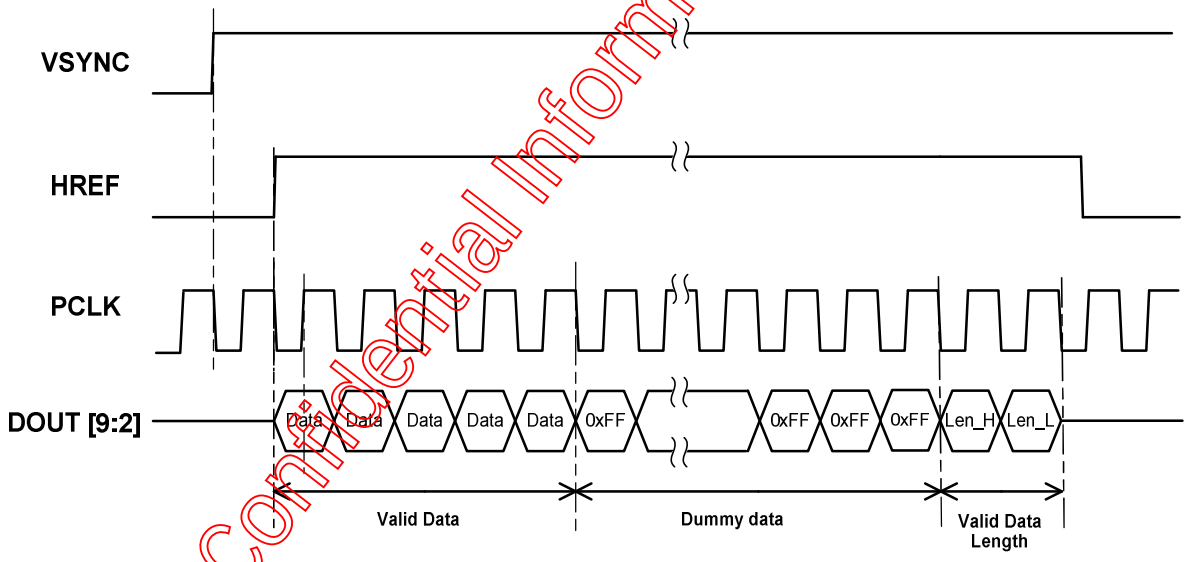


Fig. 32 JPG_Output_Mode = 1

12.3. Frame Mode 1

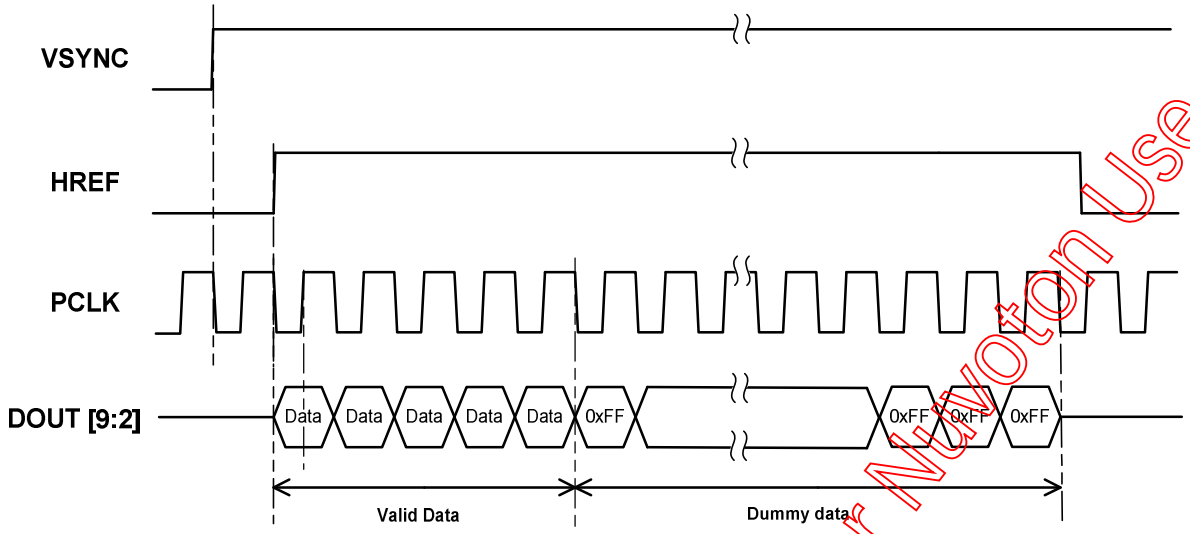


Fig. 33 JPG_Output_Mode = 2

13. CCIR656 Output Timing

Dummy Line

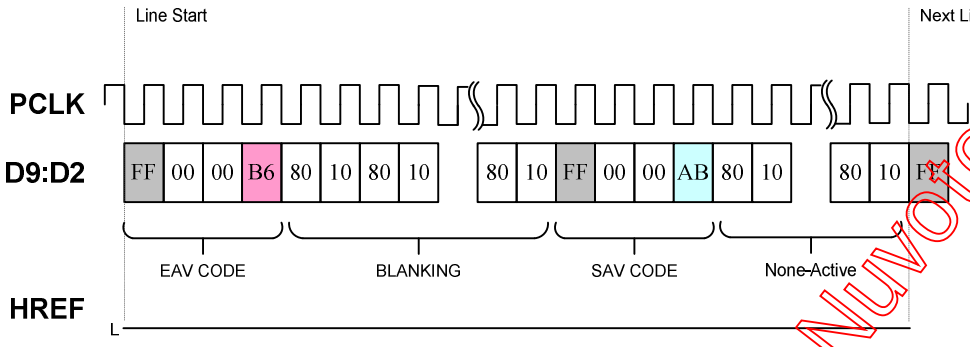


Fig. 34 CCIR656 Output Timing – Dummy Line

Active Line

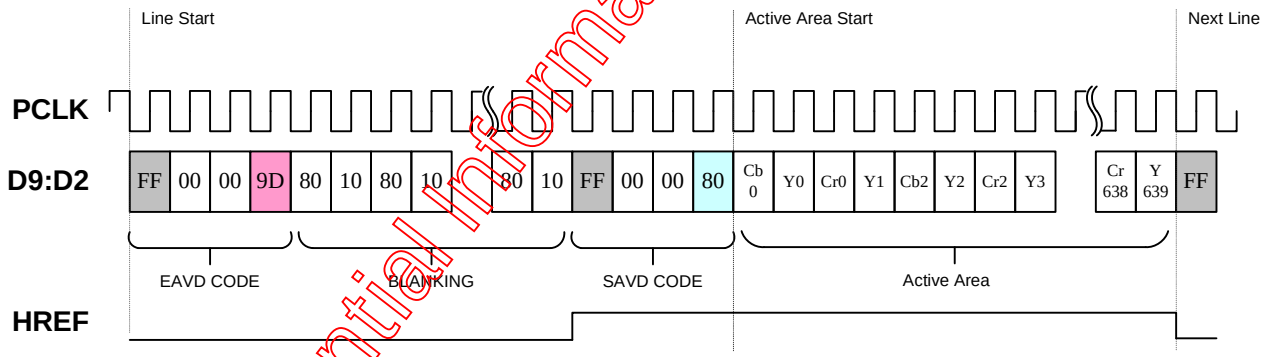


Fig. 35 CCIR656 Output Timing – Active Line

14. Control Registers

The device slave addresses are **0x54** for write and **0x55** for read. The detail control registers are listed as follow.

14.1. Sensor Control Registers (0x3000)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
					Chip_Version [15:0]
0x3000	Chip_Version_H	7:0	R	0x14	bit [15:4] is chip number bit [3:0] is version
0x3001	Chip_Version_L	7:0	R	0x10	
					X_Addr_Start [10:0] †
0x3002	X_Addr_Start_H	2:0	R/W	0x0	The first column of visible pixels to be read out. Even only. (**minimum setting 0x02**)
0x3003	X_Addr_Start_L	7:0	R/W	0x00	
					Y_Addr_Start [10:0] †
0x3004	Y_Addr_Start_H	1:0	R/W	0x00	The first row of visible pixels to be read out. Even only. (**minimum setting 0x02**)
0x3005	Y_Addr_Start_L	7:0	R/W	0x00	
					X_Addr_End [10:0] †
0x3006	X_Addr_End_H	2:0	R/W	0x04	The last column of visible pixels to be read out. Odd only. (**maximum setting 0x505**)
0x3007	X_Addr_End_L	7:0	R/W	0xFF	
					Y_Addr_End [10:0] †
0x3008	Y_Addr_End_H	1:0	R/W	0x02	The last row of visible pixels to be read out. Odd only. (**maximum setting 0x2D5**)
0x3009	Y_Addr_End_L	7:0	R/W	0xCF	
					Line_Length_Pck [15:0] †
0x300A	Line_Length_Pck_H	7:0	R/W	0x08	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time.
0x300B	Line_Length_Pck_L	7:0	R/W	0x24	
					Frame_Length_Line [15:0] †
0x300C	Frame_Length_Line_H	7:0	R/W	0x04	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines.
0x300D	Frame_Length_Line_L	7:0	R/W	0xC0	
					X_Output_Size [10:0] †
0x300E	X_Output_Size_H	2:0	R/W	0x05	Set output size of x direction for display image. The maximum size is (X_Addr_End - X_Addr_Start + 1). If the Scaling down is disable, this size is final size.
0x300F	X_Output_Size_L	7:0	R/W	0x00	
					Y_Output_Size [10:0] †
0x3010	Y_Output_Size_H	1:0	R/W	0x02	Set output size of y direction for display image. The maximum size is (Y_Addr_End - Y_Addr_Start + 1) If the Scaling down is disable, this size is final size.
0x3011	Y_Output_Size_L	7:0	R/W	0xD0	
					Integration_Time [15:0] †
0x3012	Integration_Time_H	7:0	R/W	0x00	T_{ex} = (Exposure [15:0] + 1) * Row_time
0x3013	Integration_Time_L	7:0	R/W	0x01	
0x3014	DGain_R	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.

0x3015	AGain_R	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x3016	DGain_Gr	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x3017	AGain_Gr	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x3018	DGain_Gb	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x3019	AGain_Gb	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x301A	DGain_B	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x301B	AGain_B	6:0	R/W	0x00	AGain = Gain1 * Gain2 Gain1 = (1 + bit [6]) *(1 + bit [5]) * (1 + bit [4]) Gain2 = (1 + (bit [3:0] + 1) / 16)
0x301C	Global_DGain	1:0	R/W	0x00	Digital gain (bit [1] + 1) * (bit [0] + 1) * Analog gain.
0x301D	Global_AGain	6:0	R/W	0x00	Writing a gain to this register is equivalent to writing code to each gain.
0x301E	-	-	-	-	Reserved
0x301F	-	-	-	-	Reserved
0x3020	-	-	-	-	Reserved
0x3021	Reset_Register	7:0	R/W	0x00	
	Output_Bit_Swap	7	R/W	0	Output bit swap, swap MSB and LSB. 0: Disable 1: Enable.
	Clock_Output_TriState	6	R/W	1	Clock output Tri-state 0: Output clock pin will keep the last status before sensor standby mode. 1: Output clock pin will be tri-stated during standby mode.
	Data_Output_TriState	5	R/W	1	Data output Tri-state 0: Output data pins (VSYNC, HREF) will keep last status before sensor standby mode. 1: Output data pins will be tri-stated during standby mode.
	-	4:2	-	-	Reserved
	Output_Mode_Sel	1	R/W	0	Output mode select (Start) 1: Streaming. 0: Standby
	Reset	0	R/W	0	Reset Hardware clear. Setting this bit to initiates a reset sequence.
0x3022	Read_Mode_0	7:0	R/W	0x24	
	Y_Even_Inc	7:5	R/W	1	Increment applied to even addresses in Y (row) direction † 1: Normal readout

	X_Even_Inc	4:2	R/W	1	Increment applied to even addresses in X (column) direction † 1: Normal readout
	Mirror_Horizontal	1	R/W	0	Horizontal mirror 0: Normal readout 1: Mirror readout
	Flip_Vertical	0	R/W	0	Vertical flip 0: Normal readout 1: Flip readout
0x3023	Read_Mode_1	7:0	R/W	0x24	
	Y_Odd_Inc	7:5	R/W	1	Increment applied to odd addresses in Y (row) direction † 1: Normal readout 3: 1/2x 5: 1/3x 7: 1/4x
	X_Odd_Inc	4:2	R/W	1	Increment applied to odd addresses in X (column) direction † 1: Normal readout 3: 1/2x 5: 1/3x 7: 1/4x
	-	1	-	-	Reserved
	X_Bin_En	0	R/W	0	Enable analog binning in X directions. When set, X_Odd_Inc must be set to 3. X_Even_Inc = Y_Even_Inc = Y_Odd_Inc = 1.
0x3024	Read_Mode_2	7:0	R/W	0x00	
	Show_Vert_Dark_Pix	6	R/W	0	Show vertical dark pixel 0: Don't show dark pixel. 1: Show dark pixel. The VREF is asserted early.
	-	5:4	R	0	Reserved
	Pclk_Edge_Sel	3	R/W	0	PCLK edge selection 0: Data valid on PCLK rising edge 1: Data valid on PCLK falling edge.
	Pclk_Output_Sel	2	R/W	0	PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF.
	VSync_Inverse	1	R/W	0	VSYNC inverse 0: Active high 1: Active low
	HREF_Inverse	0	R/W	0	HREF inverse 0: Active high 1: Active low
0x3025	Pattern_Mode	7:0	R/W	0x10	
	-	7:4	-	-	Reserve
	Pattern_Mode_Sel	3:0	R/W	0	Pattern select 0: Normal operation: no test pattern 1: Reserve

					2: 100% Color bars 3: PN10 4: Reserve Pattern size depend on X_Output_Size and Y_Output_Size.
0x3026	PN10_Value	7:0	R/W	0x10	PN10_Value [9:0]
	-	7:4	-	-	Reserved
	PN10_Value_H	1:0	R/W	0x00	
0x3027	PN10_Value_L	7:0	R/W	0x00	When PN10 is enabled, this byte is random value.
0x3028	PLL_CTRL1	5:0	R/W	0x0f	
	PLL_M	5:0	R/W	0x0f	PLL_M
0x3029	PLL_CTRL2	5:0	R/W -	0x10	
	PLL_N	5:4	R/W	1	PLL_N
	-	3	R	0	Reserved
	PLL_P	2:0	R/W	0	PLL_P
0x302A	PLL_CTRL3	6:0	R/W	0x20	
	PLL_Rst	6	R/W	0	0: Normal 1: Reset PLL
	PLL_Pwdn	5	R/W	1	When seting Output_Mode_Sel = 1 (stream out), then PLL_Pwdn = 0 0: Disable 1: Enable
	PLL_Bypass	4	R/W	0	0: Normal (Internal clock using PLL_PCLK) 1: Bypass (External clock using Ext_PCLK)
	PLL_PCLK	3:2	R/W	0	0: PCLK = (PLL_CKOUT) 1: PCLK = (PLL_CKOUT) / 2 2: PCLK = (PLL_CKOUT) / 4 3: PCLK = (PLL_CKOUT) / 8
	Ext_PCLK	1:0	R/W	0	External clock setting 0: PCLK = (CLK_SRC) 1: PCLK = (CLK_SRC) / 2 2: PCLK = (CLK_SRC) / 4 3: PCLK = (CLK_SRC) / 8
0x302B	-	-	-	-	Reserved
0x302C	-	-	-	-	Reserved
0x302D	-	-	-	-	Reserved
0x302E	-	-	-	-	Reserved
0x302F	-	-	-	-	Reserved
0x3030	-	-	-	-	Reserved
0x3031	-	-	-	-	Reserved
0x3032	-	-	-	-	Reserved
0x3033	-	-	-	-	Reserved
0x3034	-	-	-	-	Reserved
0x3035	-	-	-	-	Reserved

0x3036	-	-	-	-	Reserved
0x3037	-	-	-	-	Reserved
0x3038	-	-	-	-	Reserved
0x3039	-	-	-	-	Reserved
0x303A	-	-	-	-	Reserved
0x303B	-	-	-	-	Reserved
0x303C	-	-	-	-	Reserved
0x303D	-	-	-	-	Reserved
0x303E	-	-	-	-	Reserved
0x303F	-	-	-	-	Reserved
0x3040	Calibration_Control_0	2:0	R/W	0x02	
	LSC_Clamp_En	2	R/W	0	0: Disable 1: Enable
	Clamp_En	1	R/W	1	0: Disable 1: Enable
	-	0	R	-	Reserved
0x3041	Calibration_Control_1	4:0	R/W	0x00	
	-	4	R	-	Reserved
	BLC_Sampled_Pixel	3:2	R/W	0	The number of pixel to be sampled for ABLC and DBLC.
	DBLC_En	1	R/W	0	Digital black level calibration enable 0: Disable 1: Enable
	ABLC_Manual_En	0	R/W	0	Manual calibration enable 0: Auto calibration 1: Manual calibration
0x3042	ABLC_Thr_Top	7:0	R/W	0x50	Top threshold for black level
0x3043	ABLC_Thr_Bottom	7:0	R/W	0x14	Bottom threshold for black level
					ABLC_Ofs_R [9:0]
0x3044	ABLC_Ofs_R_H	1:0	R/W	0x02	DAC offset cancellation: x [9:0]
0x3045	ABLC_Ofs_R_L	7:0	R/W	0x00	
					ABLC_Ofs_Gr [9:0]
0x3046	ABLC_Ofs_Gr_H	1:0	R/W	0x02	DAC offset cancellation: x [9:0]
0x3047	ABLC_Ofs_Gr_L	7:0	R/W	0x00	
					ABLC_Ofs_Gb [9:0]
0x3048	ABLC_Ofs_Gb_H	1:0	R/W	0x02	DAC offset cancellation: x [9:0]

0x3049	ABLC_Ofs_Gb_L	7:0	R/W	0x00	
					ABLC_Ofs_B [9:0]
0x304A	ABLC_Ofs_B_H	1:0	R/W	0x02	DAC offset cancellation: x [9:0]
0x304B	ABLC_Ofs_B_L	7:0	R/W	0x00	
0x304C	ABLC_Avg_R	7:0	R	-	Black level average of R pixels
0x304D	ABLC_Avg_Gr	7:0	R	-	Black level average of Gr pixels
0x304E	ABLC_Avg_Gb	7:0	R	-	Black level average of Gb pixels
0x304F	ABLC_Avg_B	7:0	R	-	Black level average of B pixels
0x3050	OB_Top_Thr	7:0	R/W	0xFF	Optical Black Threshold If (pixel value < OB_Thr), take this pixel into account.
0x3051	-	-	-	-	Reserved
0x3052	Optical_Black_Weight_0	7:0	R/W	0xF0	
	ABLC_GainW	7:4	R/W	0xF	Avg = Avg * (ABLC_GainW + 1) / 16
	-	3:0	R-	0	Reserved
0x3053	Optical_Black_Weight_1	7:0	R/W	0x10	
	-	7:6	R	0	Reserved
	-	5	R	-	Reserved
	OB_MUL	4:0	R/W	0x10	The multiplier of optical black
0x3054	OB_OFS	7:0	R/W	0	OB Offset
0x3055	-	-	-	-	Reserved
0x3056	-	-	-	-	Reserved
0x3057	-	-	-	-	Reserved
0x3058	-	-	-	-	Reserved
0x3059	-	-	-	-	Reserved
0x305A	-	-	-	-	Reserved
0x305B	OB_AVG_R	7:0	R	-	Optical Black Average of R
0x305C	OB_AVG_GR	7:0	R	-	Optical Black Average of Gr
0x305D	OB_AVG_GB	7:0	R	-	Optical Black Average of Gb
0x305E	OB_AVG_B	7:0	R	-	Optical Black Average of B
0x305F	-	-	-	-	Reserved
0x3060	Reg_Activate_Ctrl	1:0	R/W	0x00	Activate setting for specified registers. Auto Clear
0x3061	-	-	-	-	Reserved
0x3062	-	-	-	-	Reserved
0x3063	-	-	-	-	Reserved
0x3064	-	-	-	-	Reserved
0x3065	-	-	-	-	Reserved

0x3066	-	-	-	-	Reserved
0x3067	-	-	-	-	Reserved
0x3068	Pad_Config_Serial_IO	7:0	R/W	0x00	
	-	7:2	R	0	Reserved
	Sio_Odrv	1:0	R/W	0	Output driving 0: 2 mA 1: 4 mA 2: 6 mA 3: 8 mA
0x3069	Pad_Config_Pix_Out	7:0	R/W	0x0	D0~D9, VSYNC, HREF
	-	7:2	R	0	Reserved
	PixOut_Odrv	1:0	R/W	0	Output driving 0: 2 mA 1: 4 mA 2: 6 mA 3: 8 mA
0x306A	Pad_Config_PCLKt	7:0	R/W	0x0	PCLK
	-	7:2	R	0	Reserved
	Pclk_Odrv	1:0	R/W	0	Output driving 0: 2 mA 1: 4 mA 2: 6 mA 3: 8 mA

† New register values are accepted by enabling LOAD bit in register 0x3060.

14.2. SOC Control Registers (0x3200)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3200	Mode_Control_0	5:0	R/W	0x10	
	LSC_En	5	R/W	0	Lens shading correction enable 0: Disable 1: Enable
	Gamma_En	4	R/W	1	Gamma correction enable 0: Disable 1: Enable
	Color_Gain_En	3	R/W	0	Color gain enable 0: Disable 1: Enable
	Color_Accmu_En	2	R/W	0	Color accumulation enable 0: Disable 1: Enable
	Lum_Accmu_En	1	R/W	0	Luminance accumulation enable 0: Disable 1: Enable
0x3201	Mode_Control_1	6:0	R/W	0x0F	
	Scaling_Down_En	6	R/W	0	Scaling down enable 0: Disable 1: Enable
	AE_En	5	R/W	0	Auto-exposure enable 0: Disable 1: Enable
	AWB_En	4	R/W	0	Auto-white balance enable 0: Disable 1: Enable
	Noise_Reduction_En	3	R/W	1	Noise reduction enable 0: Disable 1: Enable
	Edge_Enhance_En	2	R/W	1	Edge enhancement enable 0: Disable 1: Enable
	Color_Correct_En	1	R/W	1	Color correction and transform enable 0: Disable 1: Enable
	Special_Effect_En	0	R/W	1	Special effects enable 0: Disable 1: Enable

14.3. SOC Lens Shading Correction Registers (0x3210)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3210	LSC_R_Gain0	6:0	R/W	0x00	Gain0 of R
0x3211	LSC_R_Gain1	6:0	R/W	0x00	Gain1 of R
0x3212	LSC_R_Gain2	6:0	R/W	0x00	Gain2 of R
0x3213	LSC_R_Gain3	6:0	R/W	0x00	Gain3 of R
0x3214	LSC_Gr_Gain0	6:0	R/W	0x00	Gain0 of Gr
0x3215	LSC_Gr_Gain1	6:0	R/W	0x00	Gain1 of Gr
0x3216	LSC_Gr_Gain2	6:0	R/W	0x00	Gain2 of Gr
0x3217	LSC_Gr_Gain3	6:0	R/W	0x00	Gain3 of Gr
0x3218	LSC_Gb_Gain0	6:0	R/W	0x00	Gain0 of Gb
0x3219	LSC_Gb_Gain1	6:0	R/W	0x00	Gain1 of Gb
0x321A	LSC_Gb_Gain2	6:0	R/W	0x00	Gain2 of Gb
0x321B	LSC_Gb_Gain3	6:0	R/W	0x00	Gain3 of Gb
0x321C	LSC_B_Gain0	6:0	R/W	0x00	Gain0 of B
0x321D	LSC_B_Gain1	6:0	R/W	0x00	Gain1 of B
0x321E	LSC_B_Gain2	6:0	R/W	0x00	Gain2 of B
0x321F	LSC_B_Gain3	6:0	R/W	0x00	Gain3 of B
					LSC_CenterX_R[9:0]
0x3220	LSC_CenterX_R_H	1:0	R/W	0x01	The X-dimension of the brightest point of R
0x3221	LSC_CenterX_R_L	7:0	R/W	0x40	
					LSC_CenterX_Gr[9:0]
0x3222	LSC_CenterX_Gr_H	1:0	R/W	0x01	The X-dimension of the brightest point of Gr
0x3223	LSC_CenterX_Gr_L	7:0	R/W	0x40	
					LSC_CenterX_Gb[9:0]
0x3224	LSC_CenterX_Gb_H	1:0	R/W	0x01	The X-dimension of the brightest point of Gb
0x3225	LSC_CenterX_Gb_L	7:0	R/W	0x40	
					LSC_CenterX_B[9:0]
0x3226	LSC_CenterX_B_H	1:0	R/W	0x01	The X-dimension of the brightest point of B
0x3227	LSC_CenterX_B_L	7:0	R/W	0x40	
					LSC_CenterY_R[8:0]
0x3228	LSC_CenterY_R_H	0	R/W	0x00	The Y-dimension of the brightest point of R
0x3229	LSC_CenterY_R_L	7:0	R/W	0XB4	
					LSC_CenterY_Gr[8:0]
0x322A	LSC_CenterY_Gr_H	0	R/W	0x00	The Y-dimension of the brightest point of Gr
0x322B	LSC_CenterY_Gr_L	7:0	R/W	0xB4	
					LSC_CenterY_Gb[8:0]

0x322C	LSC_CenterY_Gb_H	0	R/W	0x00	The Y-dimension of the brightest point of Gb
0x322D	LSC_CenterY_Gb_L	7:0	R/W	0xB4	
					LSC_CenterY_B[8:0]
0x322E	LSC_CenterY_B_H	0	R/W	0x00	The Y-dimension of the brightest point of B
0x322F	LSC_CenterY_B_L	7:0	R/W	0xB4	
0x3230					Reserved
0x3231	LSC_EV_Bot	7:0	R/W	0xC0	LSC bottom EV boundary
0x3232	LSC_Shf_Ctrl	7:0	R/W	0xC3	
	LSC_Shf_Slope	7:6	R/W	3	Slope shift bit
	LSC_Shf_Gain	2:0	R/W	3	Gain Shift bit

14.4. SOC Statistic Registers (0x3250)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3250	Color_Acc_Ctrl	7:0	R/W	0x80	
	CA_Zone_En	7	R/W	1	Enable color acc zone mode
	CA_Zone_Mode	6	R/W	0	Zone mode 0: when CA_Zone_Cnt = 0, keep current setting 1: when CA_Zone_Cnt = 0, statistic the whole image
	-	5:0	R	-	Reserved
0x3251	-	-	-	-	Reserved
0x3252	-	-	-	-	Reserved
0x3253	-	-	-	-	Reserved
0x3254	-	-	-	-	Reserved
0x3255	-	-	-	-	Reserved
0x3256	-	-	-	-	Reserved
0x3257	CA_Y_Top_Thr	7:0	R/W	0xD0	Top boundary of luminance
0x3258	CA_Cnt_Ctrl_1	7:0	R/W	0x05	
	-	7:5	R	-	Reserved
	CA_Y_Bot_Thr	4:0	R/W	0x05	Bottom boundary of luminance

14.5. SOC Gamma Registers (0x3270)

Address	Register Name	Bits	R/W	Reset Value	Descriptions †
0x3270	Gamma_Tab_0	7:0	R/W	0x00	Gamma correction table register 0
0x3271	Gamma_Tab_1	7:0	R/W	0x1F	Gamma correction table register 1
0x3272	Gamma_Tab_2	7:0	R/W	0x2D	Gamma correction table register 2
0x3273	Gamma_Tab_3	7:0	R/W	0x3F	Gamma correction table register 3
0x3274	Gamma_Tab_4	7:0	R/W	0x4E	Gamma correction table register 4
0x3275	Gamma_Tab_5	7:0	R/W	0x5A	Gamma correction table register 5
0x3276	Gamma_Tab_6	7:0	R/W	0x6E	Gamma correction table register 6
0x3277	Gamma_Tab_7	7:0	R/W	0x7E	Gamma correction table register 7
0x3278	Gamma_Tab_8	7:0	R/W	0x8E	Gamma correction table register 8
0x3279	Gamma_Tab_9	7:0	R/W	0x9C	Gamma correction table register 9
0x327A	Gamma_Tab_10	7:0	R/W	0xB4	Gamma correction table register 10
0x327B	Gamma_Tab_11	7:0	R/W	0xC9	Gamma correction table register 11
0x327C	Gamma_Tab_12	7:0	R/W	0xDD	Gamma correction table register 12
0x327D	Gamma_Tab_13	7:0	R/W	0xEE	Gamma correction table register 13
0x327E	Gamma_Tab_14	7:0	R/W	0xFF	Gamma correction table register 14

14.6. SOC Auto-White Balance Registers (0x3290)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
					WB_Gain_R [9:0] †
0x3290	WB_Gain_R_H	1:0	R/W	0x01	AWB Gain R
0x3291	WB_Gain_R_L	7:0	R/W	0x00	
					WB_Gain_B [9:0] †
0x3296	WB_Gain_B_H	1:0	R/W	0x01	WB_Gain_B
0x3297	WB_Gain_B_L	7:0	R/W	0x00	
0x3298	CA_Result_R	7:0	R	-	Color accumulation result R
0x3299	CA_Result_G	7:0	R	-	Color accumulation result G
0x329A	CA_Result_B	7:0	R	-	Color accumulation result B
0x329B	AWB_Control_0	7:0	R/W	0x00	
	AWB_Conve_Range	7:4	R/W	0	AWB convergence range |R – G| < range and |B – G| < range.
	-	3:0	R	0	Reserved
0x329C	AWB_Control_1	7:0	R/W	0x4A	
	AWB_Fine_Tune_Thr	7:3	R/W	9	If difference less than this register, into fine tune mode.
	AWB_Fine_Tune_Step	2:0	R/W	2	AWB fine tune adjustment step, value from 0 to 7 0: No effect. 1: Slowly. 7: Quickly.
0x329D	AWB_Fast_Tune_thr1	6:0	R/W	0x23	Fast speed
0x329E	AWB_Fast_Tune_thr2	6:0	R/W	0x19	Middle speed
0x329F	AWB_Fast_Tune_thr3	6:0	R/W	0x0F	Slow speed
0x32A0	AWB_Fast_Tune_Step	7:0	R/W	0x78	AWB fast tune adjustment step

14.7. SOC Auto-Exposure Registers (0x32B0)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x32B0	LA_Wgt_Ctrl0	7:0	R/W	0x55	
	LA_Wgt_0	7:6	R/W	1	Weighting of Zone 0.
	LA_Wgt_1	5:4	R/W	1	Weighting of Zone 1.
	LA_Wgt_2	3:2	R/W	1	Weighting of Zone 2.
	LA_Wgt_3	1:0	R/W	1	Weighting of Zone 3.
0x32B1	LA_Wgt_Ctrl1	7:0	R/W	0x55	
	LA_Wgt_4	7:6	R/W	1	Weighting of Zone 4.
	LA_Wgt_5	5:4	R/W	1	Weighting of Zone 5.
	LA_Wgt_6	3:2	R/W	1	Weighting of Zone 6.
	LA_Wgt_7	1:0	R/W	1	Weighting of Zone 7.
0x32B2	LA_Wgt_Ctrl2	7:0	R/W	0x55	
	LA_Wgt_8	7:6	R/W	1	Weighting of Zone 8.
	LA_Wgt_9	5:4	R/W	1	Weighting of Zone 9.
	LA_Wgt_10	3:2	R/W	1	Weighting of Zone 10.
	LA_Wgt_11	1:0	R/W	1	Weighting of Zone 11.
0x32B3	LA_Wgt_Ctrl3	7:0	R/W	0x55	
	LA_Wgt_12	7:6	R/W	1	Weighting of Zone 12.
	LA_Wgt_13	5:4	R/W	1	Weighting of Zone 13.
	LA_Wgt_14	3:2	R/W	1	Weighting of Zone 14.
	LA_Wgt_15	1:0	R/W	1	Weighting of Zone 15.
0x32B4	-	-	-	-	Reserved
0x32B5	-	-	-	-	Reserved
0x32B6	-	-	-	-	Reserved
0x32B7	-	-	-	-	Reserved
0x32B8	AE_DetcRange_Upper	7:0	R/W	0x48	AE detect range upper
0x32B9	AE_DetcRange_Lower	6:0	R/W	0x38	AE detect range lower
0x32BA	LA_Result	7:0	R	-	Luminance accumulation result [7:0]
0x32BB	AE_Control_0	7:0	R/W	0x87	
	AE_Speed	7:4	R/W	0x08	0xF is fast, 0x0 is slow
	AE_Anti_Flicker_All_En	3	R/W	0	If enable. Minimum exposure line = AEC_Flicker_Base 0: Disable 1: Enable
	AE_Anti_Flicker_En	2	R/W	1	Anti-Flicker enable 0: Disable 1: Enable

	AE_AGC_En	1	R/W	1	AGC enable 0: Disable 1: Enable
	AE_AEC_En	0	R/W	1	AEC enable 0: Disable 1: Enable
0x32BC	AE_Target_Lum	7:0	R/W	0x40	AE target luminance
0x32BD	AE_ConvRange_Upper	7:0	R/W	0x44	AE convergence range upper
0x32BE	AE_ConvRange_Lower	7:0	R/W	0x3C	AE convergence range lower
0x32BF	AEC_Min_ExpLine	7:0	R/W	0x40	Minimum exposure line limit for AEC Must less than AES_Exp_Offset
0x32C0	AEC_Max_ExpLine	7:0	R/W	0x80	AE_Max_ExpLine for AEC.
0x32C1	-	-	-	-	Reserved
0x32C2	-	-	-	-	Reserved
0x32C3	AGC_Min_Limit	6:0	R/W	0x00	AE_AGC_Min_Limit
0x32C4	AGC_Max_Limit	6:0	R/W	0x20	AE_AGC_Max_Limit
0x32C5	-	-	-	-	Reserved
0x32C6	-	-	-	-	Reserved
0x32C7	AE_Control_1	7:0	R/W	0x00	
	AEC_Flicker_Base_H	7:6	R/W	0	AE flicker exposure line[9:8] Set 1/100 Sec or 1/120 into this register.
	AE_EV_A_H	5	R/W	0	AE_EV_A[8]
	AE_EV_B_H	4	R/W	0	AE_EV_B[8]
	AE_EV_C_H	3	R/W	0	AE_EV_C[8]
	AE_EV_D_H	2	R/W	0	AE_EV_D[8]
	AE_EV_E_H	1	R/W	0	AE_EV_E[8]
	AE_EV_H	0	R	-	AE_EV[8]
0x32C8	AEC_Flicker_Base_L	7:0	R/W	0x3C	AE flicker exposure line[7:0] Set 1/100 Sec or 1/120 into this register.
0x32C9	AE_EV_A_L	7:0	R/W	0x58	AE_EV_A[7:0]
0x32CA	AE_EV_B_L	7:0	R/W	0x68	AE_EV_B[7:0]
0x32CB	AE_EV_C_L	7:0	R/W	0x7C	AE_EV_C[7:0]
0x32CC	AE_EV_D_L	7:0	R/W	0x84	AE_EV_D[7:0]
0x32CD	AE_EV_E_L	7:0	R/W	0x98	AE_EV_E[7:0]
0x32CE	-	-	-	-	Reserved
0x32CF	-	-	-	-	Reserved
0x32D0	AE_ReActive_Flag	0	R/W	0x01	Set register as 1, AE will re-Active.

14.8. SOC Scaler Registers (0x32E0)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
					Scaler_Out_Size_X [10:0] †
0x32E0	Scaler_Out_Size_X_H	2:0	R/W	0x05	Output horizontal size (Even size only) Minimun width is 56.
0x32E1	Scaler_Out_Size_X_L	7:0	R/W	0x00	
					Scaler_Out_Size_Y [10:0] †
0x32E2	Scaler_Out_Size_Y_H	1:0	R/W	0x02	Output vertical size (Even size only) Minimun height is 42.
0x32E3	Scaler_Out_Size_Y_L	7:0	R/W	0xD0	
0x32E4	HSC_SCF_I	4:0	R/W	0x00	Integer part of horizontal scaling factor †
0x32E5	HSC_SCF	7:0	R/W	0x00	Fraction part of horizontal scaling factor †
0x32E6	VSC_SCF_I	4:0	R/W	0x00	Integer part of vertical scaling factor †
0x32E7	VSC_SCF	7:0	R/W	0x00	Fraction part of vertical scaling factor †

† New register values are accepted by enabling LOAD bit in register 0x3060.

14.9. SOC Output Format and Specical Effects Registers (0x32F0)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x32F0	Output_Format	7:0	R/W	0x00	
	Output_Format_Sel	7:4	R/W	0	Output format 0: YCbCr 1: RGB565 2: RGB555 3: RGB444x 4: RGBx444 5: Raw-10 bits 6: CCIR656 7: JPEG
	Raw_Output_Ch_Sel	3:2	R/W	0	Raw-10 bits mode only 0: R start 1: Gr start 2: Gb start 3: B start
	RB_Swap	1	R/W	0	R and B swap 0: Disable 1: In YCbCr mode, swap Cb and Cr. In RGB mode, swap Red and Blue.
	Output_Byte_Swap	0	R/W	0	Output byte swap 0: Disable 1: In YCbCr mode, swap chroma and luminance byte. In RGB mode, swap odd and even byte.
0x32F1	Special_Effect_0	4:0	R/W	0x00	
	Output_Limit	4:3	R/W	0	00: Data value from 0 to 255. 01: Data value from 1 to 254. 10: Y data from 16 to 235; C value form 16 to 240. 11: Reserved.
	Effect_Option	2:0	R/W	0	000: Normal 001: Black and White 010: Sepia 011: Negative 100: Solarization 101: User define and Hue adjust enable 110: Reserved 111: Reserved
0x32F2	Y_Component	7:0	R/W	0x80	Y component.
0x32F3	Chroma_Component	7:0	R/W	0x80	Cb/Cr components. For special effect.
0x32F4	Cb_Ofs	7:0	R/W	0x80	Cb offset. For special effect.
0x32F5	Cr_Ofs	7:0	R/W	0x80	Cr offset. For special effect.
0x32F6	Special_Effect_1	7:0	R/W	0x00	
	-	7:6	-	-	Reserved
	Half_Invert	5	R/W	0	Special effect: Solarization.
	Invert	4	R/W	0	Special effect. Negative.
	Se_C_Component_En	3	R/W	0	Cb/Cr component enable in color component adjustment

					0: Disable 1: Enable
	Se_Y_Component_En	2	R/W	0	Y component enable in color component adjustment 0: Disable 1: Enable
	-	1:0	-	-	Reserved
0x32F7	-	-	-	-	Reserved
0x32F8	-	-	-	-	Reserved
0x32F9	-	-	-	-	Reserved
0x32FA	-	-	-	-	Reserved
0x32FB	Hue_Angle_Shift	7:0	R/W	0x5A	If Effect_Option is 110, set Hue_Angle_Shift for hue shift effect(-90° ~ 90°).
0x32FC	Brt_Ofs	7:0	R/W	0	Brightness offset (-128 ~ 127)

14.10. Image Quality Control Registers (0x3300)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3300	Noise_Enh_Param	7:0	R/W	0x12	
	Edge_Enhancement_H	7:6	R/W	0	Edge_Enhancement [9:8]
	Noise_Reduction_Val	5:0	R/W	0x12	Noise reduction Set rbw and gw in the same time
0x3301	Edge_Enhancement_L	7:0	R/W	0x80	Edge_Enhancement [7:0]
					Matrix_RR [10:0]
0x3302	Matrix_RR_H	2:0	R/W	0x00	Color correction and transform matrix
0x3303	Matrix_RR_L	7:0	R/W	0x4D	
					Matrix_RG [10:0]
0x3304	Matrix_RG_H	2:0	R/W	0x00	Color correction and transform matrix
0x3305	Matrix_RG_L	7:0	R/W	0x96	
					Matrix_RB [10:0]
0x3306	Matrix_RB_H	2:0	R/W	0x00	Color correction and transform matrix
0x3307	Matrix_RB_L	7:0	R/W	0x1D	
					Matrix_GR [10:0]
0x3308	Matrix_GR_H	2:0	R/W	0x07	Color correction and transform matrix
0x3309	Matrix_GR_L	7:0	R/W	0xD5	
					Matrix_GG [10:0]
0x330A	Matrix_GG_H	2:0	R/W	0x07	Color correction anmd transform matrix
0x330B	Matrix_GG_L	7:0	R/W	0xAB	
					Matrix_GB [10:0]
0x330C	Matrix_GB_H	2:0	R/W	0x00	Color correction and transform matrix
0x330D	Matrix_GB_L	7:0	R/W	0x80	
					Matrix_BR [10:0]
0x330E	Matrix_BR_H	2:0	R/W	0x00	Color correction and transform matrix
0x330F	Matrix_BR_L	7:0	R/W	0x80	
					Matrix_BG [10:0]
0x3310	Matrix_BG_H	2:0	R/W	0x07	Color correction and transform matrix
0x3311	Matrix_BG_L	7:0	R/W	0x95	
					Matrix_BB [10:0]
0x3312	Matrix_BB_H	2:0	R/W	0x07	Color correction and transform matrix
0x3313	Matrix_BB_L	7:0	R/W	0xEB	

14.11. JPEG Encoder Registers (0x3400)

Address	Register Name	Bits	R/W	Reset Value	Descriptions
0x3400	JPEG_Ctrl	3:0	R/W	0x00	
	Jpg_Reset	3	R/W	0	Reset JPEG core 0: Normal. 1: Reset.
	-	2:1	R	0	Reserved
	Jpg_Active	0	R/W	0	JPEG core active 0: Disable. 1: Enable.
0x3401	Quant_Factor	7:0	R/W	0x4E	JPEG Quantization Quality Scaling Factor (1) 0 ~ 127: Linear quality scaling factor for JPEG quantization. Value 0 indicates the best image quality (the worst compressed image size), while value 127 means the best compressed image size (the worst image quality). (2) 128 ~ 255: Use default quantization table.
0x3402	Num_MCU_H	4:0	R	0x00	Total MCU Count High byte
0x3403	Num_MCU_L	7:0	R	0x00	Total MCU Count Low byte
0x3404	Num_RSTR_H	4:0	R/W	0x00	Restart Interval High byte The number of MCU between two Restart Markers. Value 0 means to disable Restart Marker Insert for the following scan.
0x3405	Num_RSTR_L	7:0	R/W	0x00	Restart Interval Low byte
0x3406	Byte_CTR_H	3:0	R	0x00	Compressed Image Size High Byte Register
0x3407	Byte_CTR_M	7:0	R	0x00	Compressed Image Size Second Byte Register
0x3408	Byte_CTR_L	7:0	R	0x00	Compressed Image Size Low Byte Register If the output stream size is over an image size, it will insert 0xFFD9 at the end of bitstream.
0x340B	Img_Width_H	7:0	R	0x00	
0x340C	Img_Width _L	7:0	R	0x00	
0x340D	Img_Height_H	7:0	R	0x00	
0x340E	Img_Height_L	7:0	R	0x00	
0x340F	-	7:0	R	0x00	Reserved
0x3410	JPG_Output_Mode	1:0	R/W	0x00	JPEG Output Mode 0: Vaild mode 1: Frame mode with valid length information 2: Frame mode

15. Chief Ray Angle

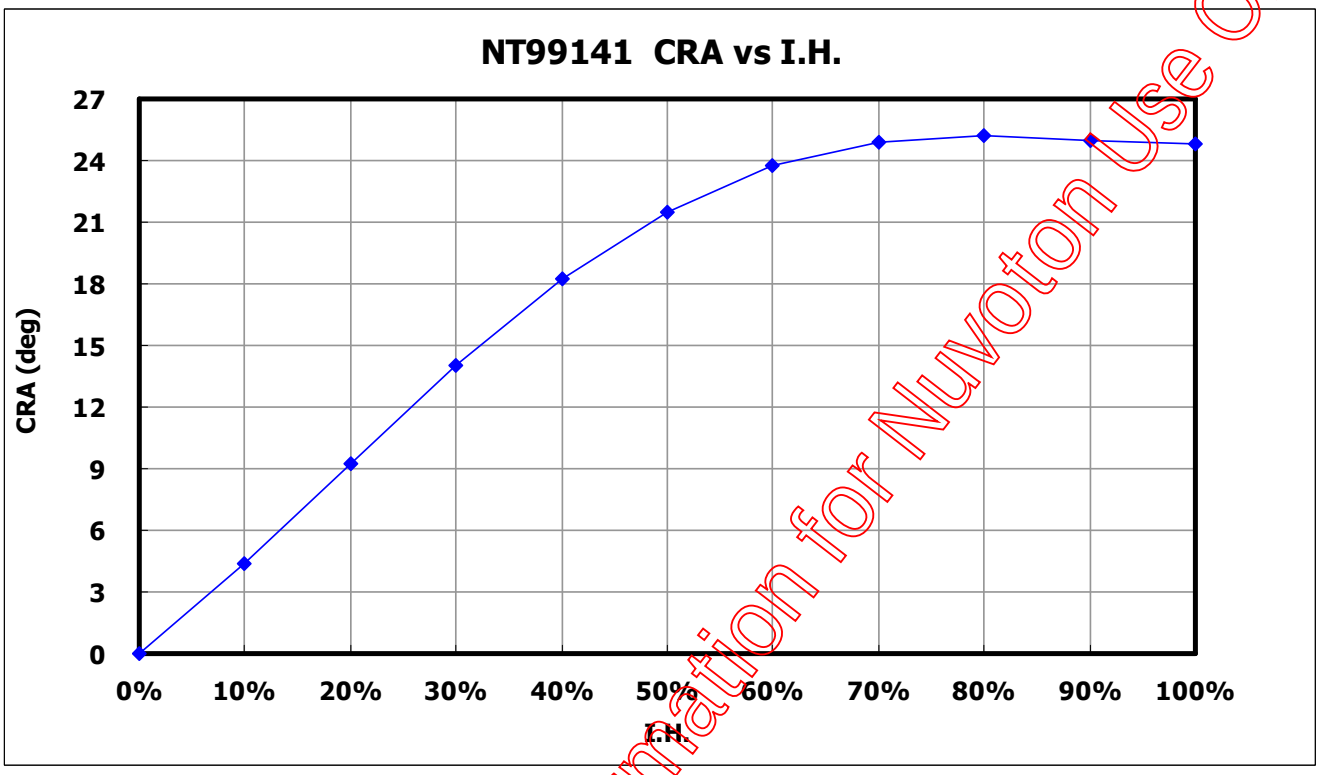


Fig. 36 Chief Ray Angle

16. Electrical Characteristics

16.1. Absolute Maximum Ratings

VDD Supply Voltage	-0.3	to	+2.0V
VDDIO / AVDD / AVDDPIX Supply Voltage	-0.3	to	+3.9V
Operating Ambient Temperature	-20^{0}C	to	+70^{0}C
Storage Temperature	-40^{0}C	to	+85^{0}C

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

16.2. DC Characteristics

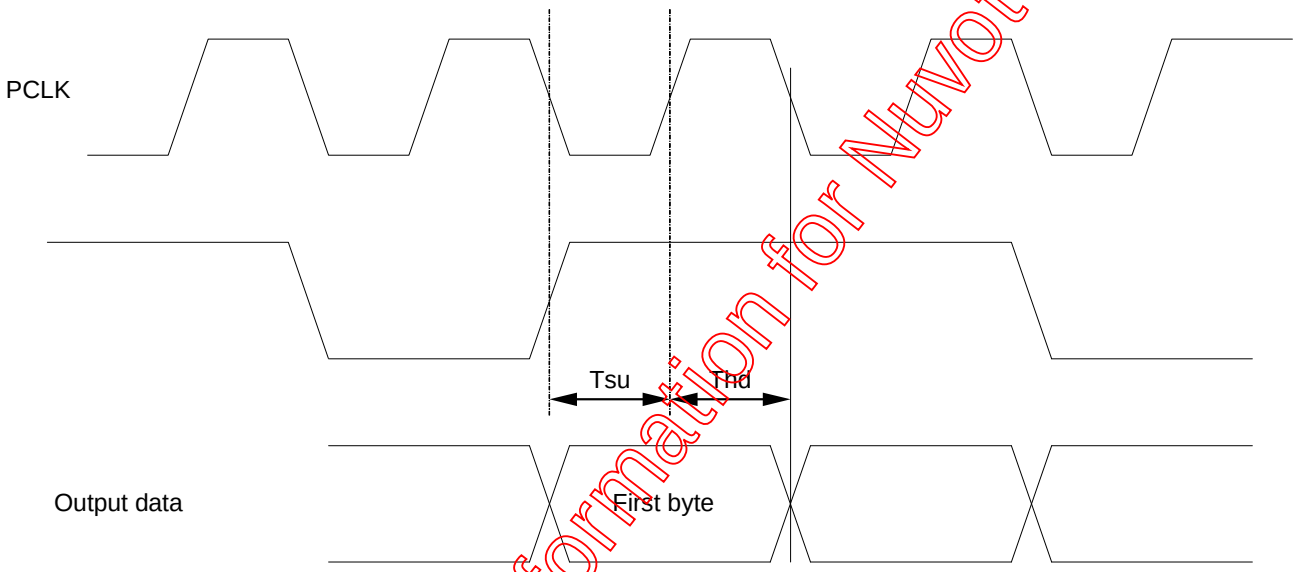
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Digital Logic Supply Voltage	1.425	1.5	1.575	V	
VDDIO	I/O Interface Supply Voltage	1.7	3.3	3.6	V	
AVDD	Analog Supply Voltage	3.0	3.3	3.6	V	
AVDDPIX	Pixel Supply Voltage	3.0	3.3	3.6	V	
P_{RUN}	Operating Power Consumption	-	215	-	mW	30fps @ HD JPG (external 1.5V)
I_{VDD}	Digital Logic Operating Current	-	32.67	-	mA	30fps @ HD JPG (external 1.5V)
I_{VDDIO}	I/O Operating Current		10.24	-	mA	30fps @ HD JPG (external 1.5V)
$I_{AVDD+AVDDPIX}$	Analog Operating Current	-	40.08	-	mA	30fps @ HD JPG
V_{IH}	Input High Voltage	0.7 x VDDIO	-	-	V	
V_{IL}	Input Low Voltage	-	-	0.3 x VDDIO	V	
I_{OH}	Output Driving Current VDDIO = 3.3V	-	4.5	-	mA	V_{OH}=VDDIO-0.3V, 4mA setting
I_{OL}	Output Sinking Current VDDIO = 3.3V	-	6.4	-	mA	V_{OL}=GND+0.3V, 4mA setting
I_{OH}	Output Driving Current VDDIO = 1.7V	-	2.6	-	mA	V_{OH}=VDDIO-0.3V, 4mA setting
I_{OL}	Output Sinking Current VDDIO = 1.7V	-	3.6	-	mA	V_{OL}=GND+0.3V, 4mA setting
I_{OZ}	Tri-state Output Leakage Current	-	-	±1	µA	

16.3. AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
F_{OSC}	Frequency MCLK	6	24	27	MHz	
	Duty cycle	45	-	55	%	

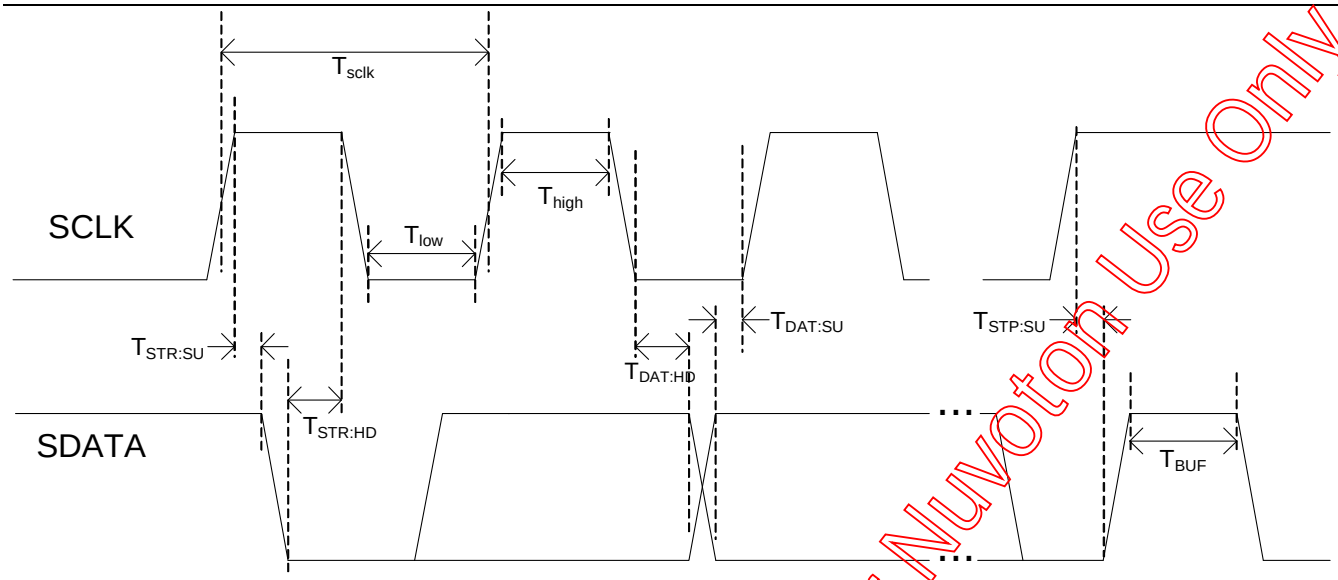
Horizontal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Tsu	Output data setup time	-	9.5	-	ns	VDDIO=3.3V
Thd	Output data hold time	-	11	-	ns	PCLK=48MHz



Two-wire Serial Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Tsclk	Serial Interface Input Clock Frequency	-	-	400	KHz	
T_{high}	High Period of The SCLK Clock	0.6	-	-	µs	
T_{low}	Low Period of The SCLK Clock	1.3	-	-	µs	
$T_{STR:SU}$	Start Setup Time	0.6	-	-	µs	
$T_{STR:HD}$	Start Hold Time	0.6	-	-	µs	
$T_{STP:SU}$	Stop Setup Time	0.6	-	-	µs	
$T_{DAT:SU}$	DATA Setup Time	0.1	-	-	µs	
$T_{DAT:HD}$	DATA Hold Time	0.2	-	-	µs	
T_{BUF}	Bus Free Time between a STOP and START Condition	1.3	-	-	µs	



15. SMT Reflow Profile

	A	B		C	D		E		F
	Ramp up	Pre-heat		Ramp up	Melt point		Peak point		Ramp down
		Temp.	Time		Temp.	Time	Temp.	Time	
New Reflow Profile	Max 3'C/sec	150 ~ 200'C	60~70 sec	Max 3'C/sec	217'C	60 ~70 sec	235 ~ 240'C	20~25 sec	Max 6'C/sec

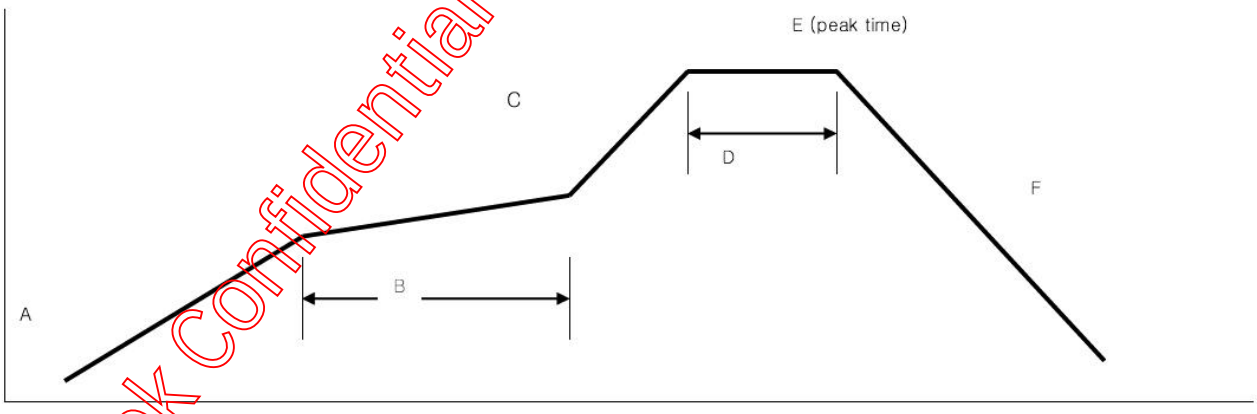


Fig. 37 SMT Rwflow Profile