

# MOSFET - Power, N-Channel 100 V, 4.2 m $\Omega$ , 201 A

# **NTB004N10G**

#### **Features**

- Low R<sub>DS(on)</sub>
- High Current Capability
- Wide SOA
- These Devices are Pb-Free and are RoHS Compliant

### **Applications**

• Hot Swap in 48 V Systems

# **MAXIMUM RATINGS** ( $T_J = 25^{\circ}C$ Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	100	V
Gate-to-Source Volta	ge – Conti	nuous	V <sub>GS</sub>	±20	V
Continuous Drain	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	201	Α
Current R <sub>θJC</sub>	State	T <sub>C</sub> = 100°C		142	
Power Dissipation $R_{\theta JC}$	Steady State	T <sub>C</sub> = 25°C	P <sub>D</sub>	340	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs		I <sub>DM</sub>	3002	Α
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	283	Α
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, $I_{L(pk)}$ = 102 A, L = 0.1 mH, $R_G$ = 25 $\Omega$ )			E <sub>AS</sub>	520	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			TL	260	°C

# THERMAL RESISTANCE RATINGS

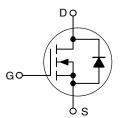
Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	0.44	°C/W
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

 Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX (Note 1)
100 V	4.2 m $\Omega$ @ 10 V	201 A

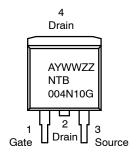
#### N-Channel





D<sup>2</sup>PAK CASE 418AJ STYLE 2

# MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Site Code

Y = Year Code WW = Week Code

ZZ = 2-digit Assembly Lot Code NTB004N10G = Specific Device Code

# **ORDERING INFORMATION**

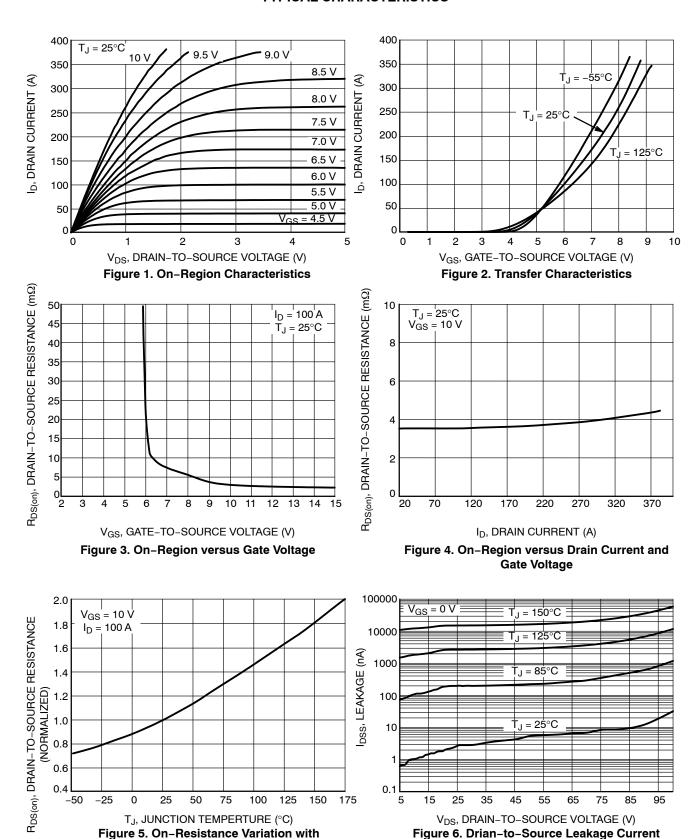
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•						•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V,	I <sub>D</sub> = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				83.2		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C			1.0	μΑ
		V <sub>DS</sub> = 80 V	T <sub>J</sub> = 150°C			100	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V	′ <sub>GS</sub> = ±20 V			±100	nA
ON CHARACTERISTICS (Note 2)	•						•
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{GS} = V_{DS}$ ,	I <sub>D</sub> = 500 μA	2.0	2.8	4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(th)</sub> /T <sub>J</sub>				-10.5		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub>	T <sub>J</sub> = 25°C		3.4	4.2	mΩ
$= 100 \text{A}$ $T_{\text{J}} = 175^{\circ}\text{C}$	T <sub>J</sub> = 175°C		6.82		mΩ		
Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 10 V	, I <sub>D</sub> = 100 A		70		S
CHARGES, CAPACITANCES & GATE RESIST.	ANCE			1	•		
Input Capacitance	C <sub>iss</sub>				11900		pF
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz			1170		1
Reverse Transfer Capacitance	C <sub>rss</sub>	'-'	IVII IZ		147		1
Total Gate Charge	Q <sub>G(TOT)</sub>				175		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				32		_
Gate-to-Source Charge	Q <sub>GS</sub>	$V_{GS} = 10 \text{ V},$			67.3		
Gate-to-Drain Charge	$Q_{GD}$	I <sub>D</sub> = 100 A			40.8		
Plateau Voltage	$V_{GP}$				6.0		V
Gate Resistance	$R_{G}$	V <sub>OSC</sub> = 100 mV, V <sub>GS</sub> = 0 V, f = 1 MHz			0.445		Ω
SWITCHING CHARACTERISTICS, V <sub>GS</sub> = 10 V	(Note 3)				1		
Turn-On Delay Time	t <sub>d(on)</sub>				43		ns
Rise Time	t <sub>r</sub>	Voc = 10 V	Vpp = 50 V		64.5		
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS} = 10 \text{ V},$ $I_D = 100 \text{ A},$	$R_G = 4.7 \Omega$		84.7		
Fall Time	t <sub>f</sub>	1			30		1
DRAIN-SOURCE DIODE CHARACTERISTICS		•		ı			
Forward Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 100 A	T <sub>J</sub> = 25°C		0.9	1.2	V
			T <sub>J</sub> = 125°C		0.77		1
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 100 A, dI <sub>SD</sub> /dt = 100 A/μs			76.6		ns
Charge Time	ta				46.4		1
Discharge Time	t <sub>b</sub>				30.2		1
Reverse Recovery Charge	Q <sub>RR</sub>				157		nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
Switching characteristics are independent of operating junction temperatures.

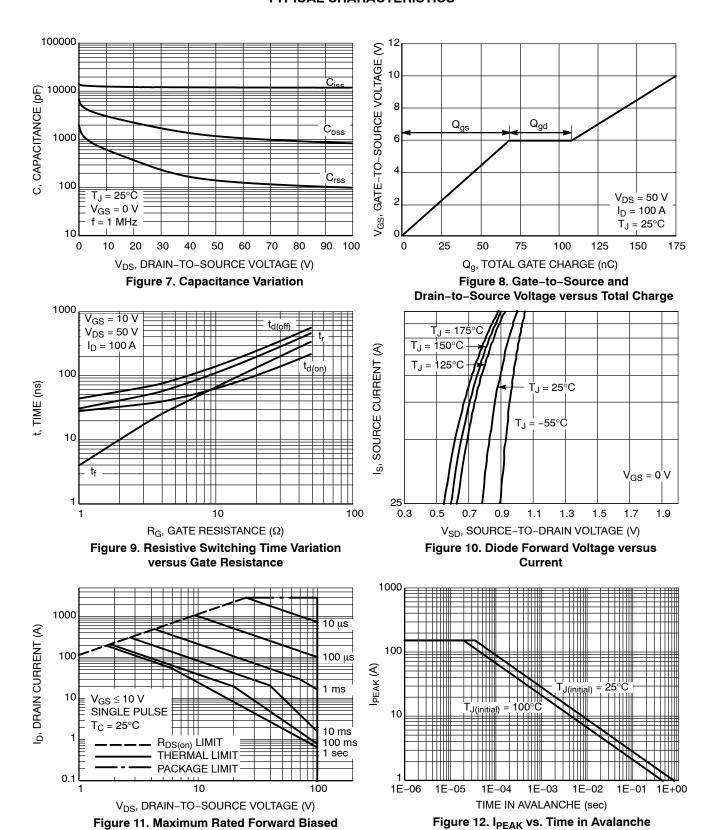
#### TYPICAL CHARACTERISTICS



versus Voltage

**Temperature** 

#### **TYPICAL CHARACTERISTICS**



Safe Opeating Area

# **TYPICAL CHARACTERISTICS**

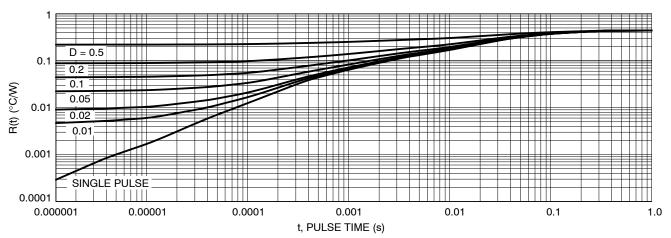


Figure 13. Thermal Response

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTB004N10G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

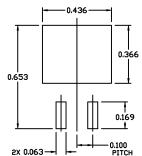




# D<sup>2</sup>PAK-3 (TO-263, 3-LEAD) CASE 418AJ

ISSUE F

**DATE 11 MAR 2021** 

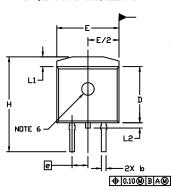


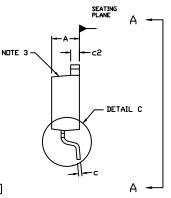
RECOMMENDED MOUNTING FOOTPRINT

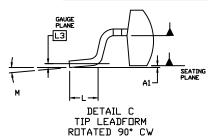
#### NOTES

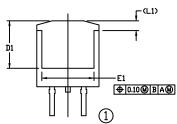
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE DUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- 5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- 6. OPTIONAL MOLD FEATURE.
- 7. ①,② ... OPTIONAL CONSTRUCTION FEATURE CALL DUTS.

	INCHES		MILLIN	IETERS
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
ھ	0.020	0.039	0.51	0.99
u	0.012	0.029	0.30	0.74
5	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260		6.60	
E	0.380	0.420	9.65	10.67
E1	0.245	-	6.22	
e	0.100 BSC		2.54 BSC	
Ξ	0.575	0.625	14.60	15.88
٦	0.070	0.110	1.78	2.79
L1		0.066		1.68
L2		0.070		1.78
L3	0.010 BSC		0.25 BSC	
М	0*	8*	0*	8*

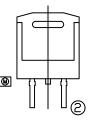


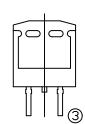


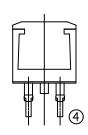




VIEW A-A







VIEW A-A OPTIONAL CONSTRUCTIONS

AYWW

XXXXXXXXX

Rectifier

**AKA** 

**GENERIC MARKING DIAGRAMS\*** 

XXXXXX

**XXYMW** 

SSG

XXXXXX = Specific Device Code = Assembly Location Α

WL = Wafer Lot

= Year ww = Work Week

W = Week Code (SSG) Μ = Month Code (SSG)

G = Pb-Free Package = Polarity Indicator **AKA** 

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ", may or may not be present. Some products may not follow the Generic Marking.

# IC

XXXXXXXX

**AWLYWWG** 

98AON56370E

Standard

XXXXXXXX

**AYWW** 

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D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)

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