

# NTP30N06, NTB30N06

## Power MOSFET 30 Amps, 60 Volts

### N-Channel TO-220 and D<sup>2</sup>PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### Features

- Pb-Free Packages are Available

#### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 10 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage	V <sub>GS</sub>	± 20	Vdc
– Continuous	V <sub>GS</sub>	± 30	
– Non-Repetitive (t <sub>p</sub> ≤ 10 ms)			
Drain Current	I <sub>D</sub>	27	A <sub>dc</sub>
– Continuous @ T <sub>A</sub> = 25°C	I <sub>D</sub>	15	
– Continuous @ T <sub>A</sub> = 100°C	I <sub>DM</sub>	80	A <sub>pk</sub>
– Single Pulse (t <sub>p</sub> ≤ 10 μs)			
Total Power Dissipation @ T <sub>A</sub> = 25°C	P <sub>D</sub>	88.2	W
Derate above 25°C		0.59	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 50 Vdc, V <sub>GS</sub> = 10 Vdc, L = 0.3 mH I <sub>L(pk)</sub> = 26 A, V <sub>DS</sub> = 60 Vdc)	E <sub>AS</sub>	101	mJ
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.7	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T <sub>L</sub>	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

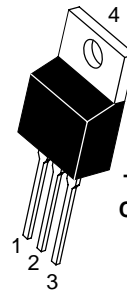
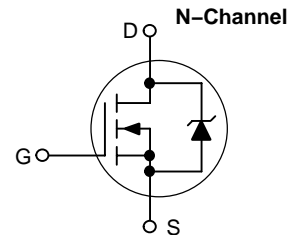


ON Semiconductor®

<http://onsemi.com>

30 AMPERES, 60 VOLTS

R<sub>DS(on)</sub> = 42 mΩ

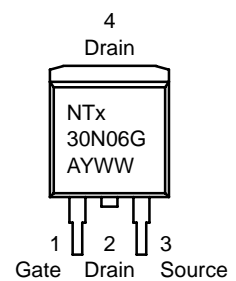
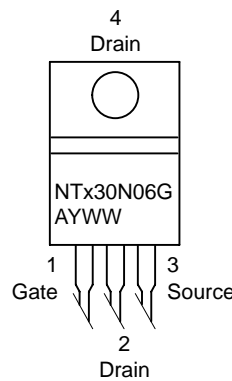


TO-220AB  
CASE 221A  
STYLE 5



D<sup>2</sup>PAK  
CASE 418B  
STYLE 2

#### MARKING DIAGRAMS & PIN ASSIGNMENTS



NTx30N06 = Device Code  
 x = B or P  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTP30N06, NTB30N06

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 1) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 –	71.1 70	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	±100	nAdc

## ON CHARACTERISTICS (Note 1)

Gate Threshold Voltage (Note 1) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 –	3.05 7.3	4.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 1) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 15 Adc)	R <sub>DS(on)</sub>	–	35	42	mΩ
Static Drain-to-Source On-Voltage (Note 1) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 30 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 15 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	– –	1.1 0.98	1.5 –	Vdc
Forward Transconductance (Note 1) (V <sub>DS</sub> = 7.0 Vdc, I <sub>D</sub> = 15 Adc)	g <sub>FS</sub>	–	16	–	mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	–	850	1200	pF
Output Capacitance		C <sub>oss</sub>	–	250	350	
Transfer Capacitance		C <sub>rss</sub>	–	68	100	

## SWITCHING CHARACTERISTICS (Note 2)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 30 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 1)	t <sub>d(on)</sub>	–	11	25	ns
Rise Time		t <sub>r</sub>	–	36	80	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	24	50	
Fall Time		t <sub>f</sub>	–	31	60	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 30 Adc, V <sub>GS</sub> = 10 Vdc) (Note 1)	Q <sub>T</sub>	–	23.4	46	nC
		Q <sub>1</sub>	–	5.1	–	
		Q <sub>2</sub>	–	11	–	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc) (Note 1) (I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	– –	1.03 1.05	1.15 –	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 1)	t <sub>rr</sub>	–	52	–	ns
		t <sub>a</sub>	–	38	–	
		t <sub>b</sub>	–	15	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.094	–	μC

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

# NTP30N06, NTB30N06

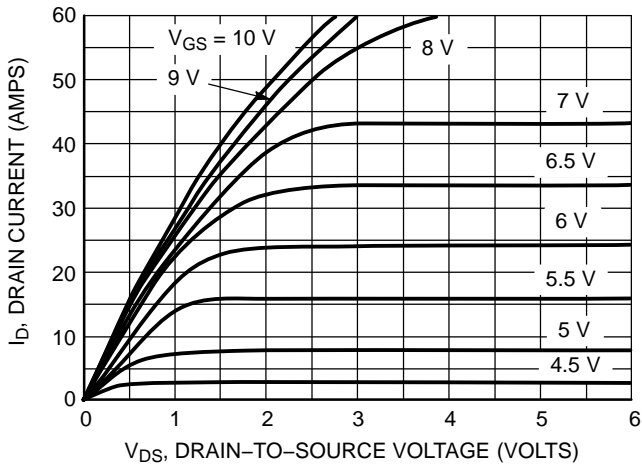


Figure 1. On-Region Characteristics

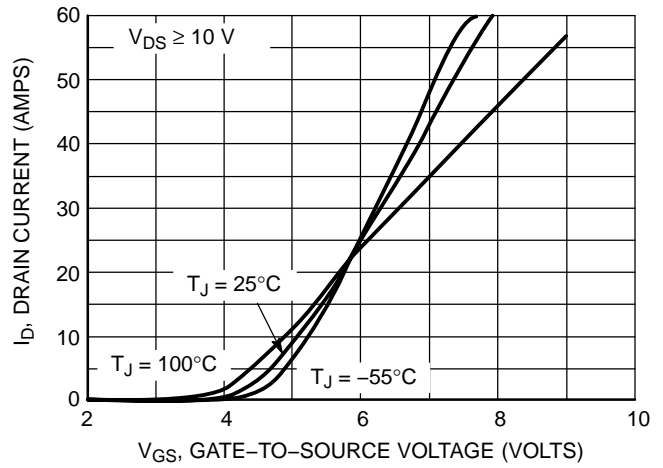


Figure 2. Transfer Characteristics

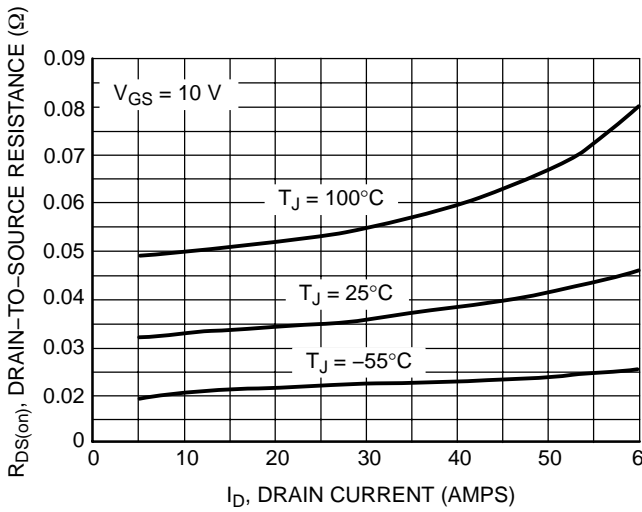


Figure 3. On-Resistance versus Gate-to-Source Voltage

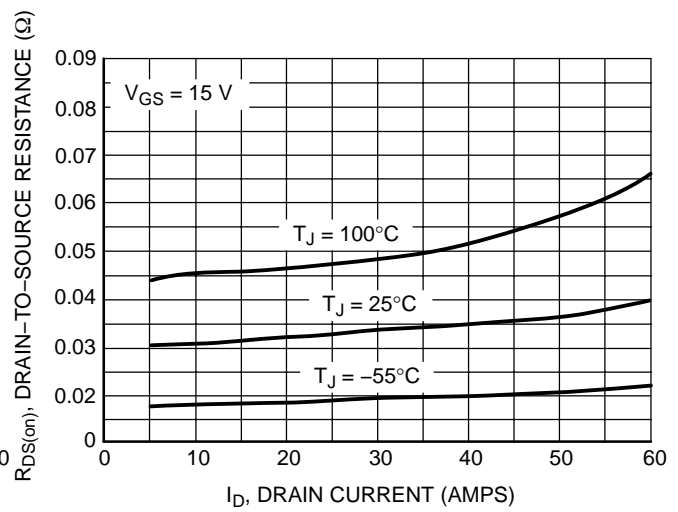


Figure 4. On-Resistance versus Drain Current and Gate Voltage

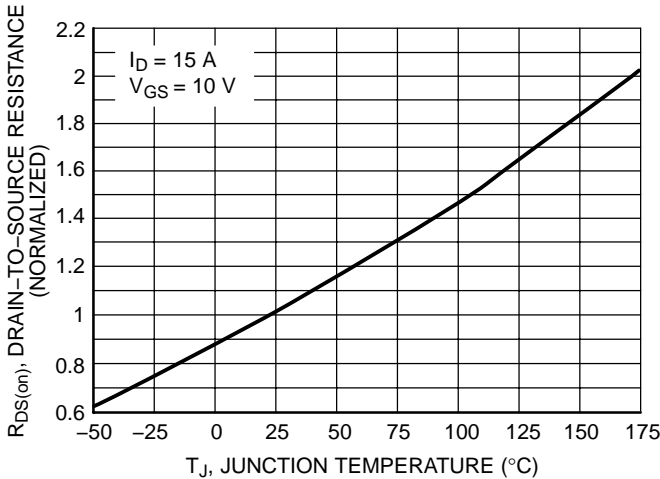


Figure 5. On-Resistance Variation with Temperature

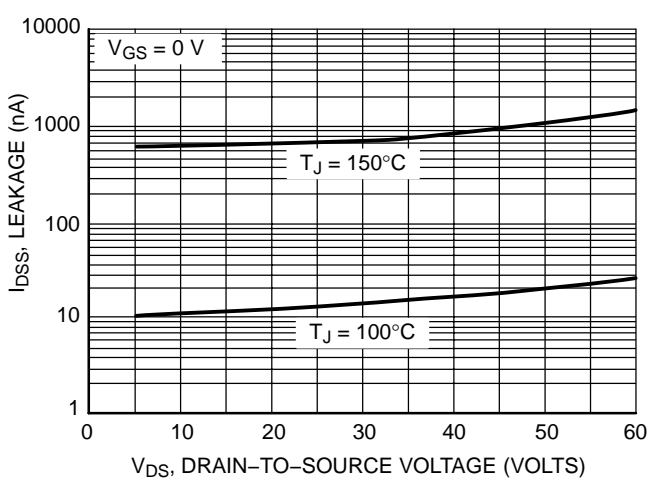


Figure 6. Drain-to-Source Leakage Current versus Voltage

# NTP30N06, NTB30N06

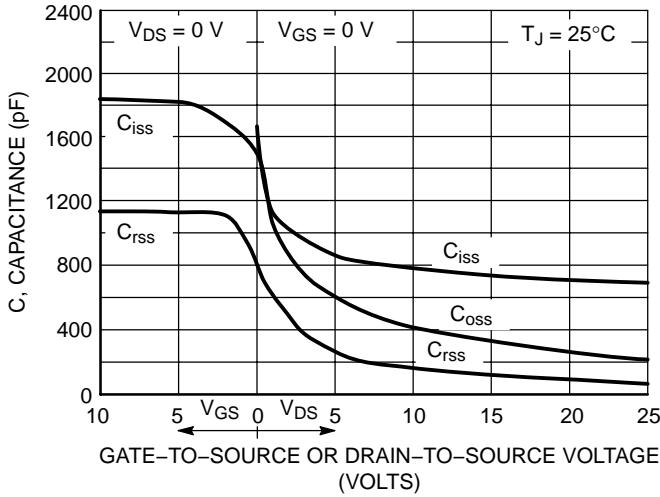


Figure 7. Capacitance Variation

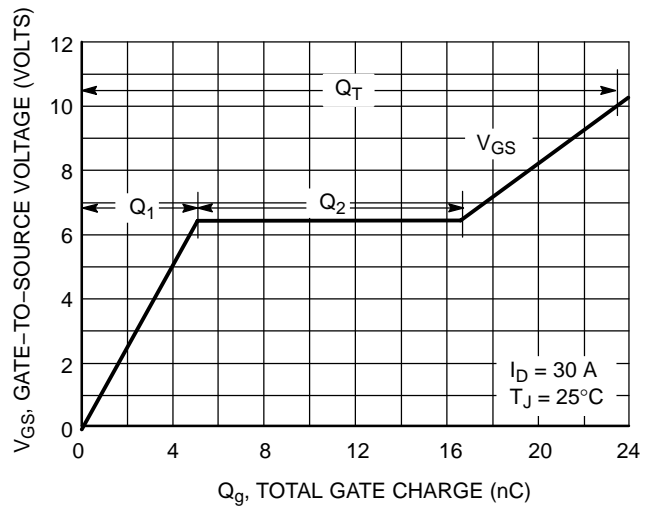


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

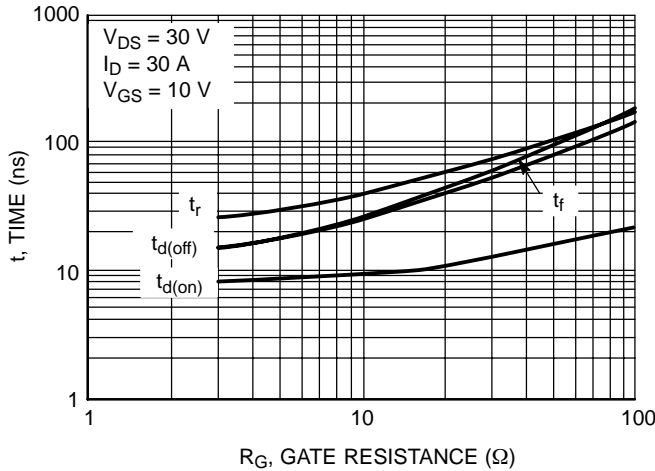


Figure 9. Resistive Switching Time Variation versus Gate Resistance

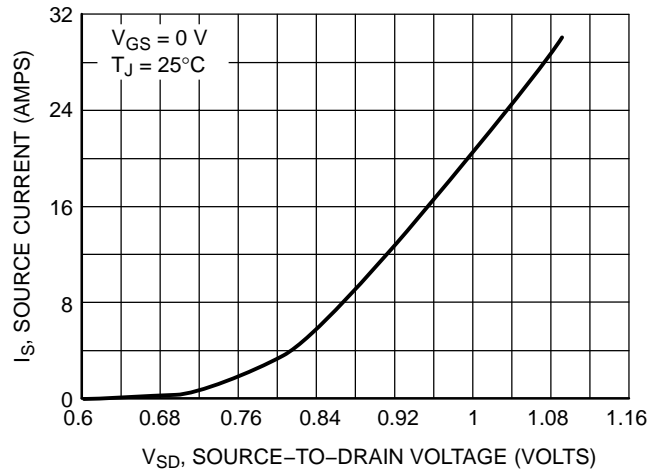


Figure 10. Diode Forward Voltage versus Current

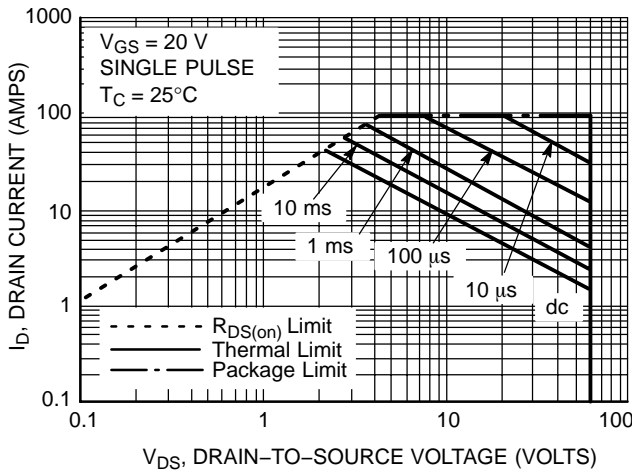


Figure 11. Maximum Rated Forward Biased Safe Operating Area

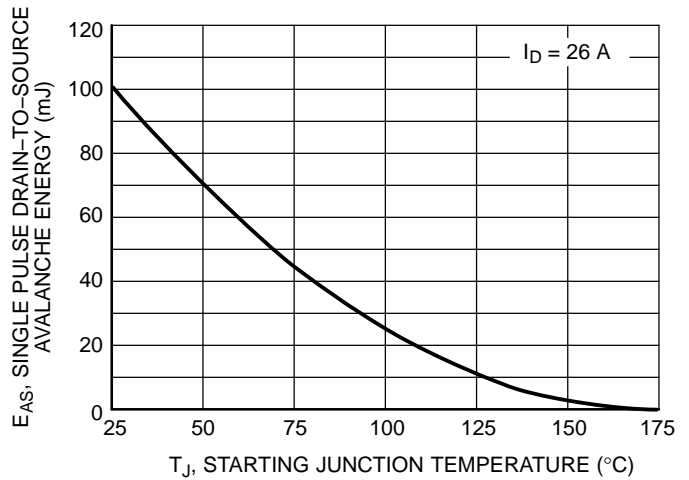


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTP30N06, NTB30N06

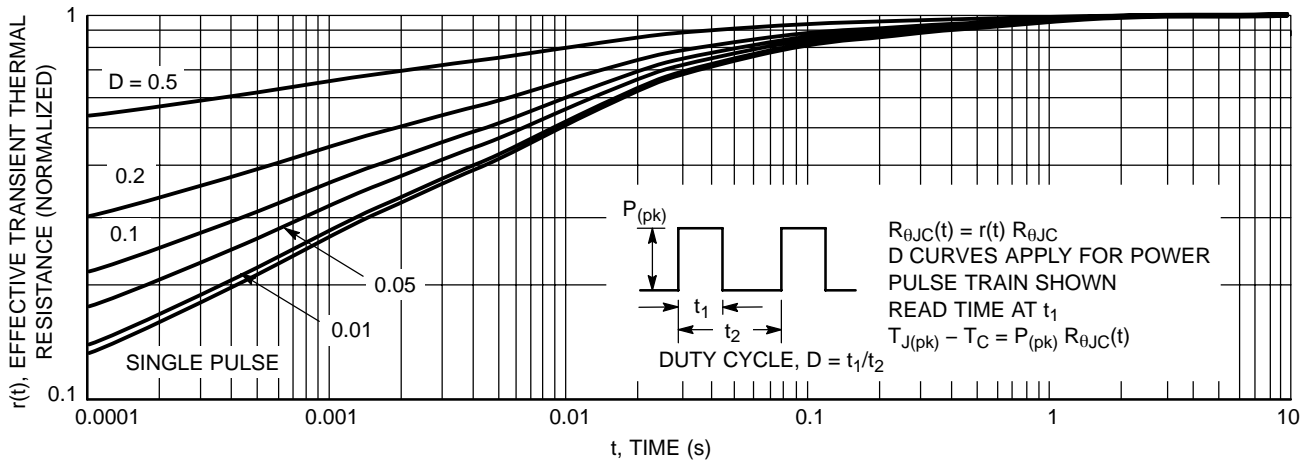


Figure 13. Thermal Response

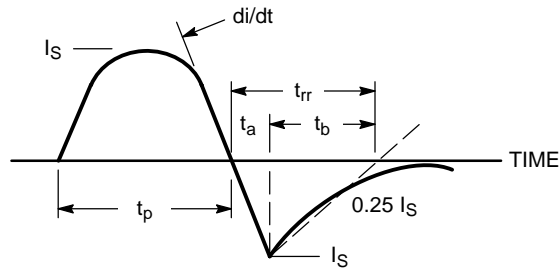


Figure 14. Diode Reverse Recovery Waveform

## ORDERING INFORMATION

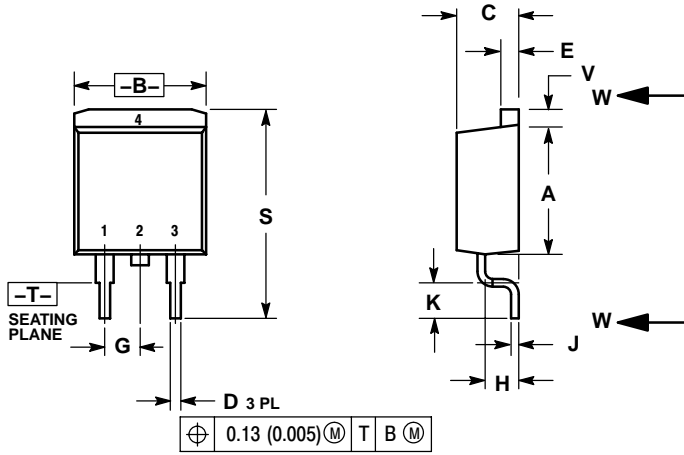
Device	Package	Shipping†
NTP30N06	TO-220AB	50 Units / Rail
NTB30N06	D <sup>2</sup> PAK	50 Units / Rail
NTB30N06G	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NTB30N06T4	D <sup>2</sup> PAK	800 Units / Tape & Reel
NTB30N06T4G	D <sup>2</sup> PAK (Pb-Free)	800 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTP30N06, NTB30N06

## PACKAGE DIMENSIONS

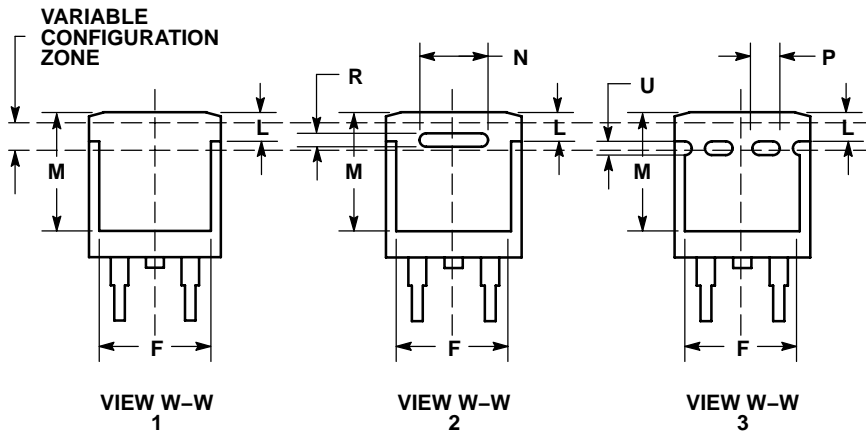
D<sup>2</sup>PAK  
CASE 418B-04  
ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

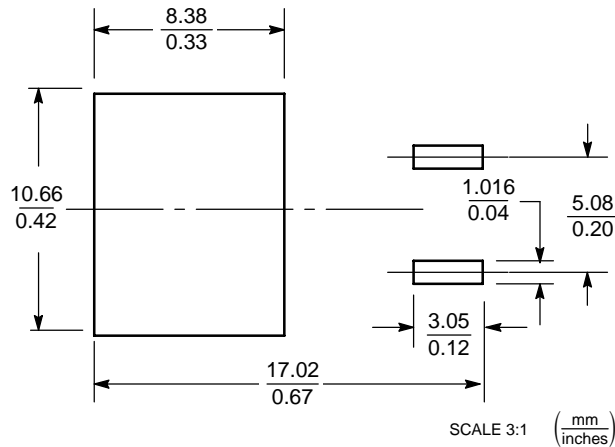
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



**STYLE 2:**

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

**SOLDERING FOOTPRINT\***

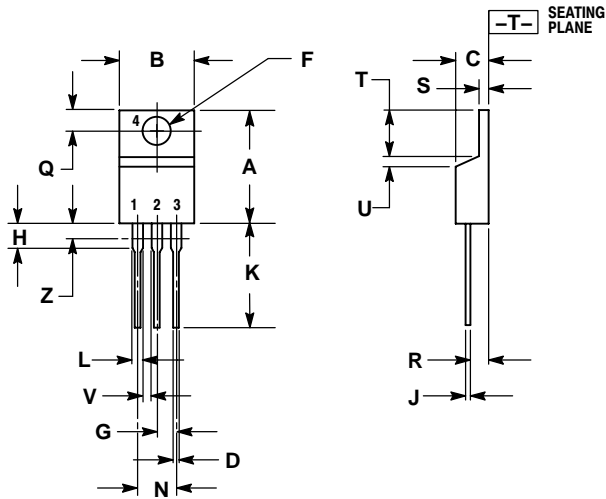


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTP30N06, NTB30N06

## PACKAGE DIMENSIONS

TO-220  
CASE 221A-09  
ISSUE AA



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

**STYLE 5:**

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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