

NTB65N02R, NTP65N02R

Product Preview

Power MOSFET 65 A, 24 V N-Channel TO-220, D²PAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Fast Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	24	V_{dc}
Gate-to-Source Voltage	V_{GS}	± 20	V_{dc}
Drain Current (Continuous @ $T_A = 25^\circ\text{C}$ (Note 3) Single Pulse ($t_p = 10 \mu\text{s}$)	I_D I_{DM}	65 160	A A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	78	W
Operating and Storage Temperature	T_J and T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 V_{dc}$, $V_{GS} = 5 V_{dc}$, $I_L = A_{pk}$, $L = 1 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	TBD	mJ
Thermal Resistance	Junction-to-Case $R_{\theta JC}$ Junction-to-Ambient (Note 1) $R_{\theta JA}$ Junction-to-Ambient (Note 2) $R_{\theta JA}$	1.6 67 120	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$

1. When surface mounted to an FR4 board using 1 inch pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).
3. Chip current capability limited by package.

PIN ASSIGNMENT

PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain

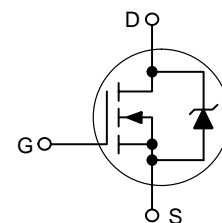
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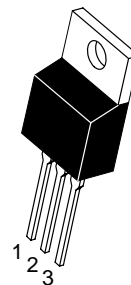
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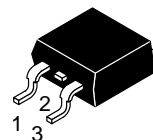
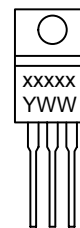
65 A, 24 V
 $R_{DS(on)} = 8.3 \text{ m}\Omega$ (TYP)



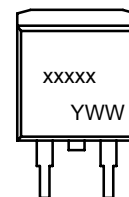
MARKING DIAGRAMS



**TO-220AB
CASE 221A
Style 5**



**D²PAK
CASE 418B
Style 2**



xxxxx = Specific Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTB65N02R	D ² PAK	50 Units/Rail
NTB65N02RT4	D ² PAK	800 Tape & Reel
NTP65N02R	TO-220AB	50 Units/Rail

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 4) (V _{GS} = 0 V _{dc} , I _D = 250 μA _{dc}) Temperature Coefficient (Positive)	V _{(br)DSS}	24 –	27.5 25.5	– –	V _{dc} mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc}) (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc} , T _J = 150°C)	I _{DSS}	– –	– –	1.5 15	μA _{dc}
Gate-Body Leakage Current (V _{GS} = ±20 V _{dc} , V _{DS} = 0 V _{dc})	I _{GSS}	–	–	±100	nA _{dc}

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage (Note 4) (V _{DS} = V _{GS} , I _D = 250 μA _{dc}) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.5 –4.1	2.0 –	V _{dc} mV/°C
Static Drain-to-Source On-Resistance (Note 4) (V _{GS} = 4.5 V _{dc} , I _D = 15 A _{dc}) (V _{GS} = 10 V _{dc} , I _D = 20 A _{dc}) (V _{GS} = 10 V _{dc} , I _D = 30 A _{dc})	R _{DS(on)}	– – –	10.5 8.3 9.5	12.5 10.5 –	mΩ
Forward Transconductance (Note 4) (V _{DS} = 10 V _{dc} , I _D = 15 A _{dc})	g _{FS}	–	20	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 24 V _{dc} , V _{GS} = 0 V f = 1 MHz)	C _{iss}	–	1050	1470	pF
Output Capacitance		C _{oss}	–	394	550	
Transfer Capacitance		C _{rss}	–	88	120	

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V _{GS} = 5 V _{dc} , V _{DD} = 10 V _{dc} , I _D = 30 A _{dc} , R _G = 3 Ω)	t _{d(on)}	–	11.2	20	ns
Rise Time		t _r	–	52	100	
Turn-Off Delay Time		t _{d(off)}	–	10	20	
Fall Time		t _f	–	4	10	
Gate Charge	(V _{GS} = 4.5 V _{dc} , I _D = 30 A _{dc} , V _{DS} = 10 V _{dc}) (Note 4)	Q _T	–	8.4	12	nC
		Q ₁	–	3.7	–	
		Q ₂	–	4.04	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 20 A _{dc} , V _{GS} = 0 V _{dc}) (Note 4) (I _S = 30 A _{dc} , V _{GS} = 0 V _{dc}) (I _S = 20 A _{dc} , V _{GS} = 0 V _{dc} , T _J = 125°C)	V _{SD}	– – –	0.88 1.10 0.80	1.2 – –	V _{dc}
Reverse Recovery Time	(I _S = 20 A _{dc} , V _{GS} = 0 V _{dc} , di _S /dt = 100 A/μs) (Note 4)	t _{rr}	–	15.5	–	ns
		t _a	–	12.6	–	
		t _b	–	2.6	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.005	–	μC

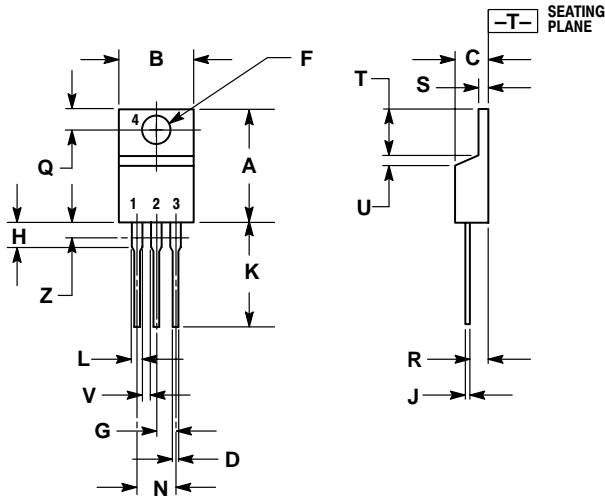
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

5. Switching characteristics are independent of operating junction temperatures.

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PACKAGE DIMENSIONS

TO-220AB CASE 221A-09 ISSUE AA

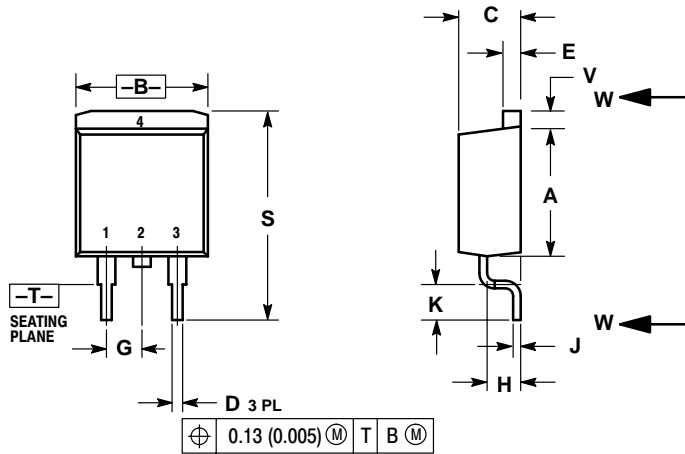


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

D²PAK CASE 418B-04 ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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