

# Silicon Carbide (SiC) MOSFET – EliteSiC, 28 mohm, 1700 V, M1, D2PAK-7L NTBG028N170M1

## Features

- Typ.  $R_{DS(on)} = 28\text{ m}\Omega$
- Ultra Low Gate Charge (typ.  $Q_{G(tot)} = 222\text{ nC}$ )
- Low Effective Output Capacitance (typ.  $C_{oss} = 200\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

## Typical Applications

- UPS
- DC–DC Converter
- Boost Converter

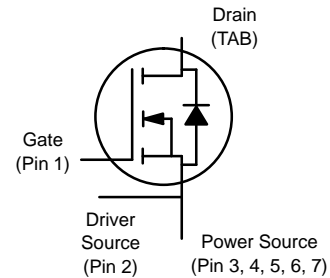
## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	1700	V	
Gate-to-Source Voltage		$V_{GS}$	-15/+25	V	
Recommended Operation Values of Gate-to-Source Voltage		$T_C < 175^\circ\text{C}$ $V_{GSop}$	-5/+20	V	
Continuous Drain Current (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	71	A
			$P_D$	428	W
Continuous Drain Current (Note 2)	Steady State	$T_C = 100^\circ\text{C}$	$I_D$	53	A
			$P_D$	214	W
Pulsed Drain Current (Note 3)	$T_A = 25^\circ\text{C}$		$I_{DM}$	195	A
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	99	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 30\text{ A}$ , $L = 1\text{ mH}$ ) (Note 4)		$E_{AS}$	450	mJ	
Maximum Lead Temperature for Soldering (1/8" from case for 5 s)		$T_L$	300	$^\circ\text{C}$	

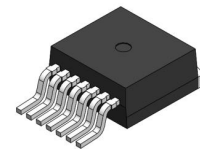
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR-4 board using 1 in 2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4. EAS of 450 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1\text{ mH}$ ,  $I_{AS} = 30\text{ A}$ ,  $V_{DD} = 120\text{ V}$ ,  $V_{GS} = 18\text{ V}$ .

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
1700 V	40 m $\Omega$ @ 20 V	71 A



N-CHANNEL MOSFET



D2PAK-7L  
CASE 418BJ

## MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Lot Traceability
- BG028N170M1 = Specific Device Code

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTBG028N170M1	D2PAK-7L	800 ea/ Tape&Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTBG028N170M1

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Typ	Max	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.35		°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$		40	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1700			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1\text{ mA}$ , referenced to $25^\circ\text{C}$		0.44		V/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 1700\text{ V}$	$T_J = 25^\circ\text{C}$		100	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$		1	mA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = +25/-15\text{ V}, V_{DS} = 0\text{ V}$			$\pm 1$	$\mu\text{A}$

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 20\text{ mA}$	1.8	3.0	4.3	V
Recommended Gate Voltage	$V_{GOP}$		-5		+20	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}, I_D = 60\text{ A}, T_J = 25^\circ\text{C}$		28	40	m $\Omega$
		$V_{GS} = 20\text{ V}, I_D = 60\text{ A}, T_J = 175^\circ\text{C}$		57		
Forward Transconductance	$g_{FS}$	$V_{DS} = 20\text{ V}, I_D = 60\text{ A}$		27		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 800\text{ V}$		4160		pF
Output Capacitance	$C_{OSS}$			200		
Reverse Transfer Capacitance	$C_{RSS}$			15		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 800\text{ V}, I_D = 60\text{ A}$		222		nC
Threshold Gate Charge	$Q_{G(TH)}$			40		
Gate-to-Source Charge	$Q_{GS}$			72		
Gate-to-Drain Charge	$Q_{GD}$			53		
Gate-Resistance	$R_G$		$f = 1\text{ MHz}$		6.1	

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 1200\text{ V}, I_D = 60\text{ A}, R_G = 2\text{ }\Omega$ inductive load		47		ns
Rise Time	$t_r$			18		
Turn-Off Delay Time	$t_{d(OFF)}$			121		
Fall Time	$t_f$			13		$\mu\text{J}$
Turn-On Switching Loss	$E_{ON}$			1311		
Turn-Off Switching Loss	$E_{OFF}$			683		
Total Switching Loss	$E_{tot}$			1994		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Continuous Drain-Source Diode Forward Current	$I_{SD}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$			99	A
Pulsed Drain-Source Diode Forward Current (Note 3)	$I_{SDM}$				195	
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -5\text{ V}, I_{SD} = 60\text{ A}, T_J = 25^\circ\text{C}$		4.3		V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = -5/20\text{ V}, I_{SD} = 60\text{ A}, dI_S/dt = 1000\text{ A}/\mu\text{s}$		33		ns
Reverse Recovery Charge	$Q_{RR}$			247		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS

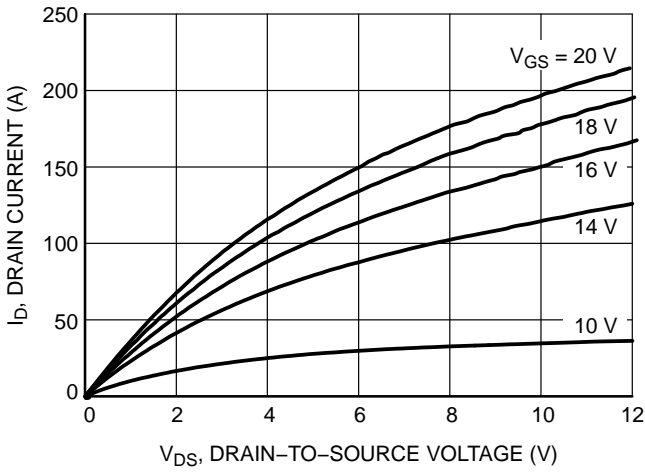


Figure 1. On-Region Characteristics

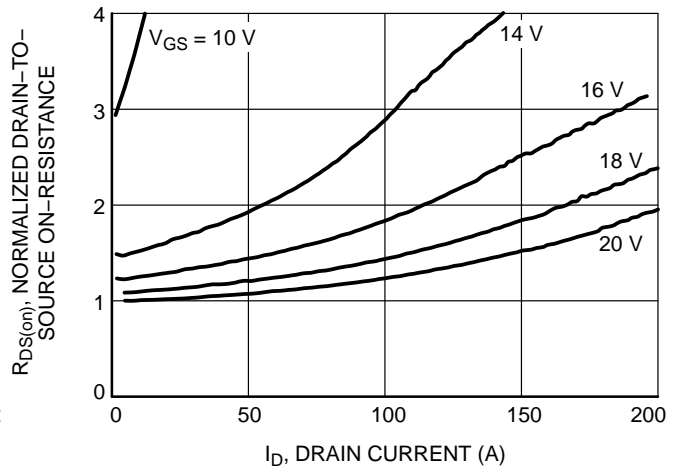


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

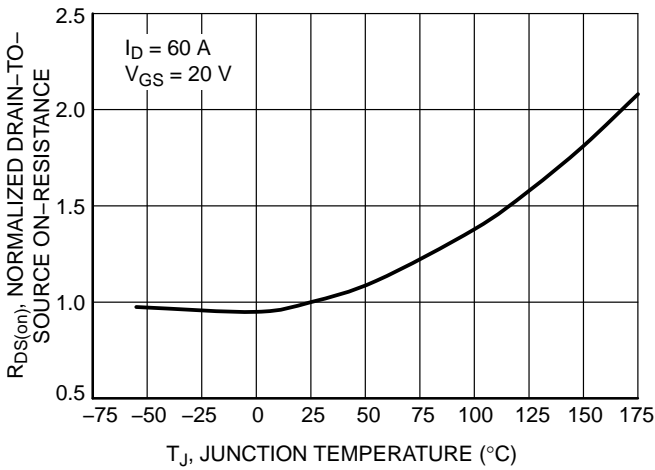


Figure 3. Normalized On-Resistance Variation with Temperature

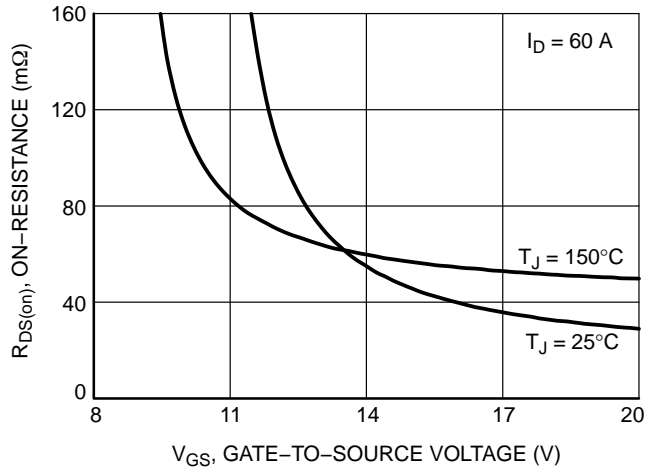


Figure 4. On-Resistance vs. Gate-to-Source Voltage

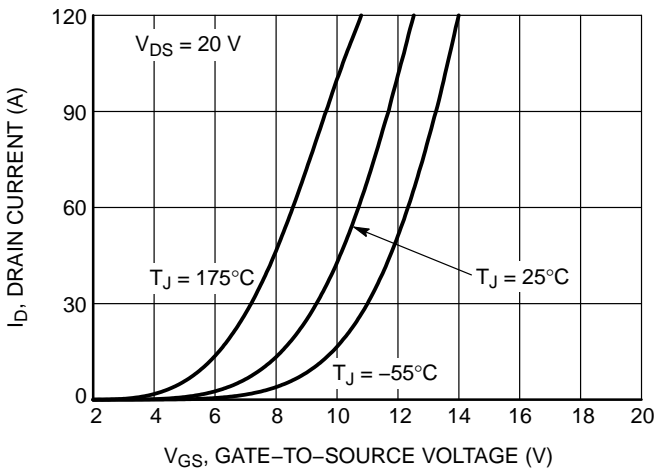


Figure 5. Transfer Characteristics

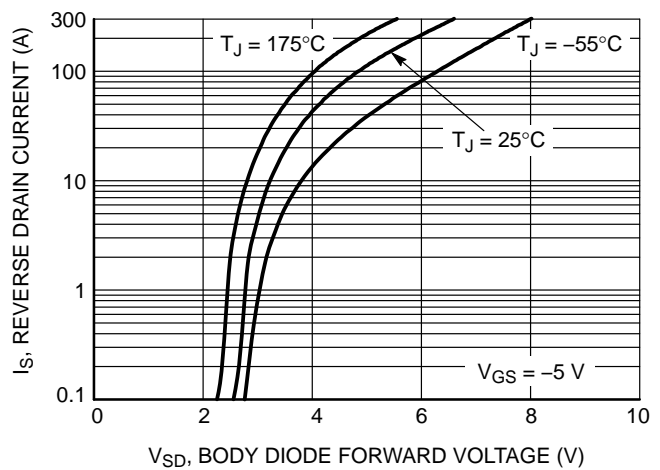


Figure 6. Diode Forward Voltage vs. Current

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## TYPICAL CHARACTERISTICS

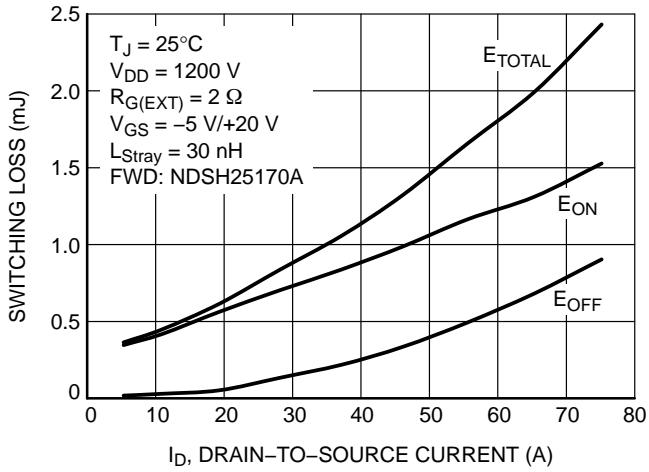


Figure 7. SW Loss vs. ID 25°C

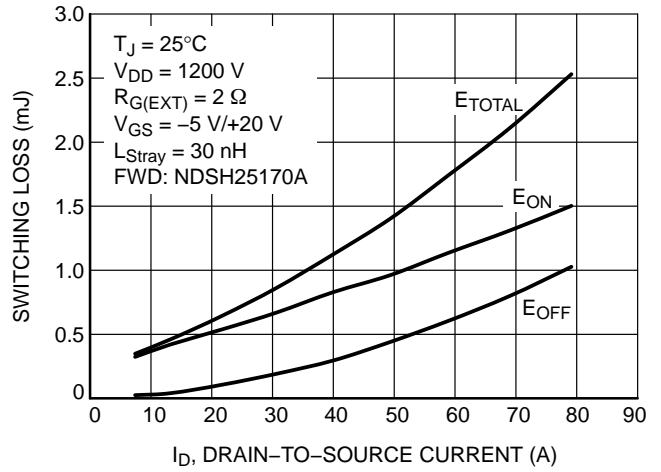


Figure 8. SW Loss vs. ID 125°C

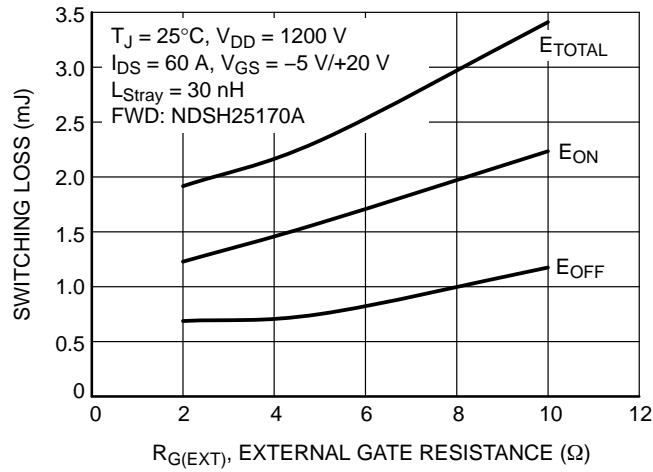
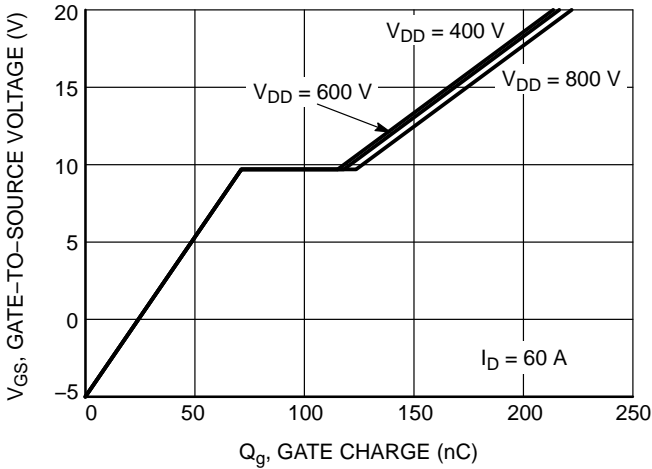


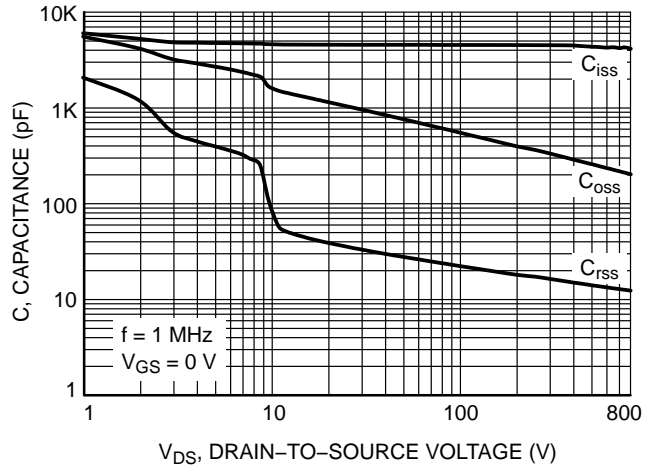
Figure 9. SW Loss vs. Rg

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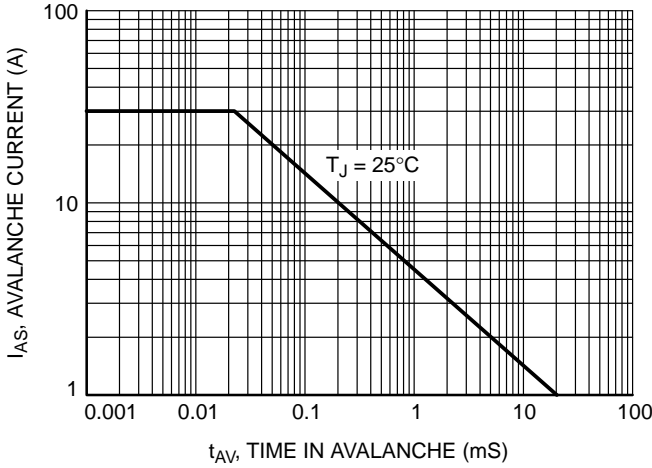
## TYPICAL CHARACTERISTICS



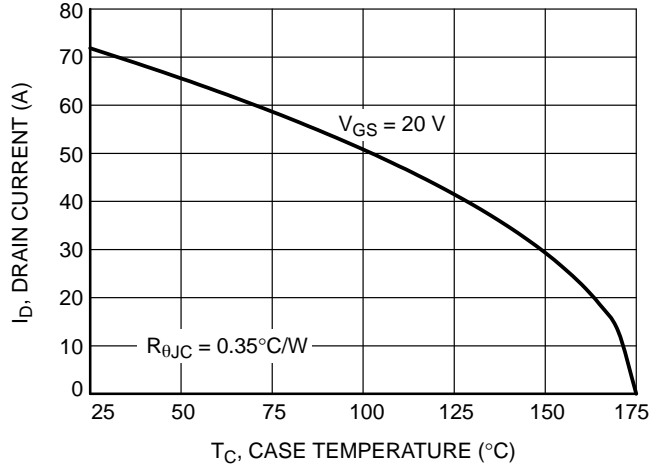
**Figure 10. Gate-to-Source Voltage vs. Total Charge**



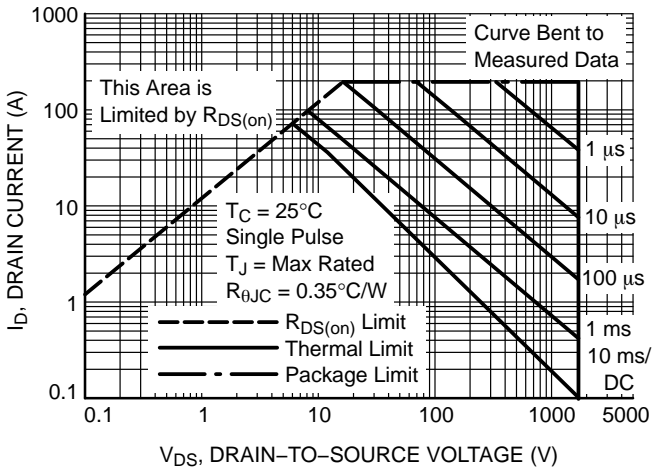
**Figure 11. Capacitance vs. Drain-to-Source Voltage**



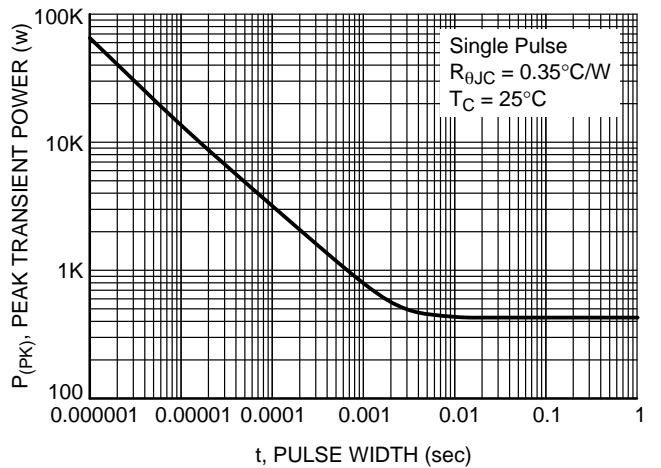
**Figure 12. Unclamped Inductive Switching Capability**



**Figure 13. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 14. Maximum Rated Forward Biased Safe Operating Area**



**Figure 15. Single Pulse Maximum Power Dissipation**

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## TYPICAL CHARACTERISTICS

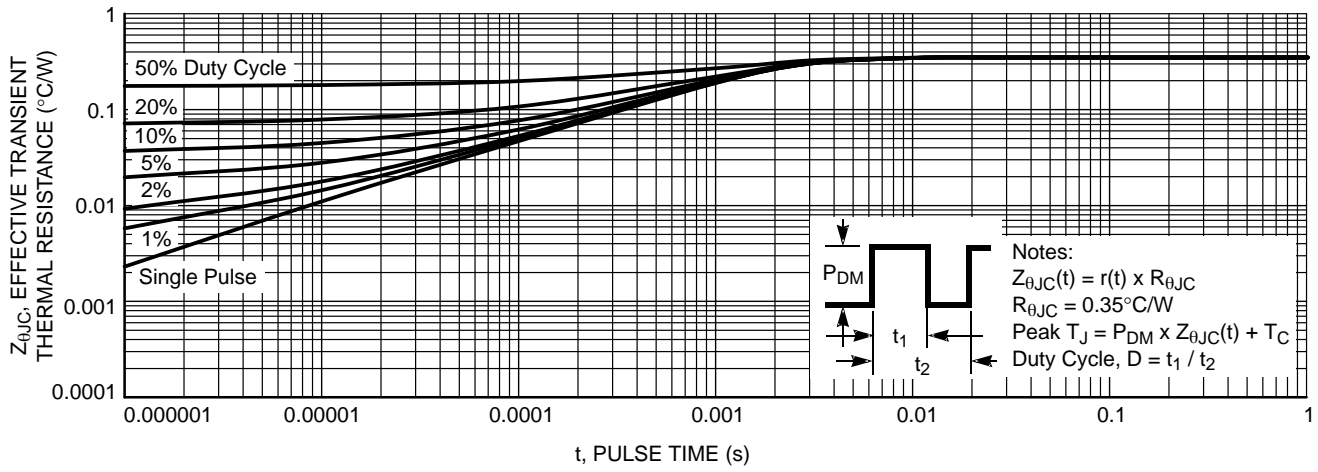


Figure 16. Transient Thermal Impedance

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## D<sup>2</sup>PAK7 (TO-263-7L HV) CASE 418BJ ISSUE B

DATE 16 AUG 2019



NOTES:

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25



### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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<b>DESCRIPTION:</b>	<b>D<sup>2</sup>PAK7 (TO-263-7L HV)</b>	<b>PAGE 1 OF 1</b>

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