

# NTD14N03R

## Power MOSFET 14 Amps, 25 Volts N-Channel DPAK

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{iss}$  to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	25	vdc
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	vdc
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	6.0	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	20.8	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ , Chip	$I_D$	14	A
– Continuous @ $T_A = 25^\circ\text{C}$ , Limited by Package	$I_D$	11.4	A
– Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_D$	28	A
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.56	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	3.1	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	120	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.04	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	2.5	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

1. When surface mounted to an FR4 board using 0.5 sq. in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.

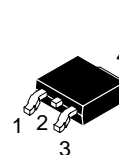
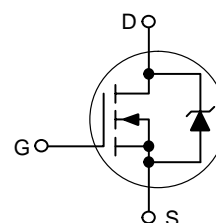


ON Semiconductor®

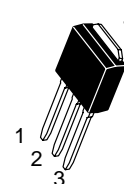
<http://onsemi.com>

**14 AMPERES, 25 VOLTS**  
 **$R_{DS(on)} = 70.4 \text{ m}\Omega$  (Typ)**

N-CHANNEL

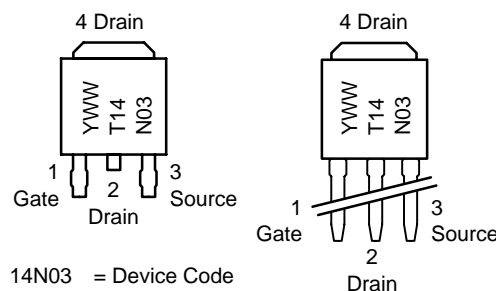


**CASE 369C**  
**DPAK**  
**(Surface Mount)**  
**STYLE 2**



**CASE 369D**  
**DPAK**  
**(Straight Lead)**  
**STYLE 2**

### MARKING DIAGRAM & PIN ASSIGNMENTS



14N03 = Device Code  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
NTD14N03R	DPAK	75 Units/Rail
NTD14N03R-1	DPAK Straight Lead	75 Units/Rail
NTD14N03RT4	DPAK	2500 Tape & Reel

# NTD14N03R

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\ \mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(br)DSS}$	25 –	28 –	– –	Vdc mV/°C
Zero Gate Voltage Drain Current ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 150^\circ\text{C}$ )	$I_{DSS}$	– –	– –	1.0 10	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = \pm 20\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	$\pm 100$	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ( $V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{Adc}$ ) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 –	1.5 –	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 5\text{ Adc}$ ) ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 5\text{ Adc}$ )	$R_{DS(on)}$	– –	117 70.4	130 95	m $\Omega$
Forward Transconductance (Note 3) ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 5\text{ Adc}$ )	$g_{FS}$	–	7.0	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ )	$C_{iss}$	–	115	–	pF
Output Capacitance		$C_{oss}$	–	62	–	
Transfer Capacitance		$C_{rss}$	–	33	–	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{GS} = 10\text{ Vdc}$ , $V_{DD} = 10\text{ Vdc}$ , $I_D = 5\text{ Adc}$ , $R_G = 3\ \Omega$ )	$t_{d(on)}$	–	3.8	–	ns
Rise Time		$t_r$	–	27	–	
Turn-Off Delay Time		$t_{d(off)}$	–	9.6	–	
Fall Time		$t_f$	–	2.0	–	
Gate Charge	$(V_{GS} = 5\text{ Vdc}$ , $I_D = 5\text{ Adc}$ , $V_{DS} = 10\text{ Vdc}$ ) (Note 3)	$Q_T$	–	1.8	–	nC
		$Q_1$	–	0.8	–	
		$Q_2$	–	0.7	–	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 5\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ ) (Note 3) $(I_S = 5\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$V_{SD}$	– –	0.93 0.82	1.2 –	Vdc
Reverse Recovery Time	$(I_S = 5\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $di_S/dt = 100\text{ A}/\mu\text{s}$ ) (Note 3)	$t_{rr}$	–	6.6	–	ns
		$t_a$	–	4.75	–	
		$t_b$	–	1.88	–	
Reverse Recovery Stored Charge		$Q_{RR}$	–	0.002	–	$\mu\text{C}$

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

# NTD14N03R

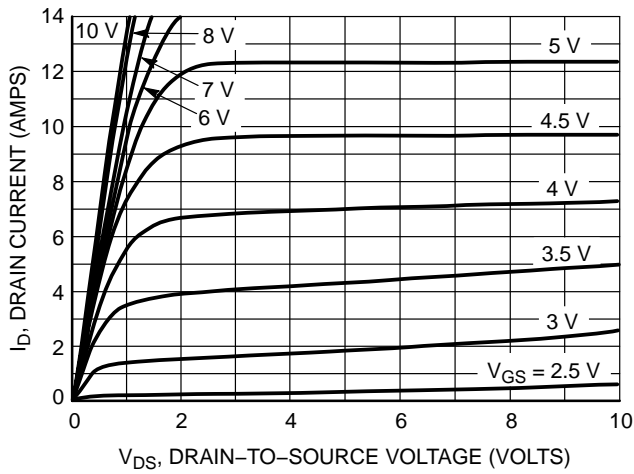


Figure 1. On-Region Characteristics

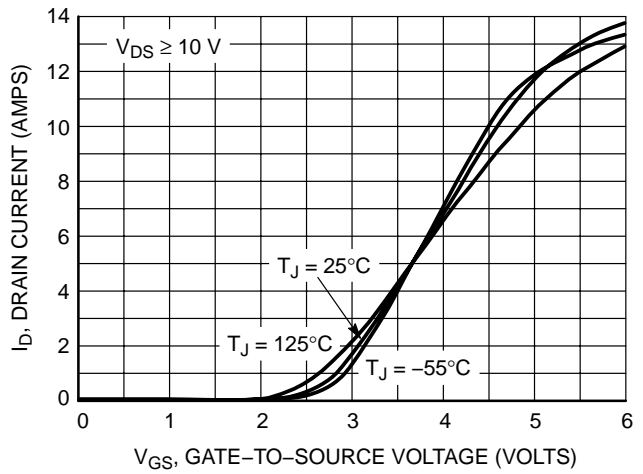


Figure 2. Transfer Characteristics

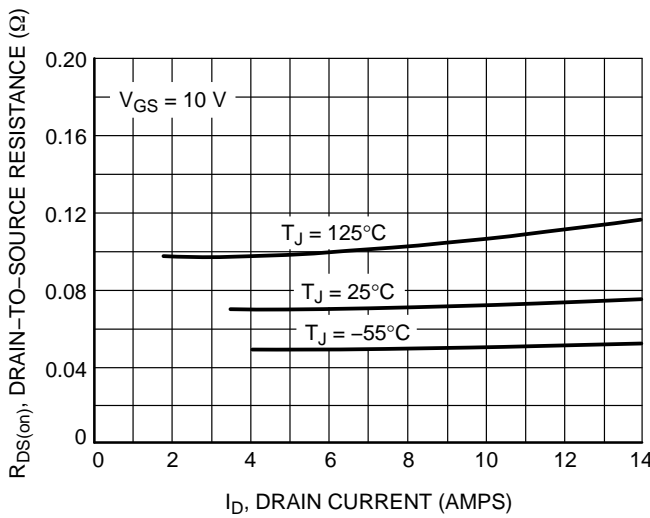


Figure 3. On-Resistance versus Drain Current and Temperature

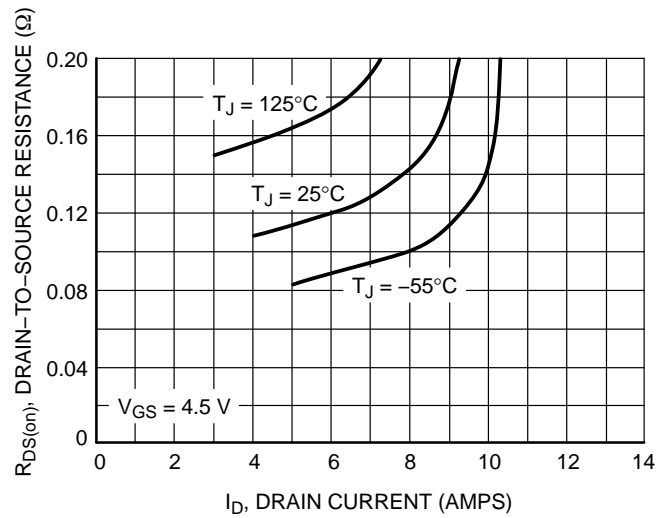


Figure 4. On-Resistance versus Drain Current and Temperature

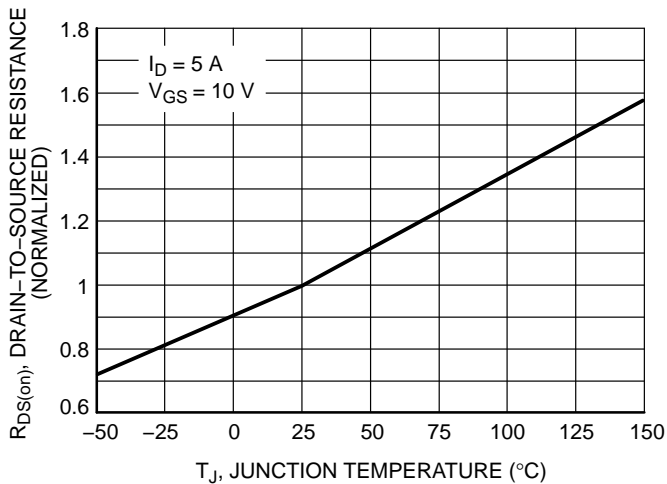


Figure 5. On-Resistance Variation with Temperature

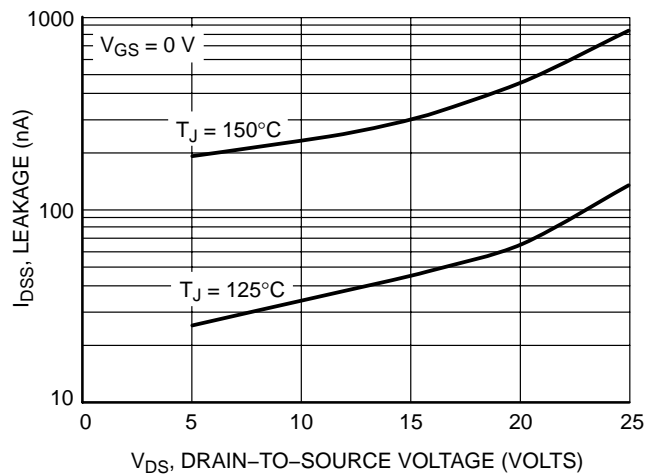
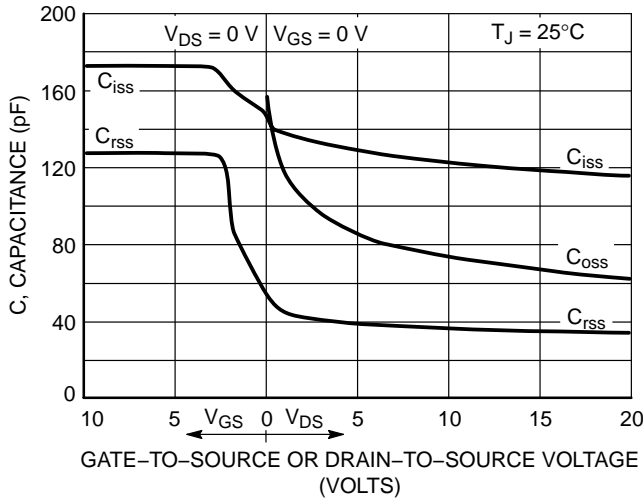
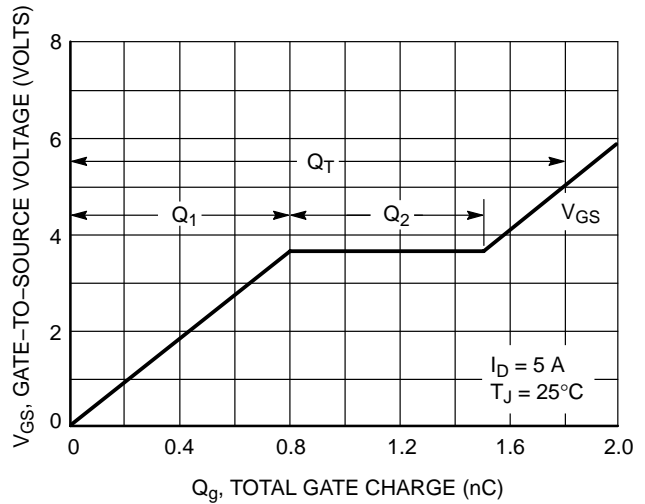


Figure 6. Drain-to-Source Leakage Current versus Voltage

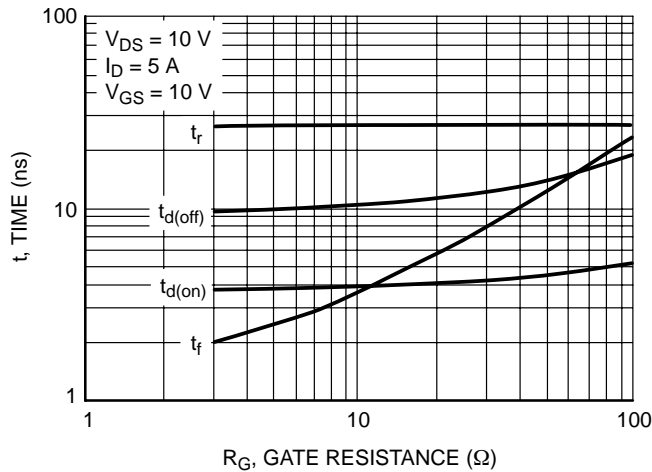
# NTD14N03R



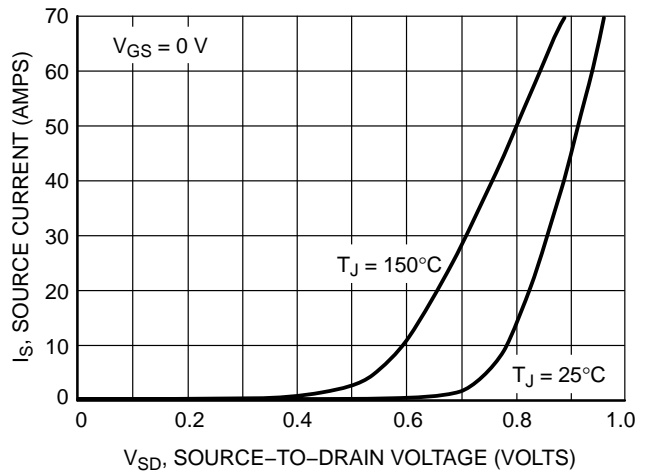
**Figure 7. Capacitance Variation**



**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

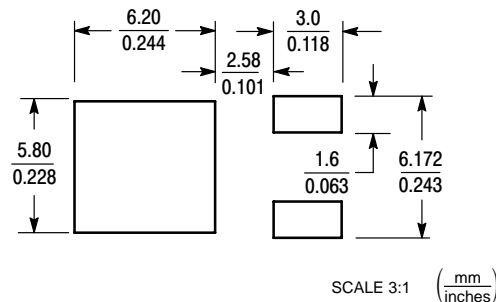


**Figure 10. Diode Forward Voltage versus Current**

## RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

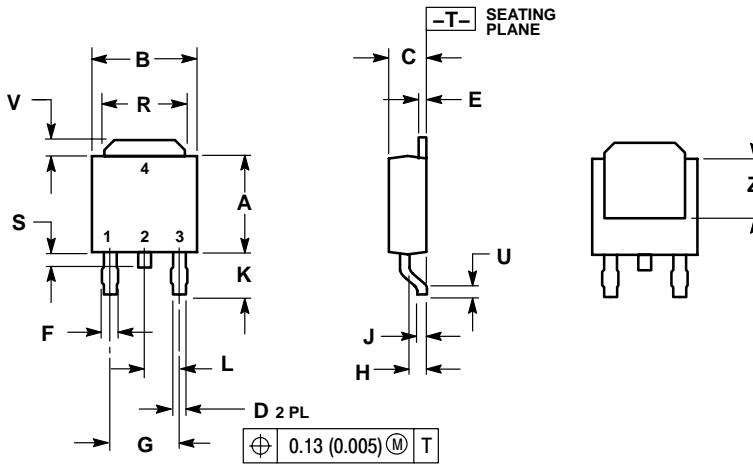
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



# NTD14N03R

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369C ISSUE O



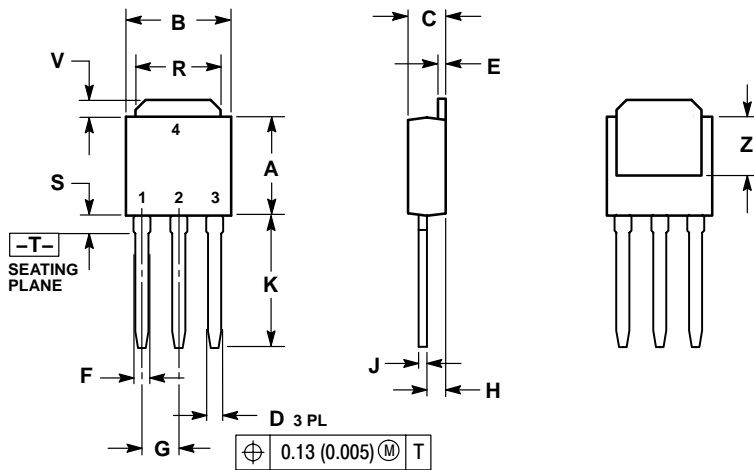
- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### DPAK (SINGLE GAUGE) CASE 369D ISSUE O

SCALE 1:1



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

# NTD14N03R

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA

**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada

**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada

**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your  
local Sales Representative.

**NTD14N03R/D**