MOSFET - Power, N-Channel, SUPERFET® III, FAST

650 V, 360 mΩ, 10 A

NTD360N65S3H

ON Semiconductor®

www.onsemi.com

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III FAST MOSFET series helps minimize various power systems and improve system efficiency.

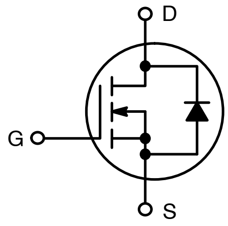
Features

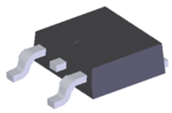
- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 296 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 17.5 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 180 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter

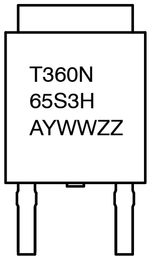
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	360 mΩ @ 10 V	10 A





D−PAK
CASE 369AS

MARKING DIAGRAM



T360N65S3H = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

March, 2021 − Rev. 2

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	10	A
		Continuous (T_C = 100°C)	6	
I_{DM}	Drain Current	Pulsed (Note 1)	28	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		75	mJ
I_{AS}	Avalanche Current (Note 2)		1.9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.83	mJ
dv/dt	MOSFET dv/dt		120	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	83	W
		Derate Above 25°C	0.66	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 s		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 1.9 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le 5.0$ A, di/dt ≤ 200 A/μs, $V_{DD} \le 400$ V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.51	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

4. Device on 1 in^2 pad 2 oz copper pad on 1.5 × 1.5 in. board of FR−4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping†
NTD360N65S3H	T360N65S3H	D−PAK	330 mm	16 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	0.63	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	3	μA
		V_{DS} = 520 V, T_C = 125°C	–	2.6	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.7 mA	2.4	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 5.0 A	–	296	360	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 5.0 A	–	11.2	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz	–	916	–	pF
C_{oss}	Output Capacitance		–	15	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	180	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	24	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 5.0 A, V_{GS} = 10 V (Note 5)	–	17.5	–	nC
Q_{gs}	Gate to Source Gate Charge		–	4.3	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	5	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.9	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 5.0 A, V_{GS} = 10 V, R_g = 12 Ω (Note 5)	–	15	–	ns
t_r	Turn-On Rise Time		–	6.7	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	45	–	ns
t_f	Turn-Off Fall Time		–	7	–	ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	10	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	28	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 5.0 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 5.0 A, dI_F/dt = 100 A/μs	–	204	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.8	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

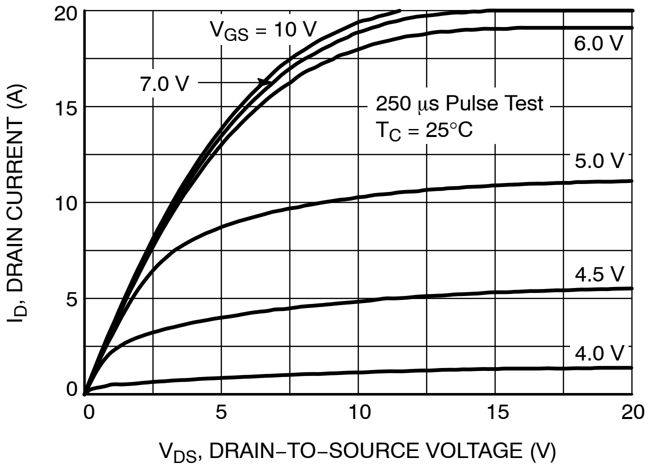


Figure 1. On−Region Characteristics

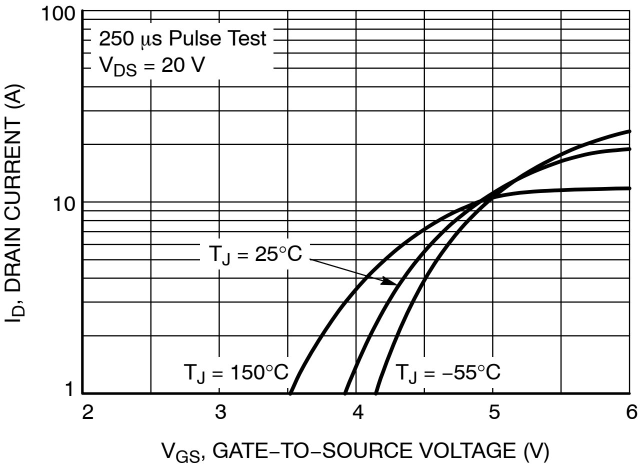


Figure 2. Transfer Characteristics

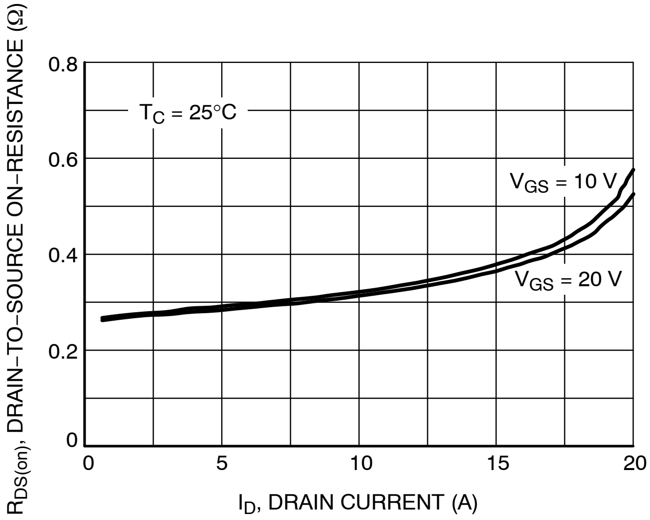


Figure 3. On Resistance Variation vs. Drain Current and Gate Voltage

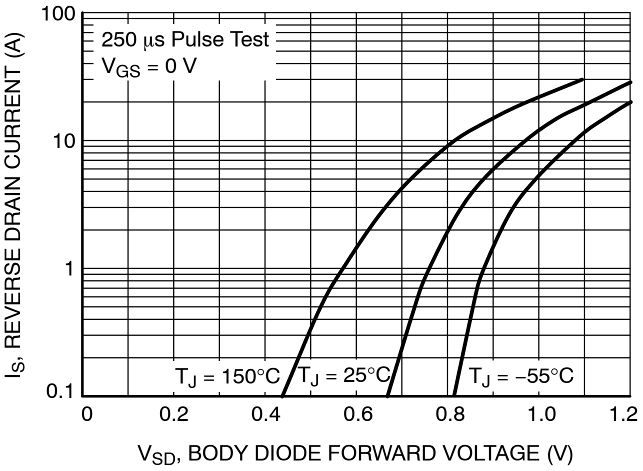


Figure 4. Diode Forward Voltage Variation vs. Source Current and Temperature

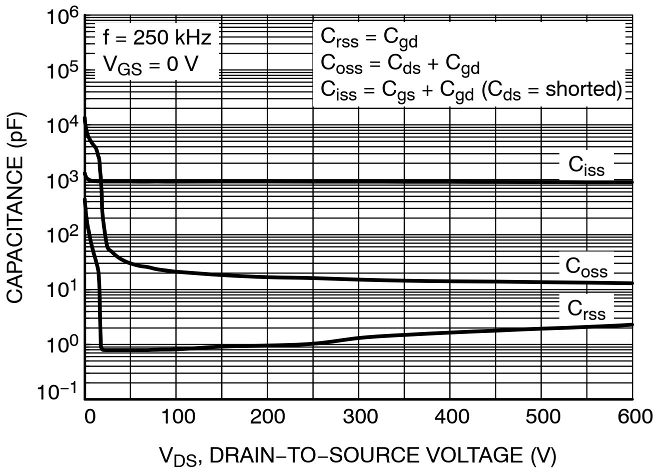


Figure 5. Capacitance Characteristics

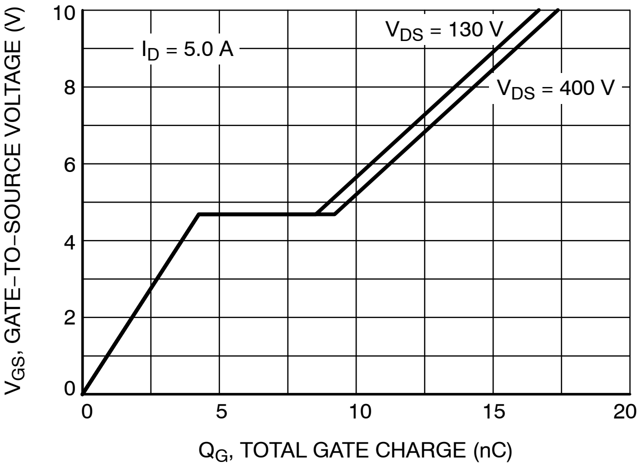


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

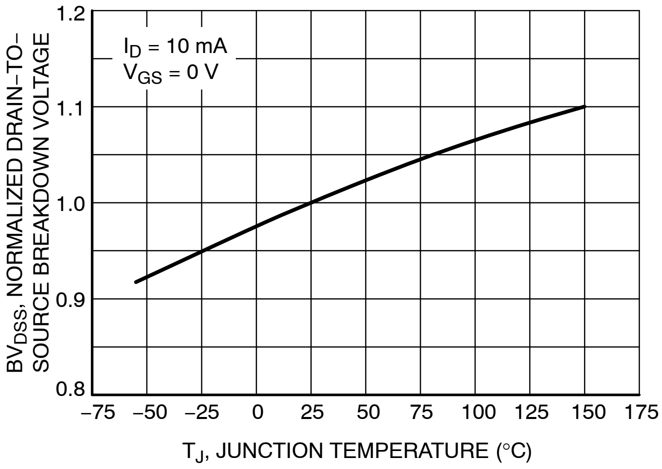


Figure 7. Breakdown Voltage Variation vs. Temperature

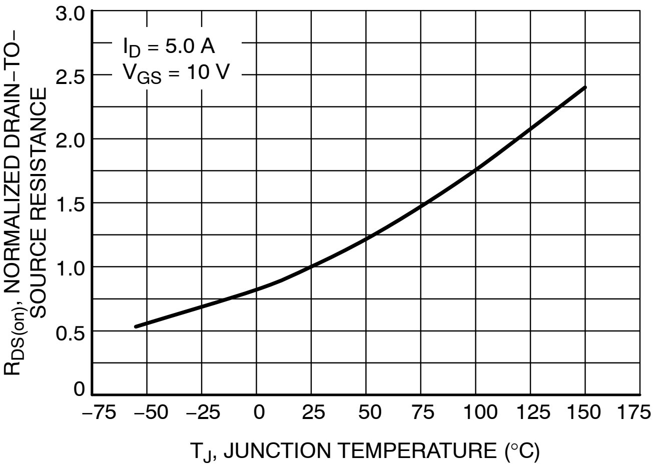


Figure 8. On−Resistance Variation vs. Temperature

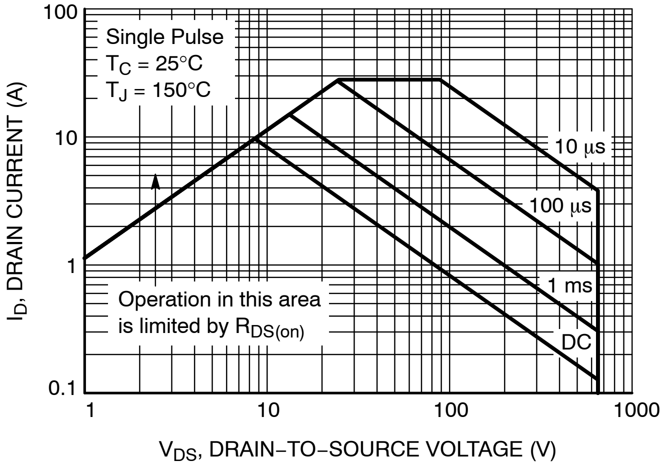


Figure 9. Maximum Safe Operating Area

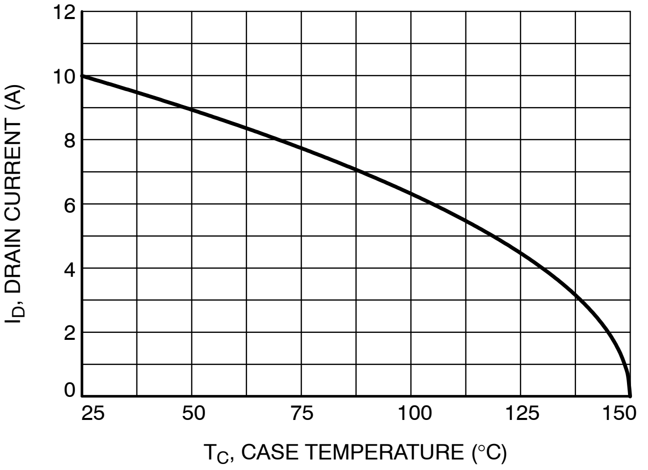


Figure 10. Maximum Drain Current vs. Case Temperature

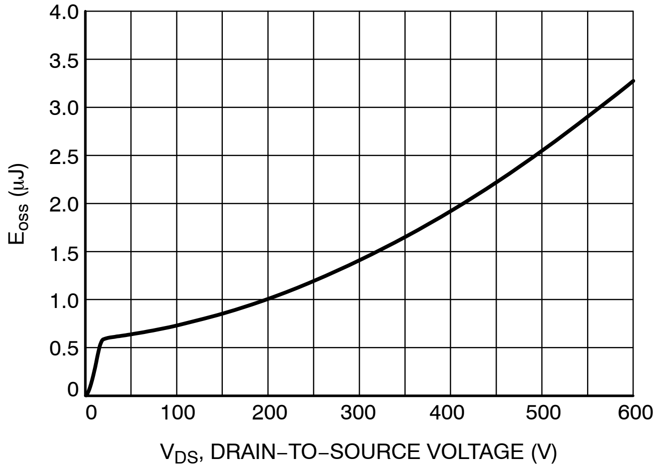


Figure 11. E_{oss} vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

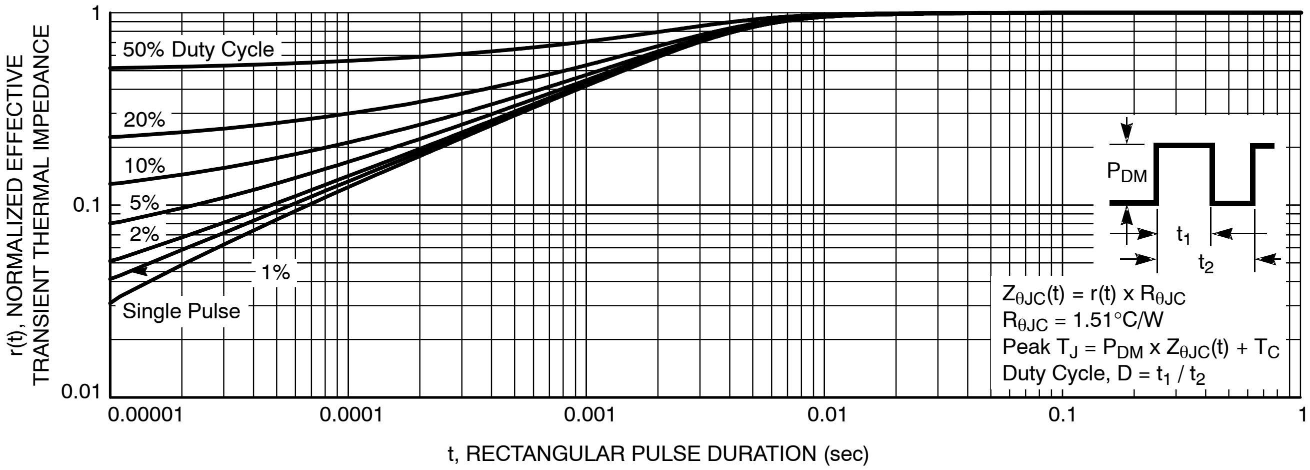


Figure 12. Transient Thermal Response Curve

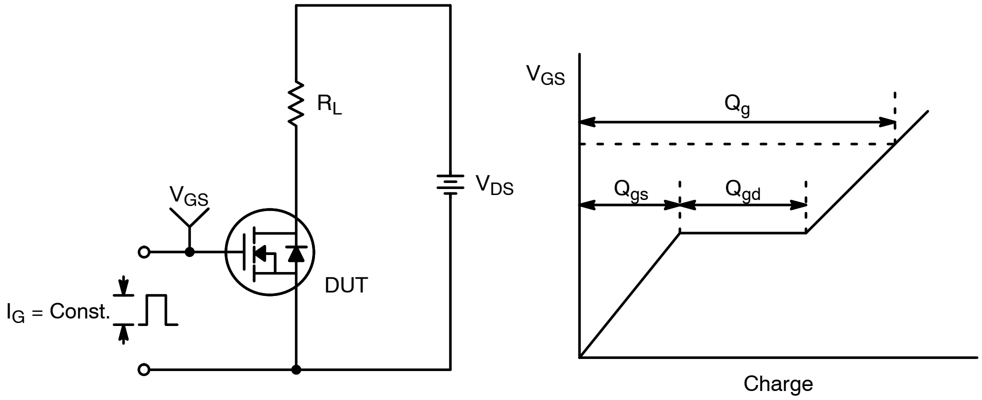


Figure 13. Gate Charge Test Circuit & Waveform

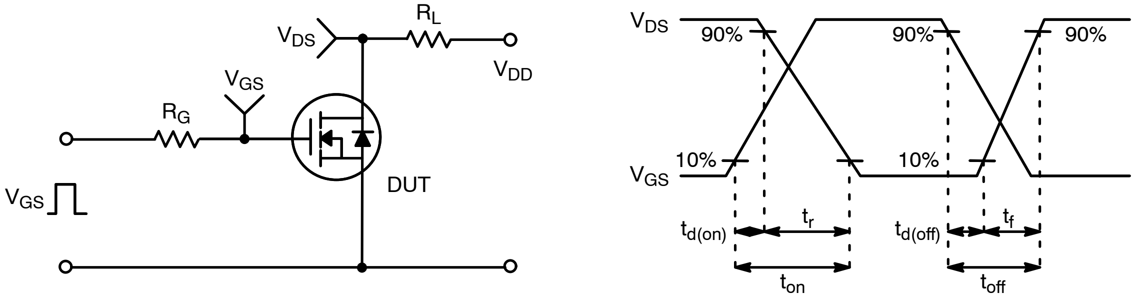


Figure 14. Resistive Switching Test Circuit & Waveforms

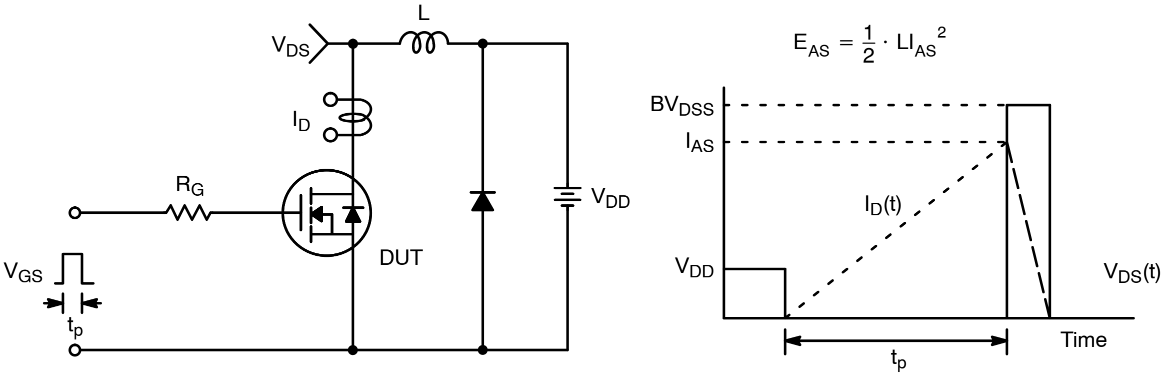


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

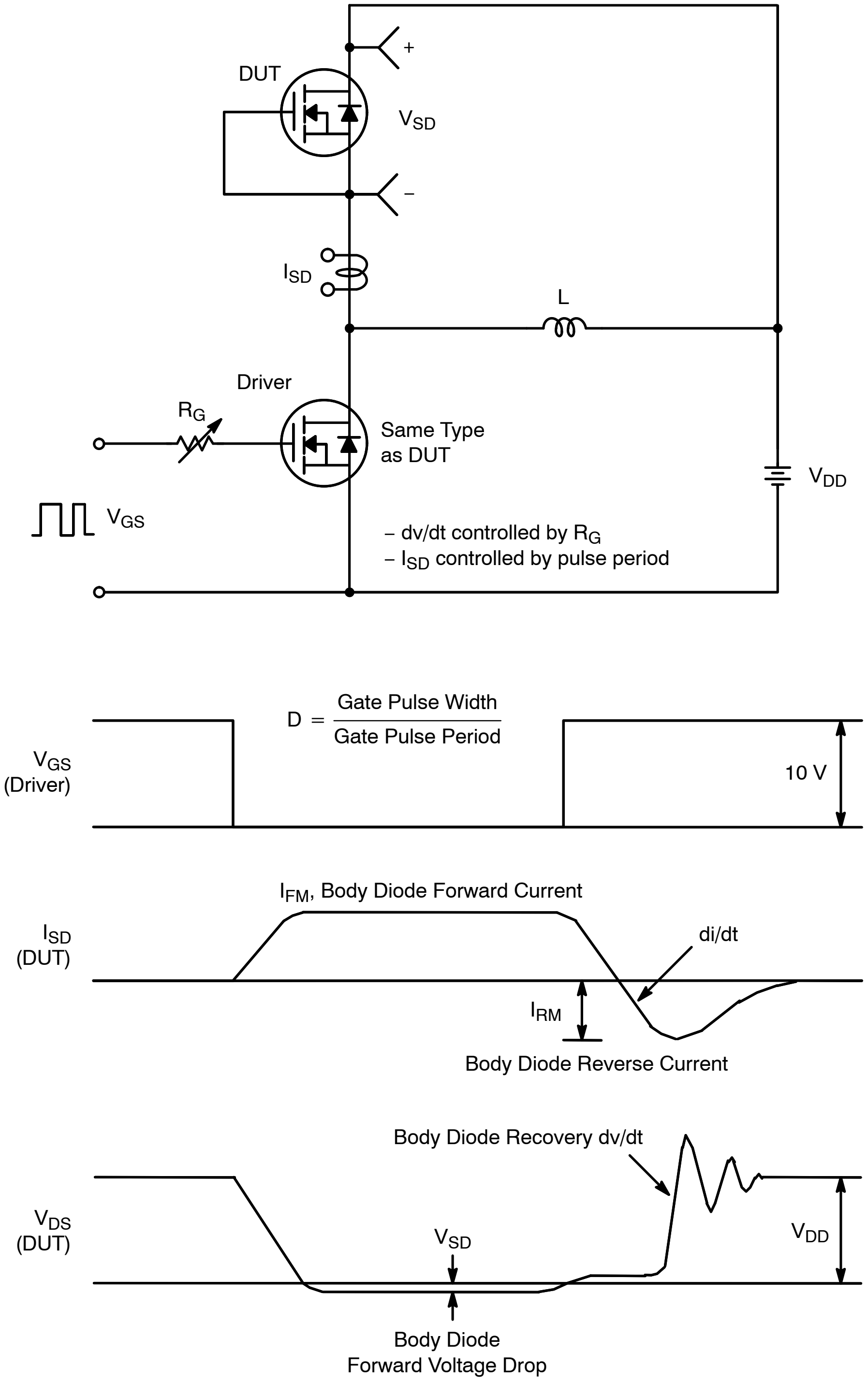
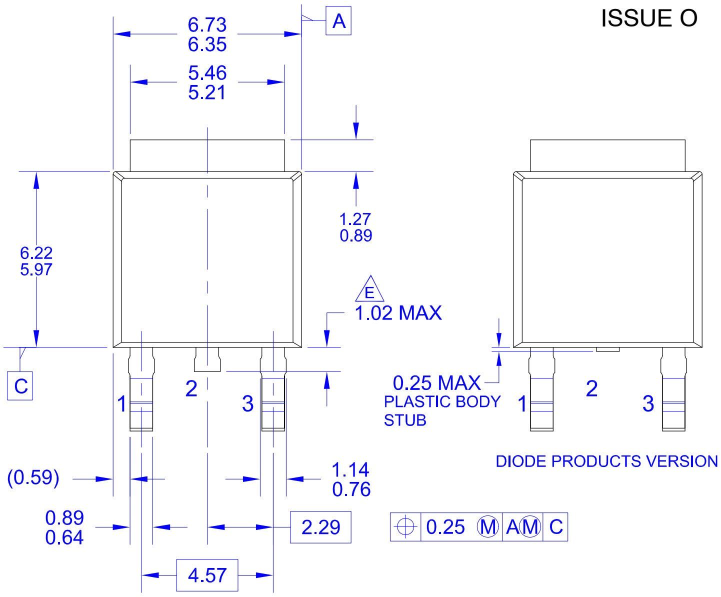


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

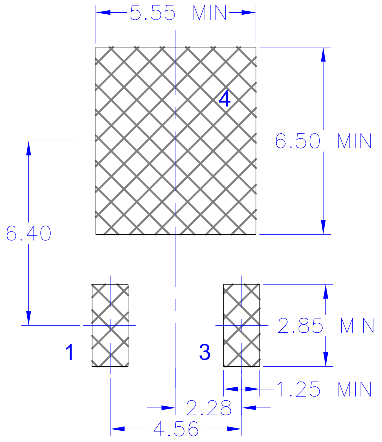
PACKAGE DIMENSIONS

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O

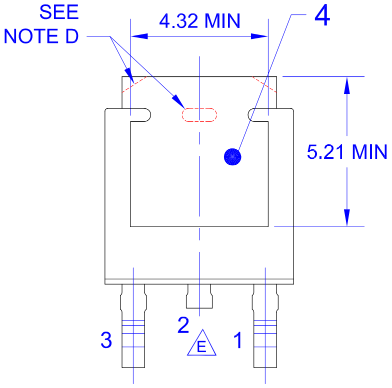


NON-DIODE PRODUCTS VERSION

DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



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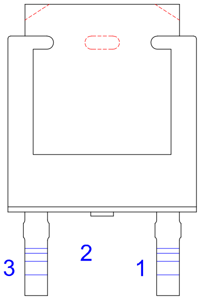
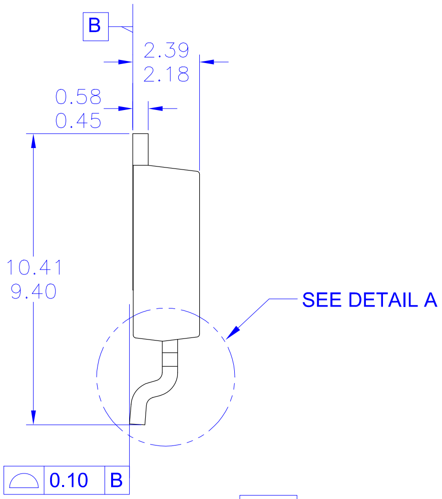
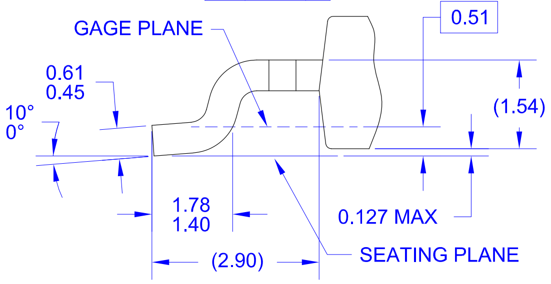


DIODE PRODUCTS VERSION





DETAIL A
(ROTATED -90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

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