

NTD5862N, NTP5862N

MOSFET – Power, N-Channel

60 V, 98 A, 5.7 mΩ



ON Semiconductor®

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Features

- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	5.7 mΩ @ 10 V	98 A

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

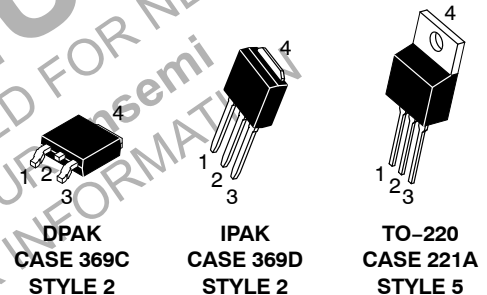
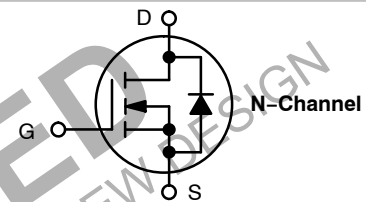
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Gate-to-Source Voltage – Non-Repetitive ($t_p < 10 \mu\text{s}$)	V_{GS}	± 30	V
Continuous Drain Current ($R_{\theta JC}$) (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	I_D 98 A
		$T_C = 100^\circ\text{C}$	69
Power Dissipation ($R_{\theta JC}$)		$T_C = 25^\circ\text{C}$	P_D 115 W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	335 A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	96	A
Single Pulse Drain-to-Source Avalanche Energy ($L = 0.3 \text{ mH}$)	E_{AS}	205	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

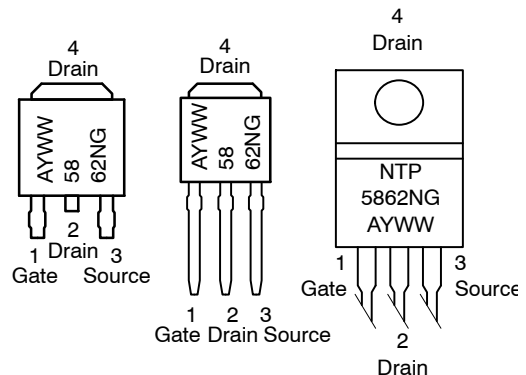
THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.3	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	37	

1. Limited by package to 50 A continuous.
2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).



MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
 Y = Year
 WW = Work Week
 5862N = Device Code
 G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			47		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25°C		1.0	μA
			T _J = 150°C		100	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	2.0		4.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-9.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 45 A		4.4	5.7	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 10 A		18		S

CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		5050	6000	pF
Output Capacitance	C _{oss}			500	600	
Reverse Transfer Capacitance	C _{rss}			300	420	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 45 A		82		nC
Threshold Gate Charge	Q _{G(TH)}			5.2		
Gate-to-Source Charge	Q _{GS}			24		
Gate-to-Drain Charge	Q _{GD}			27		
Gate Resistance	R _G			0.6		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 48 V, I _D = 45 A, R _G = 2.5 Ω		18		ns
Rise Time	t _r			70		
Turn-Off Delay Time	t _{d(off)}			35		
Fall Time	t _f			60		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 45 A	T _J = 25°C		0.9	1.2	V
			T _J = 100°C		0.75		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 45 A		38		ns	
Charge Time	t _a			20			
Discharge Time	t _b			18			
Reverse Recovery Charge	Q _{RR}			40			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

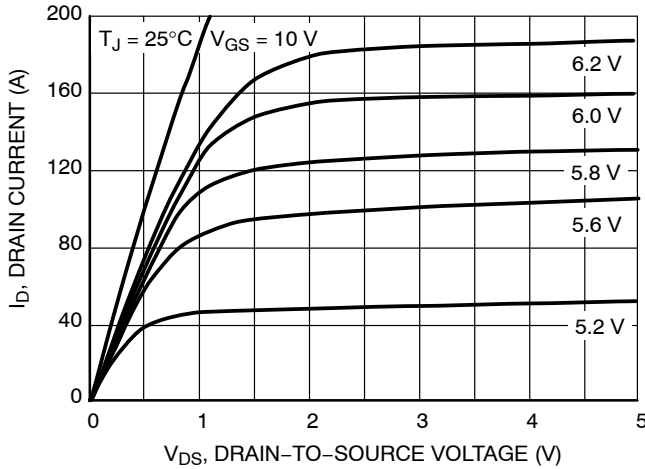


Figure 1. On-Region Characteristics

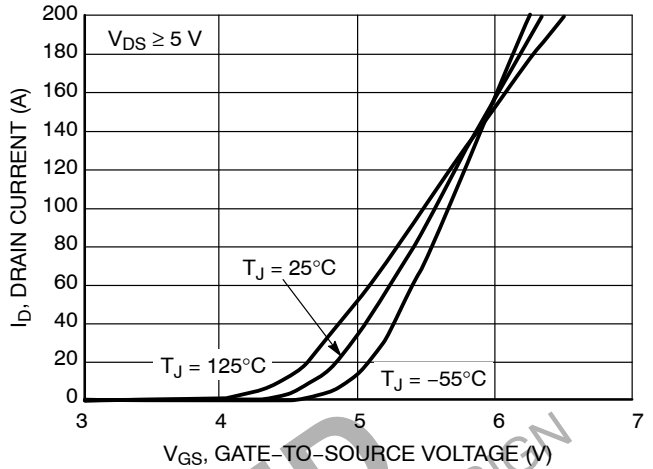


Figure 2. Transfer Characteristics

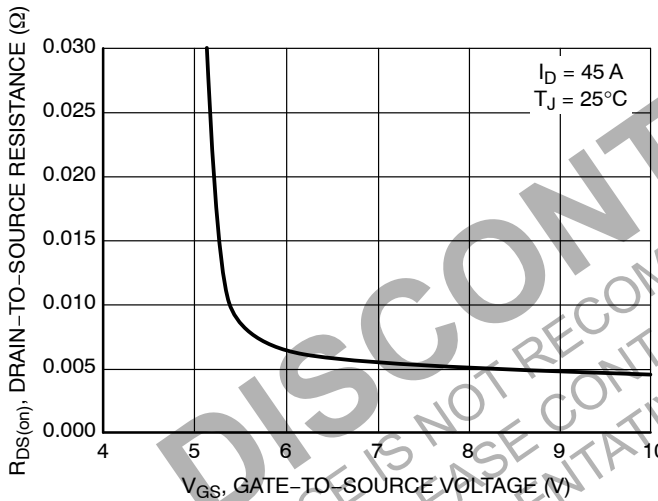


Figure 3. On-Resistance vs. Gate Voltage

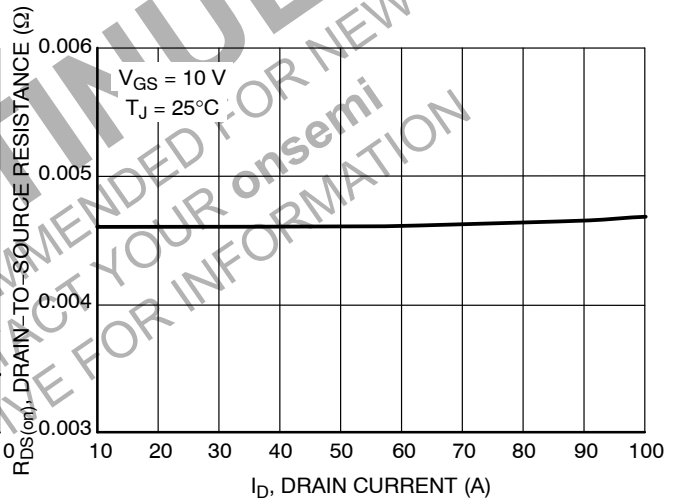


Figure 4. On-Resistance vs. Drain Current

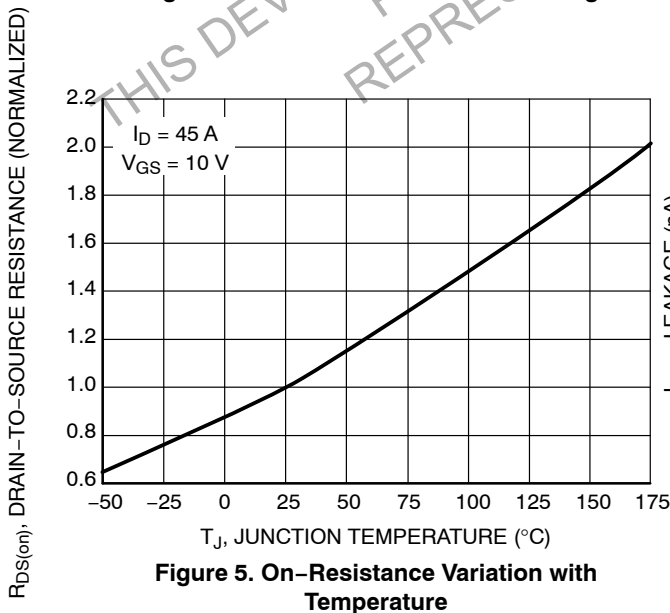


Figure 5. On-Resistance Variation with Temperature

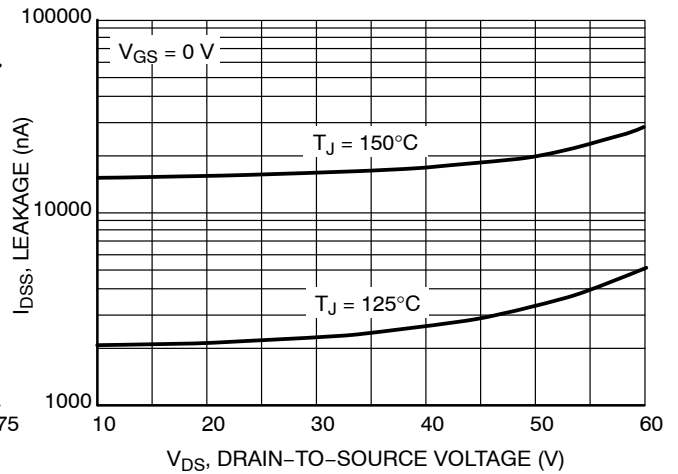


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

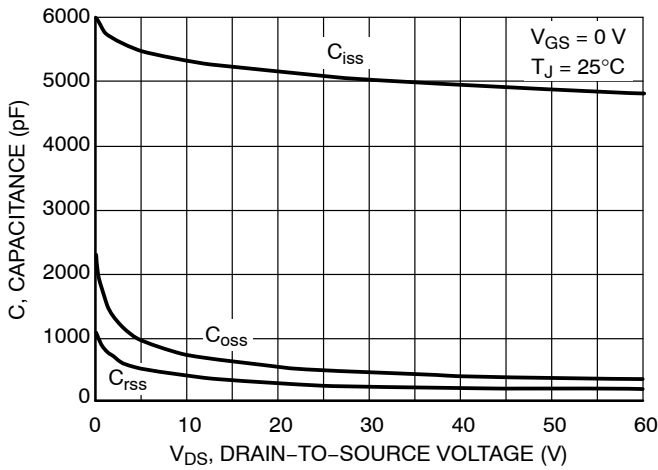


Figure 7. Capacitance Variation

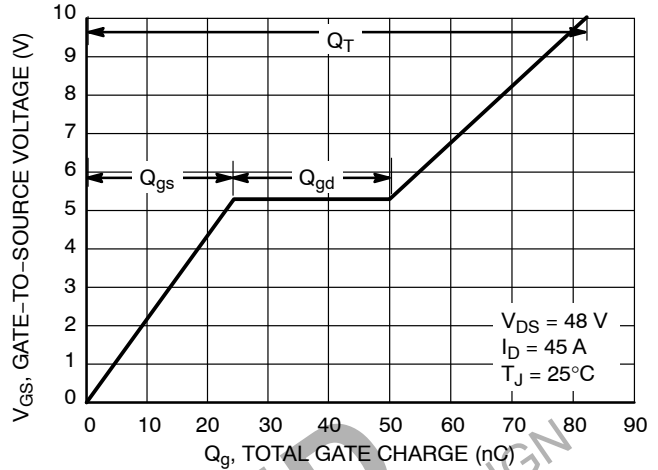


Figure 8. Gate-to-Source vs. Total Charge

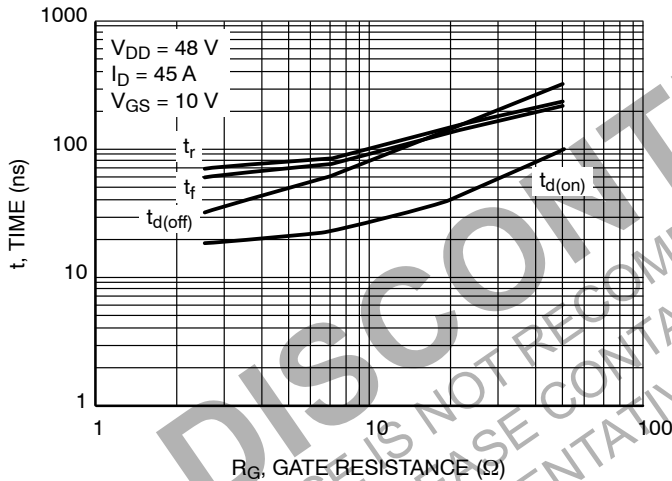


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

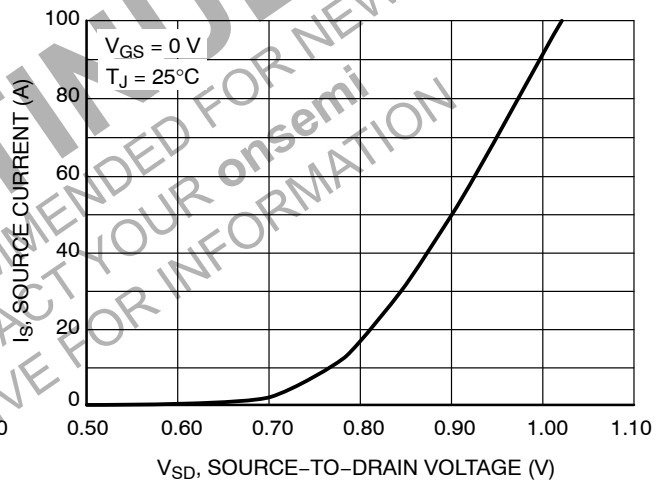


Figure 10. Diode Forward Voltage vs. Current

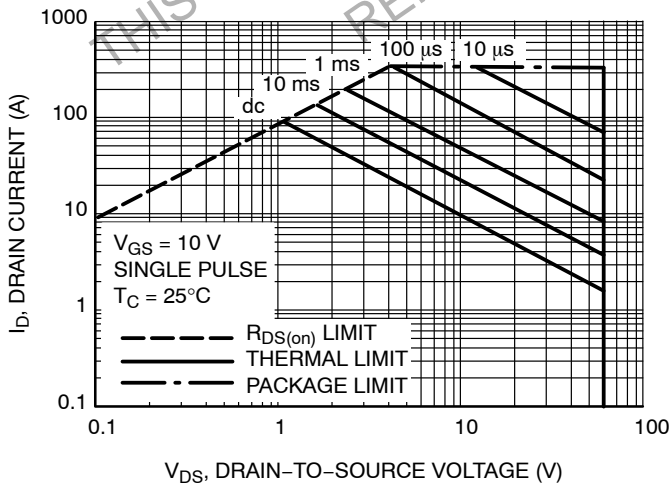


Figure 11. Maximum Rated Forward Biased Safe Operating Area

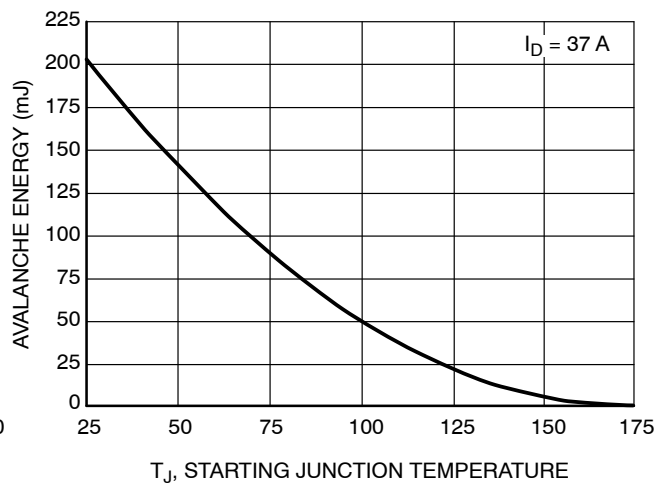


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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TYPICAL CHARACTERISTICS

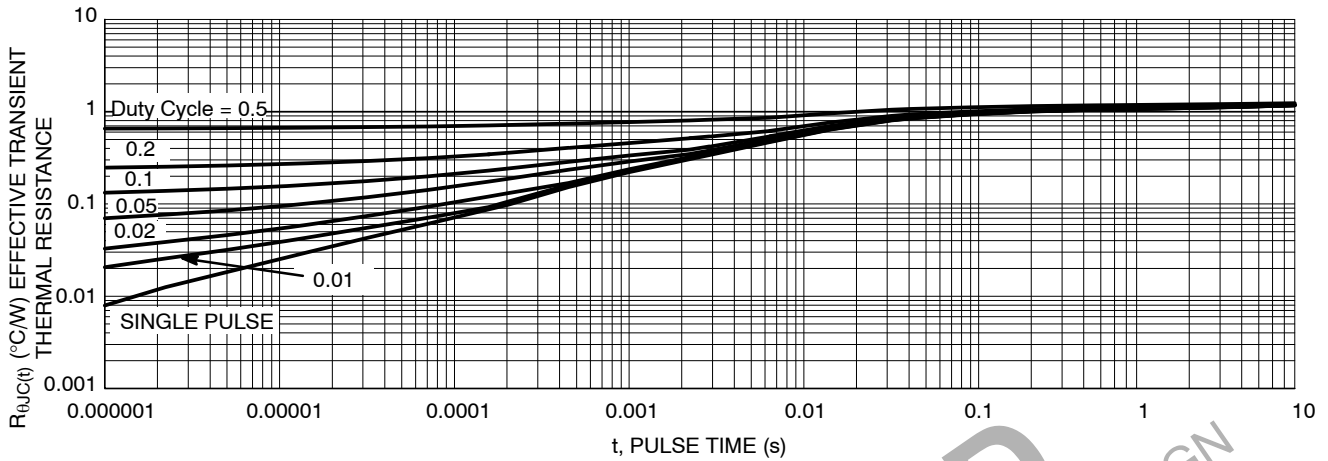


Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NTD5862N-1G	IPAK (Straight Lead) (Pb-Free)	75 Units / Rail
NTD5862NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTP5862NG	TO-220 (Pb-Free)	50 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

MARKING DIAGRAMS



- xxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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