ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE15042
Integrated Circuit
Digital Tuning System Interface for TV Systems

Description:

The NTE15042 is an integrated circuit in a 16–Lead DIP type package developed to facilitate the Phase Lock Loop (PLL) digital tuning system interface for TV systems. Since all the peripheral blocks are incorporated into this device, the number of peripheral parts can be greatly reduced.

Features:

- All–in–One Chip Incorporating the Peripheral Blocks of the PLL System
- Built–In Synchronized Separate for Channel Detecting Circuit
- Externally Controllable Channel Detection Level
- High Current Low–Saturation–Voltage Band Switch Output: $V_{O(sat)}$ = 0.3V Typ @ I_{OH} = –40mA
- Built–In Channel Tuning Voltage: 34V Typ

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Supply Voltage, V_{CC1} 14.4V
Band Output Current, I_{OH} . . . . . –60mA
Band Output Applied Voltage, V_{OL} . . . . . –15V
Zener Terminal Current, I_z 15mA
Channel Detection Output Applied Voltage, V_{OH} . . . . . V_{CC1} V
Band Input Voltage, V_I . . . . . 0 to V_{CC1} V
Video Signal Input Voltage, V_{CV} . . . . . 0 to 5V
Error Amplifier Input Voltage, V_{AI} . . . . . 0 to V_{CC1} V
Error Amplifier Output Current, I_{AO} . . . . . –5mA
Flyback Pulse Input Voltage, V_{FBP} . . . . . V_{CC1} V_P
Allowable Power Dissipation (T_A = +60°C), P_D 600mW
Operating Temperature Range, T_{opr} . . . . . –20° to +65°C
Storage Temperature Range, T_{stg} . . . . . –40° to +150°C

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC1}	8.1	12.0	13.2	V
Band Signal High–Level Input Voltage	e_{BIH} (V_1H, V_2H)	3.1	–	5.5	V
Band Signal Low–Level Input Voltage	e_{BIL} (V_1L, V_2L)	0	–	0.8	V
Video Signal Input Voltage	e_{iv} (V_3)	–	2	–	$V_{P–P}$
Flyback Pulse High–Level Input Voltage	e_{FBPH} (V_4H)	5.0	–	8.0	V
Flyback Pulse Low–Level Input Voltage	e_{FBPL} (V_4L)	0	–	0.7	V
Incoming Current to Pin11	I_{11}	5	–	6	mA

Electrical Characteristics: (T_A = +25°C ±3°C, V_{CC} = 12V unless otherwise specified)

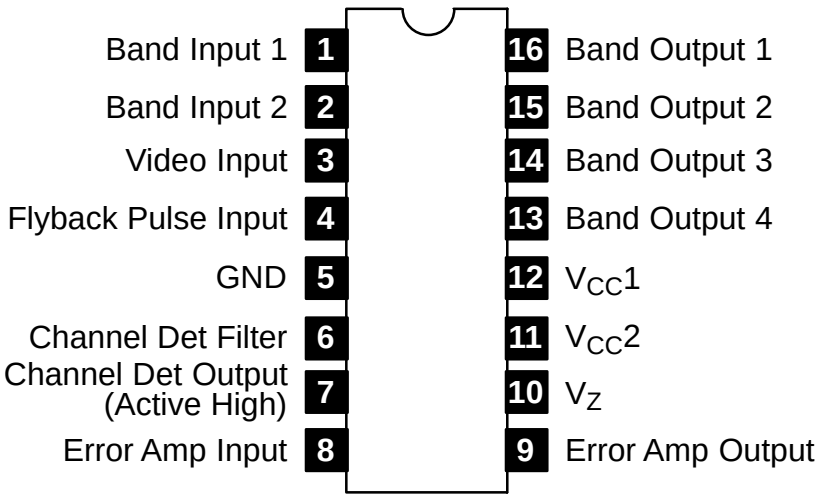
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	I_{CC}	Error amp output (High) connected to the band output V_{CC}	2.0	6.0	12.0	mA
Band Input Threshold Voltage	V_{ITH}		1.0	2.0	3.0	V
Band Output Saturation Voltage	$V_{O(sat)}$	I_{OH} = –40mA, I_{11} = 5mA	–	0.3	0.7	V
Band Output Leakage Current	I_{OL}	V_{OL} = –15V	–	–	–50	µA
Zener Stabilization Voltage	V_Z	I_Z = 5mA	32	34	36	V
Stabilization Voltage Temperature Factor	$\Delta V_Z/\Delta T$	T_A = –20° to +65°C, I_Z = 5mA	–5	0	+5	mV/°C
Operating Resistance	V_Z	I_Z = 5mA	–	10	25	Ω
Error Amplifier Input Bias Current	I_{BIAS}		–	–	200	nA
Error Amplifier Minimum Output Voltage	V_{AOL}	R_L = 8.2kΩ	–	0.2	0.5	V
Error Amplifier Maximum Output Voltage	V_{AOH}	R_L = 8.2kΩ	V_Z –1.5	V_Z	–	V
Error Amplifier Reference Input Voltage	V_{Aref}		1.5	2.0	2.5	V
Comparator Reference Voltage 1	$V_{Cref\ 1}$	No signal voltage compared with voltage when signal is input	6.5	7.0	7.5	V
Comparator Reference Voltage 2	$V_{Cref\ 2}$	Signal voltage compared with no signal voltage	4.5	5.0	5.5	V
Channel Detection Output Low–Level Voltage	V_{OL}	I_{OL} = 1mA	–	0.2	0.5	V
Channel Detection Output Leakage Current	I_{OH}	V_{OH} = 13.2V	–	–	5	µA

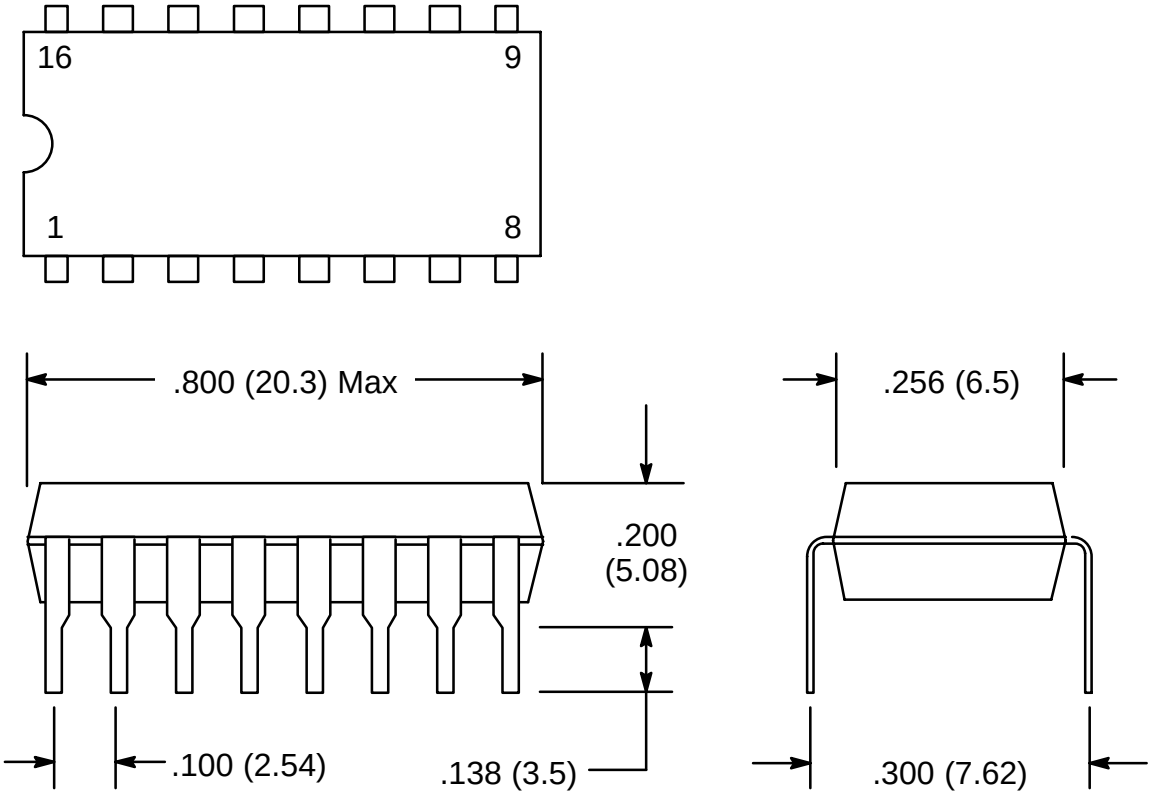
Band Output Format:

BIN_1	BIN_2	$BAND_1$	$BAND_2$	$BAND_3$	$BAND_4$
L	L	H	Z	Z	Z
H	L	Z	H	Z	Z
L	H	Z	Z	H	Z
H	H	Z	Z	Z	H

Z: High Impedance

Pin Connection Diagram




16
9
1
8
.800 (20.3) Max
.200
(5.08)
.100 (2.54)
.138 (3.5)
.256 (6.5)
.300 (7.62)