

NTE1784 Integrated Circuit TV Horizontal Processor

Description:

The NTE1784 is an integrated circuit in a 16-Lead DIP type package designed for use as a horizontal processor circuit for B/W and color television receivers.

Features:

- Noise Gated Horizontal Sync Separator
- Noise Gated Vertical Sync Separator
- Horizontal Oscillator with Frequency Range Limiter
- Phase Comparator between Sync Pulses and Oscillator Pulses (PLL)
- Phase Comparator between Flyback Pulses and Oscillator Pulses (PLL)
- Loop Gain and Time Constant Switching (VCR)
- Composite Blanking and Key Pulse Generator
- Protection Circuits
- Output Stages with High Current Capability

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Supply Voltage (Pin1), V_S	15V
Circuit Voltage, V_2	18V
Circuit Voltage, V_4, V_{11}	V_S
Circuit Voltage, V_8	V_S to -6V
Circuit Voltage, V_9	$+6\text{V}$ to -6V
Peak Circuit Current, I_2	1A
Peak Circuit Current, I_3	500mA
Circuit Current, I_6, I_{10}	30mA
Circuit Current, I_7	20mA
Total Power Dissipation ($T_A \leq +70^\circ\text{C}$), P_{tot}	1W
Operating Junction Temperature Range, T_J	-40° to $+150^\circ\text{C}$
Storage Temperature Range, T_{stg}	-40° to $+150^\circ\text{C}$
Maximum Thermal Resistance, Junction-to-Ambient, R_{thJA}	80°C/W

Electrical Characteristics: ($T_A = +25^\circ\text{C}$, $V_S = 12\text{V}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_S		10.0	12.0	13.2	V
		Output pulses at Pin2 and Pin3 OFF	—	—	4	V
Supply Current	I_S	$I_3 = 0$	—	40	52	mA

Electrical Characteristics (Cont'd): ($T_A = +25^{\circ}\text{C}$, $V_S = 12\text{V}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Horizontal Sync Separator and Noise Gate						
Input Signal (Peak-to-Peak)	V_i		1	3	6	V
Input Switching Voltage	V_8	$I_8 = 80\mu\text{A}$	–	1.5	–	V
Input Switching Current	I_8	$V_8 = 1.4\text{V}$	–	10	–	μA
Input Blocking Current for Noise Suppression	I_8		–	0.9	–	mA
Input Switching Voltage for Noise Suppression	V_8		–	2.1	–	V
Leakage Current	I_8	$V_8 = -5\text{V}$	–	–	1	μA
Vertical Sync Separator						
Input Signal (Peak-to-Peak)	V_i		1	3	6	V
Input Switching Voltage	V_9	$I_9 = 80\mu\text{A}$	–	1.5	–	V
Input Switching Current	I_9	$I_9 = 1.4\text{V}$	–	5	–	μA
Leakage Current	I_9	$V_9 = -5\text{V}$	–	–	1	μA
Vertical Sync Pulse Output Voltage	V_{10}	No load at Pin10	11	–	–	$\text{k}\Omega$
Output Resistance	R_{10}		–	10	–	$\text{k}\Omega$
Delay between Leading Edge of Input and Output Signals	t_{LV}		–	17	–	μs
Delay between Trailing Edge of Input and Output Signals	t_{TV}		–	50	–	μs
Vertical Sync Pulse Duration	t_V		–	190	–	μs
Protection Circuit						
Input Voltage for Switching Off the Output Pulses	V_4	Output pulses OFF	–	–	0.5	V
		Output pulses ON	1	–	–	V
Input Resistance	R_4		–	200	–	$\text{k}\Omega$
Input Current	I_4		5	–	–	μA
Flyback Pulse						
Input Threshold Voltage of Blanking 'Generator'	V_6		–	1.5	–	V
Input Threshold Voltage of Phase Comparator	V_6		–	7.6	–	V
Input Switching Current	I_6	$V_6 \geq 1.7\text{V}$	–	0.23	–	mA
Output Pulse						
Output Voltage (Peak-to-Peak)	V_3	$I_3 = 150\text{mA}_{P-P}$	–	10	–	V
Output Current	I_3	$V_3 = 5\text{V}$	–	500	–	mA
Output Resistance	R_3	At leading edge of output pulse	–	3	–	Ω
		At trailing edge of output pulses	–	20	–	Ω
Output Pulse Duration	t_p		20	22	26	μs
Composite Blanking and Key Pulse						
Key Pulse Output Peak Voltage	V_{7K}		9	11	–	V
Blanking Pulse Output Voltage	V_{7B}		4.2	4.5	4.8	V
Output Resistance	R_7		–	100	–	Ω

Electrical Characteristics (Cont'd): ($T_A = +25^{\circ}\text{C}$, $V_S = 12\text{V}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Composite Blanking and Key Pulse (Cont'd)						
Phase Relation between Trailing Edge of Key Pulse and Middle of Sync Input Pulse	t _{SK}		–	2.7	–	μs
Key Pulse Duration	t _K		3.5	3.8	–	μs
Delay between Flyback Pulse and Blanking Pulse	t _{tb}	V ₆ = 1.7V	–	–	0.2	μs
Internal Gating Pulse						
Gating Pulse Duration	t _q		–	7.5	–	μs
Phase Relation between Middle of Sync Pulse and Trailing and Leading Edge of Gating Pulse	t		–	3.75	–	μs
Coincidence Detector						
Output Voltage	V ₁₁	With coincidence	–	6.8	–	V
		Without coincidence	–	–	4	V
Peak Output Current	I ₁₁		–	0.5	–	mA
VCR Switch						
Input Voltage	V ₁₁		0 to 4 or 8.5 to 12			V
Output Current	–I ₁₁		35	–	–	μA
	I ₁₁		0.4	–	–	mA
Time Constant Switch						
Output Voltage	V ₁₂		–	3	–	V
Output Resistance	R ₁₂	4.5V < V ₁₁ < 8V	–	100	–	Ω
		V ₁₁ > 8.5V or V ₁₁ < 4V	–	40	–	kΩ
Oscillator						
Low Level Threshold Voltage	V ₁₄		–	5.4	–	V
High Level Threshold Voltage	V ₁₄		–	8.2	–	V
Charge Current	I ₁₄		–	0.6	–	mA
Discharge Current	I ₁₄		–	0.3	–	mA
Current Source Supply Voltage	V ₁₅		–	3	–	V
Current Source Supply Current	I ₁₅		–	0.3	–	mA
Free-Running Frequency	f ₀		–	15625	–	Hz
Adjustment Range			–	±10	–	%
Frequency Control Sensitivity			–	52	–	Hz/μA
Frequency Change when V _S Drops to 4V			–	–	±10	%
Oscillator-Flyback Pulse Phase Comparator						
Control Voltage Range	V ₅		9.4 to 8.2			V
Peak Control Current	I ₅		–	–	±0.5	mA
Input Current (Blocked Phase Detector)	I ₅		–	–	5	μA
Permissible Delay between Output Pulse Leading Edge and Flyback Pulse Leading Edge	t _d		–	t _p – t _f	–	μs
Static Control Error			–	–	0.2	%

Electrical Characteristics (Cont'd): ($T_A = +25^\circ\text{C}$, $V_S = 12\text{V}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Sync Pulse–Oscillator Phase Comparator						
Control Voltage Range	V_{13}			4.6 to 1.4		V
Control Peak Range	I_{13}		–	± 2	–	mA
Phase Lock Loop			–	2	–	kHz/ μs
Catching and Holding Range	f		–	± 700	–	Hz
Overall Phase Relationship						
Phase Relation between Middle of Flyback Pulse and Middle of Sync Pulse	t_0		–	2.6	–	μs
Adjustment Sensitivity			–	65	–	mV/ μs
			–	10	–	$\mu\text{A}/\mu\text{s}$

Pin Connection Diagram

