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## NTE1851 Integrated Circuit Audio Amplifier, 24W BTL

**Description:**

The NTE1851 is a monolithic integrated class-B amplifier in a 13-Lead Staggered SIP type package primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6Ω). At a supply voltage  $V_{CC} = 14.4V$ , an output power of 21W can be delivered into a 4Ω BTL (Bridge-Tied Load), or, when used as a stereo amplifier, it delivers 2 x 11W into 2Ω or 2 x 6.5W into 4Ω.

**Features:**

- Flexibility In Use – Mono BTL as well as Stereo
- High Output Power
- Low Offset Voltage at the Output (Important for BTL)
- Large Usable Gain Variation
- Very Good Ripple Rejection
- Internal Limited Bandwidth for High Frequencies
- Low Standby Current Possibility (1μA Typ), to Simplify Required Switches: TTL Drive Possible
- Low Number of Small-Sized External Components
- High Reliability
- Load Dump Protection
- AC and DC Short-Circuit Safe to Ground up to  $V_{CC} = 18V$
- Thermal Protection
- Speaker Protection in Bridge Configuration
- SOAR Protection
- Outputs Short-Circuit Safe to Ground in BTL
- Reverse-Polarity Safe

**Applications:**

- Car Radio Applications
- Drive Low Impedance Loads
- Stereo Amplifier

**Absolute Maximum Ratings:**

Supply Voltage (Pin10), $V_{CC}$	
Operating	18V
Non-Operating	28V
Supply Voltage (During 50ms Load Dump Protection), $V_{CC}$	45V
Peak Output Current, $I_{OM}$	8A
Crystal Temperature, $T_C$	+150°C
Storage Temperature Range, $T_{stg}$	-65° to +150°C
AC and DC Short-Circuit Safe Voltage	18V
Reverse Polarity	10V

**DC Electrical Characteristics:**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range (Pin10)	$V_{CC}$		6	–	18	V
Repetitive Peak Output Current	$I_{ORM}$		–	–	4	A
Total Quiescent Current	$I_{TOT}$		–	75	75	mA
Switching Level 11 OFF	$V_{11}$		–	–	1.8	V
ON			3.0	–	–	V
Impedance Between Pin10 & Pin6; Pin10 & Pin8	$ Z_{OFF} $	Standby Position $V_{11} < 1.8V$	100	–	–	k $\Omega$
Standby Current	$I_{SB}$	$V_{11} = 0$ to 0.8V	–	1	100	$\mu A$
Switch-On Current (Pin11)	$I_{SO}$	$V_{11} \leq V_{10}$	–	10	100	$\mu A$

**AC Electrical Characteristics:** ( $T_A = +25^\circ C$ ,  $V_{CC} = 14.4V$ ,  $f = 1kHz$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
<b>Bridge-Tied Load Application (BTL)</b>							
Output Power with Bootstrap	$P_O$	$R_L = 4\Omega$	$V_{CC} = 14.4V$ , $d_{TOT} = 0.5\%$	15.5	18.0	–	W
			$V_{CC} = 14.4V$ , $d_{TOT} = 10\%$	20	24	–	W
			$V_{CC} = 13.2V$ , $d_{TOT} = 0.5\%$	–	15	–	W
			$V_{CC} = 13.2V$ , $d_{TOT} = 10\%$	–	20	–	W
Open-Loop Voltage Gain	$G_O$		–	75	–	dB	
Closed-Loop Voltage Gain	$G_C$	Note 2	–	40	–	dB	
Output Power without Bootstrap	$P_O$	Note 3	$V_{CC} = 14.4V$ , $d_{TOT} = 0.5\%$	–	12	12	W
			$V_{CC} = 14.4V$ , $d_{TOT} = 10\%$	–	15	15	W
			$V_{CC} = 13.2V$ , $d_{TOT} = 0.5\%$	–	9	9	W
			$V_{CC} = 13.2V$ , $d_{TOT} = 10\%$	–	12	12	W
Frequency Response at –3dB	B	Note 4	20	–	20	Hz	
Input Impedance	$ Z_i $	Note 5	1	–	–	M $\Omega$	
Noise Input Voltage (RMS Value)	$V_{N(RMS)}$	$R_S = 0\Omega$	f = 20Hz to 20kHz	–	0.2	0.2	mV
		$R_S = 10k\Omega$		–	0.35	0.35	mV
	$V_N$	–		0.25	0.8	mV	
Supply Voltage Ripple Rejection	RR	f = 100Hz	42	50	50	dB	
DC Output Offset Voltage Between the Outputs	$ \Delta V_{5-9} $		–	2	50	mV	
Loudspeaker Protection (All Conditions) Maximum DC Voltage (Across the Load)	$ \Delta V_{5-9} $		–	–	1	V	
Power Bandwidth	B	–1dB, $d_{TOT} = 0.5\%$	30	–	40	kHz	

Note 1. The internal circuit impedance at Pin11 is  $> 5k\Omega$  if  $V_{11} > V_{10}$ .

Note 2. Closed-Loop voltage gain can be chosen between 32 and 56dB (BTL), and is determined by external components.

Note 3. Without the bootstrap the 100 $\mu F$  capacitor between Pin5 and Pin6 (Pin8 and Pin9) can be omitted. Pin6, Pin8, and Pin10 have to be interconnected.

Note 4. Frequency response externally fixed.

Note 5. The input impedance in the test circuit is typically 100k $\Omega$ .

**AC Electrical Characteristics (Cont'd):** ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 14.4\text{V}$ ,  $f = 1\text{kHz}$  unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
<b>Stereo Application</b>							
Output Power with Bootstrap	$P_O$	$d_{TOT} = 10\%$ Note 6	$V_{CC} = 14.4\text{V}$ , $R_L = 4\Omega$	6	7	–	W
			$V_{CC} = 14.4\text{V}$ , $R_L = 2\Omega$	10	12	–	W
			$V_{CC} = 13.2\text{V}$ , $R_L = 4\Omega$	–	6	–	W
			$V_{CC} = 13.2\text{V}$ , $R_L = 4\Omega$	–	10	–	W
Output Power with Bootstrap	$P_O$	$d_{TOT} = 0.5\%$ Note 6	$V_{CC} = 14.4\text{V}$ , $R_L = 4\Omega$	–	5.5	–	W
			$V_{CC} = 14.4\text{V}$ , $R_L = 2\Omega$	–	9.0	–	W
			$V_{CC} = 13.2\text{V}$ , $R_L = 4\Omega$	–	4.5	–	W
			$V_{CC} = 13.2\text{V}$ , $R_L = 4\Omega$	–	7.5	–	W
Output Power without Bootstrap	$P_O$	$d_{TOT} = 10\%$ , $V_{CC} = 14.4\text{V}$ , $R_L = 4\Omega$ , Note 3, Note 6, & Note 7		–	6	–	W
Frequency Response at –3dB	B	Note 4		40	–	20	kHz
Supply Voltage Ripple Rejection	RR	Note 8		–	50	–	dB
Channel Separation	$\alpha$	$R_S = 10\text{k}\Omega$ , $f = 1\text{kHz}$		40	50	–	dB
Closed–Loop Voltage Gain	$G_C$	Note 9		–	40	–	dB
Noise Input Voltage (RMS Value)	$V_{N(RMS)}$	$R_S = 0\Omega$	$f = 20\text{Hz to } 20\text{kHz}$	–	0.15	–	mV
		$R_S = 10\text{k}\Omega$		–	0.25	–	mV
	$V_N$	–		0.2	–	mV	

Note 1. The internal circuit impedance at Pin11 is  $> 5\text{k}\Omega$  if  $V_{11} > V_{10}$ .

Note 2. Closed–Loop voltage gain can be chosen between 32 and 56dB (BTL), and is determined by external components.

Note 3. Without the bootstrap the  $100\mu\text{F}$  capacitor between Pin5 and Pin6 (Pin8 and Pin9) can be omitted. Pin6, Pin8, and Pin10 have to be interconnected.

Note 4. Frequency response externally fixed.

Note 5. The input impedance in the test circuit is typically  $100\text{k}\Omega$ .

Note 6. Output power is measured directly at the output pins of the IC.

Note 7. A resistor of  $56\text{k}\Omega$  between Pin3 and Pin7 to reach symmetrical clipping.

Note 8. Supply voltage ripple rejection measured with a source impedance of  $0\Omega$  (Maximum ripple amplitude: 2V).

Note 9. Closed–Loop voltage gain can be chosen between 26 and 50dB (Stereo), and is determined by external components.

**Pin Connection Diagram**  
(Front View)

