

## NTE1853 Integrated Circuit Digital Filter for Compact Disc Digital Audio System

**Features:**

- 16–Bit Serial Data Input (Two’s Complement)
- Interpolated Data Replaces Erroneous Data Samples
- –12dB Attenuation via the Active Low Attenuation Input Control (ATSB)
- Smoothed Transitions Before and After Muting
- Two Identical Finite Impulse Response Transversal Filters each with a Sampling Rate of Four Times that of the Normal Digital Audio Data
- Digital Audio Output of 32–Bit Words Transmitted in Biphasemark Code

**Applications:**

- Compact Disc Digital Audio System
- Digital Filter

**Absolute Maximum Ratings:**

Supply Voltage Range (Pin24),  $V_{DD}$  ..... –0.5V to +7.0V  
 Maximum Input Voltage Range,  $V_I$  ..... –0.5V to  $V_{DD}+0.5V$   
 Electrostatic Handling (Note 2),  $V_{ES}$  ..... –1000V to +1000V  
 Operating Ambient Temperature Range,  $T_A$  ..... –20° to +70°C  
 Storage Temperature Range,  $T_{stg}$  ..... –65° to +150°C

Note 1. All outputs are short–circuit protected except the crystal oscillator output.

Note 2. Equivalent to discharging a 100pF capacitor through a 1.5Ω series resistor with a rise time of 15ns.

**DC and AC Electrical Characteristics:** ( $V_{DD} = 4.5$  to  $5.5V$ ,  $V_{SS} = 0$ ,  $T_A = -20^\circ$  to  $+70^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (Pin24)	$V_{DD}$		4.5	5.0	5.5	V
Supply Current (Pin24)	$I_{DD}$		–	180	–	mA

**DC and AC Electrical Characteristics (Cont'd):** ( $V_{DD} = 4.5$  to  $5.5V$ ,  $V_{SS} = 0$ ,  $T_A = -20^\circ$  to  $+70^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>WSAB, DAAB</b>						
Input Voltage, Low	$V_{IL}$		-0.3	-	+0.8	V
Input Voltage, High	$V_{IH}$		2.0	-	$V_{DD}+0.5$	V
Input Leakage Current	$I_{LI}$		-10	-	+10	$\mu A$
Input Capacitance	$C_I$		-	-	7	pF
<b>EFAB, SDAB (Note 1)</b>						
Input Voltage, Low	$V_{IL}$		-0.3	-	+0.8	V
Input Voltage, High	$V_{IH}$		2.0	-	$V_{DD}+0.5$	V
Input Leakage Current	$I_{LI}$	$V_I = 0V$	-10	-	-	$\mu A$
		$V_I = V_{DD}$	-	-	+50	$\mu A$
Input Capacitance	$C_I$		-	-	7	pF
<b>CLAB, SCAB, ATSB, MUSB (Note 2)</b>						
Input Voltage, Low	$V_{IL}$		-0.3	-	+0.8	V
Input Voltage, High	$V_{IH}$		2.0	-	$V_{DD}+0.5$	V
Input Leakage Current	$I_{LI}$	$V_I = 0V$	-30	-	-	$\mu A$
		$V_I = V_{DD}$	-	-	+10	$\mu A$
Input Capacitance	$C_I$		-	-	7	pF
<b>Output XOUT</b>						
Mutual Conductance at 100kHz	$G_M$		1.5	-	-	mA/V
Small-Signal Voltage Gain	$A_V$	$A_V = G_M \times R_O$	3.5	-	-	V/V
Input Capacitance	$C_I$		-	-	10	pF
Feedback Capacitance	$C_{FB}$		-	-	5	pF
Output Capacitance	$C_O$		-	-	10	pF
Input Leakage Current	$I_{LI}$		-10	0	+10	$\mu A$
<b>Slave Clock Mode</b>						
Input Voltage (Peak to Peak)	$V_{I(P-P)}$	Note 3	3.0	-	$V_{DD}+0.5$	V
Input Voltage, Low	$V_{IL}$	Note 3	0	-	1	V
Input Voltage, High	$V_{IH}$	Note 3	3.0	-	$V_{DD}+0.5$	V
Input Rise Time	$t_R$	Note 4	-	-	20	ns
Input Fall Time	$t_F$	Note 4	-	-	20	ns
Input High Time at 2V (Relative to Clock Period)	$t_{HIGH}$		35	-	65	%

Note 1. Inputs EFAB and SDAB both have internal pull-downs.

Note 2. Inputs CLAB, SCAB,  $\overline{ATSB}$ , and  $\overline{MUSB}$  have internal pull-ups.

Note 3. The minimum peak-to-peak voltage can be reduced to 2V if the output XSYS is not being used. Similarly  $V_{IH}$  can be reduced to 2.4V (Min). All other levels remain the same.

Note 4. Reference levels = 10% and 90%.

**DC and AC Electrical Characteristics (Cont'd):** ( $V_{DD} = 4.5$  to  $5.5V$ ,  $V_{SS} = 0$ ,  $T_A = -20^\circ$  to  $+70^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>DABD, CLBD, WSBD</b>						
Output Voltage, Low	$V_{OL}$	$I_{OL} = 1.6mA$	0	–	0.4	V
Output Voltage, High	$V_{OH}$	$-I_{OH} = 0.2mA$	2.4	–	$V_{DD}$	V
Load Capacitance	$C_L$		–	–	50	pF
<b>XSYS (Note 5)</b>						
Output Voltage, Low	$V_{OL}$		0	–	0.4	V
Output Voltage, High	$V_{OH}$		2.4	–	$V_{DD}$	V
Load Capacitance	$C_L$		–	–	50	pF
<b>DOBM</b>						
Voltage Across a $75\Omega$ Load via Attenuator (Peak-to-Peak)	$V_{L(P-P)}$		0.4	–	0.6	V

Note 5. The output current conditions are dependent on the drive conditions. When a crystal oscillator is being used, the output current capability is  $I_{OL} = +1.6mA$ ;  $I_{OH} = -0.2mA$ . But if a slave input is being used, the output currents are reduced to  $I_{OL} = +0.2mA$ ;  $I_{OH} = -0.2mA$ .

**Timing Characteristics:**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Frequency (XTAL)	$f_{XTAL}$		10.16	11.2896	12.42	MHz
<b>Inputs</b>						
<b>SCAB, CLAB (Note 6)</b>						
SCAB Clock Frequency (Burst Clock)	$f_{SCAB}$		–	2.8224	–	MHz
CLAB Clock Frequency	$f_{CLAB}$	Note 7	–	2.8224	–	MHz
			–	1.4112	–	MHz
Clock Low Time	$t_{CKL}$		110	–	–	ns
Clock High Time	$t_{CKH}$		110	–	–	ns
Input Rise Time	$t_R$		–	–	20	ns
Input Fall Time	$t_F$		–	–	20	ns
<b>DAAB, WSAB, EFAB (Note 8)</b>						
Data Setup Time	$t_{SU}, t_{DAT}$		40	–	–	ns
Data Hold Time	$t_{HD}, t_{DAT}$		0	–	–	ns
Input Rise Time	$t_R$		–	–	20	ns
Input Fall Time	$t_F$		–	–	20	ns

Note 6. Reference levels = 0.8V and 2.0V

Note 7. The signal CLAB can run at either 2.8MHz ( $1/4$  system clock) or 1.4MHz ( $1/8$  system clock) under typical conditions. It does not have a minimum or maximum frequency, but is limited to being  $1/4$  or  $1/8$  of the system clock frequency.

Note 8. Input setup and hold times measured with respect to clock input from A-chip (CLAB). Reference levels = 0.8V and 2.0V.

## Timing Characteristics (Cont'd):

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>SDAB</b> (Note 9)						
Subcode Data Setup Time	$t_{SU}, t_{SDAT}$		40	–	–	ns
Subcode Data Hold Time	$t_{HD}, t_{SDAT}$		0	–	–	ns
Input Rise Time	$t_R$		–	–	20	ns
Input Fall Time	$t_F$		–	–	20	ns
<b>Outputs</b>						
<b>WSBD</b> (Note 6 & Note 10)						
Word Select Setup Time	$t_{SU}, t_{WS}$		40	–	–	ns
Word Select Hold Time	$t_{HD}, t_{WS}$		0	–	–	ns
<b>WSBD</b> (Note 6)						
Output Rise Time	$t_R$		–	–	20	ns
Output Fall Time	$t_F$		–	–	20	ns
<b>DABD</b> (Note 6 & Note 10)						
Data Setup Time	$t_{SU}, t_{DATD}$		40	–	–	ns
Data Hold Time	$t_{HD}, t_{DATD}$		0	–	–	ns
<b>Outputs (Cont'd)</b>						
<b>DABD</b> (Note 6)						
Output Rise Time	$t_R$		–	–	20	ns
Output Fall Time	$t_F$		–	–	20	ns
<b>CLBD</b> (Note 6 & Note 10)						
Clock Period	$t_{CK}$		161	177	197	ns
Clock Low Time	$t_{CKL}$		65	–	–	ns
Clock High Time	$t_{CKH}$		65	–	–	ns
Clock Setup Time	$t_{SU}, t_{CLD}$		40	–	–	ns
Clock Hold Time	$t_{HD}, t_{CLD}$		0	–	–	ns
<b>CLBD</b> (Note 6)						
Output Rise Time	$t_R$		–	–	20	ns
Output Fall Time	$t_F$		–	–	20	ns
<b>DABD</b> (Note 6 & Note 11)						
Data Setup Time	$t_{SU}, t_{DATBD}$		40	–	–	ns
Data Hold Time	$t_{HD}, t_{DATBD}$		60	–	–	ns

Note 6. Reference levels = 0.8V and 2.0V

Note 7. The signal CLAB can run at either 2.8MHz ( $1/4$  system clock) or 1.4MHz ( $1/8$  system clock) under typical conditions. It does not have a minimum or maximum frequency, but is limited to being  $1/4$  or  $1/8$  of the system clock frequency.

Note 8. Input setup and hold times measured with respect to clock input from A–chip (CLAB). Reference levels = 0.8V and 2.0V.

Note 9. Input setup and hold times measured with respect to subcode burst clock input from A–chip (SCAB). Reference levels = 0.8V and 2.0V.

Note 10. Output setup and hold times measured with respect to system clock output (XSYS).

Note 11. Output setup and hold times measured with respect to clock output (CLBD).

**Timing Characteristics (Cont'd):**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>WSBD</b> (Note 6 & Note 11)						
Word Select Setup Time	$t_{SU}$ , $t_{DATWSD}$		40	–	–	ns
Word Select Hold Time	$t_{SU}$ , $t_{DATWSD}$		60	–	–	ns
<b>DOB M</b> (Note 12)						
Output Rise Time	$t_R$		–	–	20	ns
Output Fall Time	$t_F$		–	–	20	ns
Data Bit 0 Pulse Width High	$t_{HIGH(0)}$		–	354	–	ns
Data Bit 0 Pulse Width Low	$t_{LOW(0)}$		–	354	–	ns
Data Bit 1 Pulse Width High	$t_{HIGH(1)}$		–	177	–	ns
Data Bit 1 Pulse Width Low	$t_{LOW(1)}$		–	177	–	ns
<b>XSYS</b>						
Output Rise Time	$t_R$	Note 6	–	–	20	ns
Output Fall Time	$t_F$	Note 6	–	–	20	ns
Output High Time at 2V (Relative to Clock Period)	$t_{HIGH}$		35	–	65	%

Note 6. Reference levels = 0.8V and 2.0V

Note 11. Output setup and hold times measured with respect to clock output (CLBD).

Note 12. Output rise and fall times measured between the 10% and 90% levels; the data bit pulse width measured at the 50% level.

### Pin Connection Diagram

