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NTE7115
Integrated Circuit
Color TV Horizontal Combination Circuit

Description:

The NTE71115 is a monolithic integrated circuit in a 18–Lead DIP type package designed for use in color television receivers.

Features:

- Positive Video Input: Capacitively Coupled (Source Impedance < 200Ω)
- Adaptive Sync Separator: Slicing Level at 50% of Sync Amplitude
- Internal Vertical Pulse Separator ^{W}/Double Slope Integrator
- Output Stage for Vertical Sync Pulse or Composite Sync Depending on the Load; Both are Switched OFF at Muting
- φ_1 Phase Control Between Horizontal Sync and Oscillator
- Coincidence Detector φ_3 for Automatic Time Constant Switching; Overruled by the VCR Switch
- Time Constant Switch Between Two External Time Constants for Loop Gain; Both Controlled by the Coincidence Detector φ_3
- φ_1 Gating Pulse Controlled by Coincidence Detector φ_3
- Mute Circuit Depending on TV Transmitter Identification
- φ_2 Phase Control Between Line Flyback and Oscillator; the Slicing Levels for φ_2 Control and Horizontal Blanking can be set Separately
- Burst Keying and Horizontal Blanking Pulse Generation, in Combination with Clamping of the Vertical Blanking Pulse (Three–Level Sandcastle)
- Horizontal Drive Output with Constant Duty Cycle Inhibited by the Protection Circuit or the Supply Voltage Sensor
- Detector for Too Low Supply Voltage
- Protection Circuit for Switching Off the Horizontal Drive Output Continuously if the Input Voltage is Below 4V or Higher than 8V
- Line Flyback Control Causing the Horizontal Blanking Level at the Sandcastle Output Continuously in Case of a Missing Flyback Pulse
- Spot Suppressor Controlled by the Line Flyback Control

Applications:

- Television Receivers
- Video Receivers

Absolute Maximum Ratings:

Supply Voltage (Pin19), $V_{15-5} = V_{CC}$ 13.2V
Voltages at:
(Pin1, Pin4, and Pin7), V_{1-5}, V_{4-5}, V_{7-5} 18V
(Pin8, Pin13, and Pin18), V_{8-5}, V_{13-5}, V_{18-5} . . . . . V_{CC}
(Pin11 (Range)), V_{11-5} . . . . . –0.5 to +6.0V
Currents at:
Pin1, I_1 . . . . . 10mA
Pin2 (Peak Value), $\pm I_{2M}$ 10mA
Pin4, I_4 . . . . . 100mA
Pin6 (Peak Value), $\pm I_{6M}$ 6mA
Pin7, I_7 . . . . . 10mA
Pin8 (Range), I_8 . . . . . –5 to +1mA
Pin9 (Range), I_9 . . . . . –10 to +3mA
Pin18, $\pm I_{18}$ 10mA
Total Power Dissipation, P_{TOT} 800mW
Operating Ambient Temperature Range, T_A . . . . . –0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

DC and AC Electrical Characteristics: (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Composite Video Input and Sync Separator, Pin11 (Internal Black Level Determination)						
Input Signal (Positive Video; Standard Signal; Peak–to–Peak Value)	$V_{11-5(P-P)}$		0.2	1.0	3.0	V
Sync Pulse Amplitude (Independent of Video Content)	$V_{11-5(P-P)}$		50	–	–	mV
Generator Resistance	R_G		–	–	200	Ω
Input Current During Video	I_{11}		–	5	–	µA
Sync Pulse	$-I_{11}$		–	40	–	µA
Black Level	$-I_{11}$		–	25	–	µA
Composite Sync Generation, Pin10 (Horizontal Slicing Level at 50% of the Sync Pulse Amplitude)						
Capacitor Current During Video	I_{10}		–	16	–	µA
Sync Pulse	$-I_{10}$		–	170	–	µA
Vertical Sync Pulse Generation, Pin9 (Slicing Level at 30% (60% Between Black Level and Horizontal Slicing Level))						
Output Voltage	V_{9-5}		10	–	–	V
Pulse Duration	t_p		–	190	–	µs
Delay With Respect to the Vertical Sync Pulse (LeadinG Edge)	t_D		–	45	–	µs
Pulse–Mode Control Output Current for Vertical Sync Pulse (Dual Integrated)			No Current Applied at Pin9			
Output Current for Horizontal and Vertical Sync Pulse (Non–Integrated Separated Signal)			Current Applied Via a 15kΩ from V_{CC} to Pin9			
Horizontal Oscillator, Pin14 and Pin16						
Free–Running Frequency	f_{OSC}		–	15.625	–	kHz
Reference Voltage for f_{OSC}	V_{14-5}		–	6	–	V

DC and AC Electrical Characteristics (Cont'd): (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Horizontal Oscillator, Pin14 and Pin16 (Cont'd)						
Frequency Control Sensitivity	$\Delta f_{OSC}/\Delta I_{14}$		–	31	–	Hz/µA
Adjustment Range of Circuit	Δf_{OSC}		–	±10	–	%
Spread of Frequency	Δf_{OSC}		–	–	5	%
Frequency Dependency (Excluding Tolerance of External Components) w/Supply Voltage	$\frac{\Delta f_{OSC}/f_{OSC}}{\Delta V_{15-5}/V_{15-5}}$	V_{CC} = 12V	–	±0.05	–	%
w/Supply Voltage Drop of 5V	Δf_{OSC}		–	–	10	%
w/Temperature	TC		–	–	$\pm 10^{-4}$	$°C^{-1}$
Capacitor Current During: Charging	$-I_{16}$		–	1024	–	µA
Discharging	I_{16}		–	313	–	µA
Sawtooth Voltage Timing (Pin14) Rise Time	t_R		–	49	–	µs
Fall Time	t_F		–	15	–	µs
Horizontal Output Pulse, Pin4						
Output Voltage, Low	V_{4-5}	I_4 = 30mA	–	–	0.5	V
Pulse Duration, High	t_P		–	29 ±1.5	–	µs
Supply Voltage for Switching Off the Output Pulse (Pin15)	V_{CC}		–	4	–	V
Hysteresis for Switching On the Output Pulse	ΔV_P		–	250	–	mV
Phase Compensation, φ_1, Pin17						
Control Voltage Range	V_{17-5}		3.55	–	8.3	V
Leakage Current	I_{17}	V_{17-5} = 3.55 to 8.3V	–	–	1	µA
Control Current: for External Time Constant Switch	$\pm I_{17}$		1.8	2.0	2.2	mA
at $V_{18-5} = V_{15-5}$ and $V_{13-5} < 2V$ or $V_{13-5} > 9.5V$			–	8	–	mA
at $V_{18-5} = V_{15-5}$ and V_{13-5} = 2 to 9.5V			1.8	2.0	2.2	mA
Horizontal Oscillator Control Control Sensitivity	S_φ		6	–	–	kHz/µs
Catching and Holding Range	Δf_{OSC}		–	±680	–	Hz
Spread of Catching and Holding Range			–	±10	–	%
Internal Keying Pulse	t_P	V_{13-5} = 2.9 to 9.5V	–	7.5	–	µs
Time Constant Switch Slow Time Constant	V_{13-5}		9.5	–	2.0	V
Fast Time Constant			2.0	–	9.5	V
Impedance Converter Offset Voltage (Slow Time Constant)	$\pm V_{17-18}$		–	–	3	mV
Output Resistance Slow Time Constant	R_{18-5}		–	–	10	Ω
Fast Time Constant			High Impedance	–	–	Ω

DC and AC Electrical Characteristics (Cont'd): (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Phase Compensation, φ_1, Pin17 (Cont'd)						
Leakage Current	I_{18}		–	–	1	µA
Coincidence Detector, φ_3, Pin13						
Output Voltage $^{W}/_{O}$ Coincidence ^{W}/Composite Video Signal	$V_{13–5}$		–	–	1	V
$^{W}/_{O}$ Coincidence $^{W}/_{O}$ Composite Video Signal (Noise)			–	–	2	V
^{W}/Coincidence ^{W}/Composite Video Signal			–	6	–	V
Output Current $^{W}/_{O}$ Coincidence ^{W}/Composite Video Signal	I_{13}		–	50	–	µA
^{W}/Coincidence ^{W}/Composite Video Signal	$–I_{13}$		–	300	–	µA
Switching Current	I_{13}	$V_{13–5} = V_{CC}–0.5V$	–	–	100	µA
	$I_{13(av)}$	$V_{13–5}$ = 0.5V (Average)	–	–	100	µA
Phase Comparison, φ_2, Pin2 and Pin3 (Note 1)						
Phase Relation Between Middle of the Horizontal Sync Pulse and the Middle of the Line Flyback Pulse	Δt	t_{FP} = 12µs, Note 2	–	2.6 ±0.7	–	µs
If Additional Adjustment is Required, it can be Arranged by Applying a Current at Pin3, such that for Applied Current	$\Delta I/\Delta t$		–	30	–	µA/µs
Input for Line Flyback Pulse, Pin2						
Switching Level for φ_2 Comparison	$V_{2–5}$		–	3	–	V
Switching Level for Horizontal Blanking and Flyback Control	$V_{2–5}$		–	0.3	–	V
Input Voltage Limiting	$V_{2–5}$		–	–0.7 +4.5	–	V
Switching Current at Horizontal Flyback	I_2		0.01	1.0	–	mA
at Horizontal Scan			–	–	2.0	µA
Maximum Negative Input Current	$–I_2$		–	–	500	µA
Phase Detector Output, Pin3						
Control Current for φ_2	$\pm I_3$		–	1	–	mA
Control Range	$\Delta t_{\varphi 2}$		–	19	–	µs
Static Control Error	$\Delta t/\Delta t_d$		–	–	0.2	%
Leakage Current	I_3		–	–	5	µA

Note 1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase–modulated (φ_2) horizontal output pulse with constant duration.

Note 2. t_{FP} is the line flyback pulse duration.

DC and AC Electrical Characteristics (Cont'd): (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Burst Gating Pulse, Pin6 (Note 3)						
Output Voltage	$V_{6–5}$		10	11	–	V
Pulse Duration	t_p		3.7	4.0	4.3	µs
Phase Relation Between Middle of Sync Pulse at the Input and the Leading Edge of the Burst Gating Pulse	$t_{\varphi 6}$	$V_{6–5}$ = 7V	2.15	2.65	3.15	µs
Output Trailing Edge Current	I_6		–	2	–	mA
Horizontal Blanking Pulse, Pin6 (Note 3)						
Output Voltage	$V_{6–5}$		4.2	4.5	4.9	V
Output Trailing Edge Current	I_6		–	2	–	mA
Saturation Voltage at Horizontal Scan	$V_{6–5sat}$		–	–	0.5	V
Clamping Circuit for Vertical Blanking Pulse, Pin6 (Note 3)						
Output Voltage	$V_{6–5}$	I_6 = 2.8mA	2.15	2.5	3.0	V
Minimum Output Current	I_{6min}	$V_{6–5}$ > 2.15V	–	2.3	–	mA
Maximum Output Current	I_{6max}	$V_{6–5}$ < 3V	–	3.3	–	mA
TV Transmitter Identification, Pin12						
Output Voltage No TV Transmitter	$V_{12–5}$		–	–	1	V
TV Transmitter Identified			7	–	–	V
Mute Output, Pin7						
Output Voltage, No TV Transmitter	$V_{7–5}$	I_7 = 3mA	–	–	0.5	V
Output Resistance, No TV Transmitter	$R_{7–5}$	I_7 = 3mA	–	–	100	Ω
Output Leakage Current, TV Transmitter Identified	I_7	$V_{12–5}$ > 3V	–	–	5	µA
Protection Circuit, Pin8 (Beam Current/EHT Voltage Protection)						
No–Load Voltage (Operative Condition)	$V_{8–5}$	I_8 = 0	–	6	–	V
Threshold Positive–Going Voltage	$V_{8–5}$		–	8 ±0.8	–	V
Negative–Going Voltage			–	4 ±0.4	–	V
Current Limiting	$\pm I_8$	$V_{8–5}$ = 1 to 8.5V	–	60	–	µA
Input Resistance	$R_{8–5}$	$V_{8–5}$ > 8.5V	–	3	–	kΩ
Response Delay of Threshold Switch	t_d		–	10	–	µs
Control Output of Line Flyback Pulse Condition, Pin1						
Saturation Voltage at Standard Operation	$V_{1–5sat}$	I_1 = 3mA	–	–	0.5	V
Output Leakage Current in Case of Break in Transmission	I_1		–	–	5	µA

Note 3. Three–level sandcastle pulse.

Pin Connection Diagram