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NTE7159
Integrated Circuit
Switch Mode Power Supply Controller

Description:

The NTE7159 is a monolithic integrated circuit in a 16–Lead DIP type package designed for use as the primary part of an off–line switching mode power supply. All functions required for SMPS control under normal operating, transient or abnormal conditions are provided.

The capability of working according to the “master–slave” concept, or according to the “primary regulation” mode makes the NTE7159 very flexible and easy to use. This is particularly true for TV receivers where the IC provides an attractive and low cost solution (no need of stand–by auxiliary power supply).

Features:

- Positive and Negative Current Up To 1.2A and –2A
- Low Start–Up Current
- Direct Drive of the Power Transistor
- Two Levels Transistor Current Limitation
- Double Pulse Suppression
- Soft–Starting
- Under and Overvoltage Lock–Out
- Automatic Stand–By Mode Recognition
- Large Power Range Capability in Stand–By (Burst Mode)
- Internal PWM Signal Generator

Absolute Maximum Ratings:

Power Supply (V_{16}–V_4, V_5, V_{12}, V_{13}), V_{CC} 20V
Output Stage Power Supply (V_{15}–V_4, V_5, V_{12}, V_{13}), V+ 20V
Output Current, I_{OUT}
    Positive (Source Current) 1.5A
    Negative (Sink Current) 2.5A
Operating Junction Temperature, T_J . . . . . +150°C
StorageTemperature Range, T_{stg} . . . . . –40° to +150°C
Thermal Resistance, Junction–to–Case (Note 1), R_{thJC} . . . . . 11°C/W
Thermal Resistance, Junction–to–Ambient (Note 1), R_{thJA} . . . . . 45°C/W

Note 1. Soldered on a 35µm, 40cm^2 board copper area.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	V_{CC}stop	12	V_{CC}max	V
Positive Output Current (Source Current)	$I_{OUT}+$	–	–	1.2	A
Negative Output Current (Sink Current)	$I_{OUT}–$	–	–	2.0	A
Average Positive Output Current	$I_{OUT}+$	–	–	0.6	A
Average Negative Output Current	$I_{OUT}–$	–	–	0.6	A
Operating Frequency	F_{oper}	10	–	100	kHz
Input Pulses Amplitude (Pin2)	V_{IN}	1.5	2.5	4.5	V
Oscillator Resistor Range	R_{OSC}	20	–	150	kΩ
Oscillator Capacitor Range	C_{OSC}	0.47	–	4.7	nF
Soft–Starting Capacitor Range	C1	0.047	1.0	–	µF
Overload Integration Capacitor	C2	0.047	1.0	–	µF
Ratio C2/C1 (C2 must be ≥ C1)	C2/C1	1	–	–	
Operating Ambient Temperature	T_A	–20	–	+70	°C

Electrical Characteristics: (T_A = +25°C, V_{CC} = 12V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Starting Voltage	$V_{CC(start)}$	V_{CC} increasing	9.3	10.3	11.3	V
Stopping Voltage	$V_{CC(stop)}$	V_{CC} decreasing	6.4	7.4	8.4	V
Hysteresis	Hyst V_{CC}	$V_{CC(start)} – V_{CC(stop)}$	2.4	2.9	–	V
Starting Current	$I_{CC(start)}$	V_{CC} = 9V	–	0.7	1.4	mA
Supply Current	I_{CC}	V_{CC} = 12V	–	7.5	15.0	mA
Overvoltage Threshold on V_{CC}	$V_{CC(max)}$		15.0	15.7	–	V
Supply Current After Overvoltage Detection	$I_{CC(over)}$	V_{CC} = 17V	26	35	42	mA
Oscillator/PWM Section						
Accuracy	ΔF/F	R_{OSC} = 68kΩ, C_{OSC} = 1nF	–	10	–	%
Error Amplifier Section						
Open Loop Gain	A_{VO}		–	75	–	dB
Unity Gain Frequency	F_{ug}		–	550	–	kHz
Short Circuit Output Current	I_{SC}	Pin7 Connected to GND	–	2	–	mA
E Input Bias Current	I_{BE}	Pin6	–	0.08	–	µA
Internal Voltgage Reference	V_{REF}	Connected to Error Amplifier Input and Not Directly Accessible	2.34	2.49	2.64	V
Input Section						
IN Input Threshold	V_{IN}	Pin2	0.60	0.85	1.20	V
IS Input Threshold	V_{IS}	Pin1	–	0.15	–	V
IN Input Bias Current	I_{BIN}		–	0.3	–	µA
IS Input Bias Current	I_{BIS}		–	0.4	–	µA

Electrical Characteristics (Cont'd): (T_A = +25°C, V_{CC} = 12V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limitation Section						
First Current Limitation Threshold	V_{IM1}		558	600	642	mV
Second Current Limitation Threshold	V_{IM2}		837	900	963	mV
Thresholds Difference	ΔV_{IM}	$V_{IM2} - V_{IM1}$	–	300	–	mV
Lock–Out Threshold on Pin2	V_{C2}		2.25	2.55	2.85	V
Capacitor C2 Discharge Current	I_{DC2}		–	10	–	µA
Capacitor C2 Charge Current	I_{CC2}		–	45	–	µA
Maximum Input Bias Current	$I_{BI(max)}$	Pin3	–	0.2	–	µA

Pin Connection Diagram