



ELECTRONICS, INC.
 44 FARRAND STREET
 BLOOMFIELD, NJ 07003
 (973) 748-5089
<http://www.nteinc.com>

NTE74148 Integrated Circuit TTL – 8–Line–to–3–Line Octal Priority Encoder

Description:

The NTE74148 is an 8–line–to–3–line octal priority encoder in a 16–Lead plastic DIP type package that features priority decoding of the inputs to ensure that only the highest–order data line is encoded. This device encodes eight data lines to three–line (4–2–1) BINARY (OCTAL). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. Data inputs and output are active at the low logic level. All inputs are buffered.

Applications:

- N–Bit Encoding
- Code Converters and Generators

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC}	7V
DC Input Voltage, V_{IN}	5.5V
Interemitter Voltage (Note 2)	5.5V
Power Dissipation, P_D	190mW
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_{stg}	–65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Note 2. This is the voltage between two emitters of a multiple–emitter transistor. This rating applies between any two of the eight data lines, 0 through 7.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–800	μA
Low–Level Output Current	I_{OL}	–	–	18	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
High Level Input Voltage	V_{IH}		2	–	–	V	
Low Level Input Voltage	V_{IL}		–	–	0.8	V	
Input Clamp Voltage	V_{IK}	$V_{CC} = \text{MIN}, I_I = -12\text{mA}$	–	–	-1.5	V	
High Level Output Voltage	V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = -800\mu\text{A}$	2.4	3.3		V	
Low Level Output Voltage	V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = 16\text{mA}$	–	0.2	0.4	V	
Input Current	I_I	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$	–	–	1	mA	
High Level Input Current 0 Input	I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$	–	–	40	μA	
Any Input Except 0			–	–	80	μA	
Low Level Input Current 0 Input	I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	–	–	-1.6	mA	
Any Input Except 0			–	–	-3.2	mA	
Short-Circuit Output Current	I_{OS}	$V_{CC} = \text{MAX}, \text{Note 5}$	-35	–	-85	mA	
Supply Current	I_{CC}	$V_{CC} = \text{MAX}, \text{Note 5}$	Condition 1	–	40	60	mA
			Condition 2	–	35	55	mA

Note 3. For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 4. All typical values are at $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$.

Note 5. Not more than one output should be shorted at a time.

Note 6. I_{CC} (Condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open, I_{CC} (Condition 2) is measured with all inputs and outputs open.

Switching Characteristics: ($V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Propagation Delay Time (From Input 1 thru 7 to A0, A1, or A2 Output)	t_{PLH}	$R_L = 400\Omega,$ $C_L = 15\text{pF}$	In-Phase Output	–	10	15	ns
	t_{PHL}			–	9	14	ns
Propagation Delay Time (From Input 1 thru 7 to A0, A1, or A2 Output)	t_{PLH}		Out-of-Phase Output	–	13	19	ns
	t_{PHL}			–	12	19	ns
Propagation Delay Time (From Input 0 thru 7 to EO Output)	t_{PLH}		Out-of-Phase Output	–	6	10	ns
	t_{PHL}			–	14	25	ns
Propagation Delay Time (From Input 0 thru 7 to GS Output)	t_{PLH}		In-Phase Output	–	18	30	ns
	t_{PHL}			–	14	25	ns
Propagation Delay Time (From EI Input to A0, A1, or A2 Output)	t_{PLH}		In-Phase Output	–	10	15	ns
	t_{PHL}			–	10	15	ns
Propagation Delay Time (From EI Input to GS Output)	t_{PLH}		In-Phase Output	–	8	12	ns
	t_{PHL}			–	10	15	ns
Propagation Delay Time (From EI Input to EO Output)	t_{PLH}		In-Phase Output	–	10	15	ns
	t_{PHL}			–	17	30	ns

Function Table:

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Pin Connection Diagram

