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NTE74221
Integrated Circuit
TTL – Dual Monostable Multivibrator

Description:

The NTE74221 is a monolithic dual multivibrator in a 16–Lead plastic DIP type package with performance characteristics virtually identical to those of the NTE74121. Each multivibrator features a negative–transition–triggered input and a positive–transition–triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt–trigger input circuitry (TTL hysteresis) for B input allows jitter–free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal latching circuitry.

Once fired, the outputs are independent o further transitions of the A an B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35ns to the maximum pulse length of 70 seconds by choosing appropriate timing components. With $R_{ext} = 2k\Omega$ and $C_{ext} = 0$, and output pulse of typically 30ns is achieved which may be used as a DC triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter–free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ).Throughout these ranges, pulse width is defined by the relationship: $t_w(out) = C_{ext}R_{ext}\,ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where the pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used. Also, the range of jitter–free output pulse widths is extended if V_{CC} is held to 5V and free–air temperature is +25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse–width jitter is allowed.

Features:

- Overriding Clear Terminates Output Pulse

Recommended Operating Conditions:

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.0	5.25	V
High−Level Output Current		I_{OH}	–	–	−800	μA
Low−Level Output Current		I_{OL}	–	–	16	mA
Rate of Rise or Fall of Input Pulse	Schmitt, B	dv/dt	1	–	–	V/s
	Logic Input, A		1	–	–	V/μs
Input Pulse Width	A or B	$t_{w(in)}$	50	–	–	ns
	Clear	$t_{w(clear)}$	20	–	–	ns
Clear Inactive−State Setup Time		t_{su}	15	–	–	ns
External Timing Resistance		R_{ext}	1.4	–	40	kΩ
External Timing Capacitance		C_{ext}	0	–	1000	μF
Output Duty Cycle	R_T = 2kΩ		–	–	67	%
	R_T = MAX R_{ext}		–	–	90	%
Operating Temperature Range		T_A	0	–	+70	°C

Electrical Characteristics: (Note 1, Note 2)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Threshold Voltage at A Input	V_{T+}	V_{CC} = MIN		–	1.4	2.0	V
	$V_{T−}$			0.8	1.4	–	V
Threshold Voltage at B Input	V_{T+}	V_{CC} = MIN		–	1.55	2.0	V
	$V_{T−}$			0.8	1.35	–	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, I_{OH} = −800μA		2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, I_{OL} = 16mA		–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V		–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	Input A	–	–	40	μA
			Input B, Clear	–	–	80	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	Input A	–	–	−1.6	mA
			Input B, Clear	–	–	−3.2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 3		−18	–	−55	mA
Supply Current	I_{CC}	V_{CC} = MAX	Quiescent	–	26	50	mA
			Triggered	–	46	80	mA

Note 1. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 2. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 3. Not more than one output should be shorted at a time.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay Time (From A Input to Q Output)	t_{PLH}	C_L = 15pF, R_L = 400Ω	C_{ext} = 80pF, R_{ext} = 2kΩ	–	45	70	ns
Propagation Delay Time (From B Input to Q Output)	t_{PLH}			–	35	55	ns
Propagation Delay Time (From A Input to $\overline{Q}$ Output)	t_{PHL}			–	50	80	ns
Propagation Delay Time (From B Input to $\overline{Q}$ Output)	t_{PHL}			–	40	65	ns
Propagation Delay Time (From Clear Input to Q Output)	t_{PHL}			–	–	27	ns
Propagation Delay Time (From Clear Input to $\overline{Q}$ Output)	t_{PHL}			–	–	40	ns
Output Pulse Width (From A or B Input to Q or $\overline{Q}$ Output)	$t_{w(out)}$		C_{ext} = 80pF, R_{ext} = 2kΩ	70	110	150	ns
			C_{ext} = 0pF, R_{ext} = 2kΩ	20	30	50	ns
			C_{ext} = 100pF, R_{ext} = 10kΩ	650	700	750	ns
			C_{ext} = 1μF, R_{ext} = 10kΩ	6.5	7.0	7.5	ns

Function Table:

Truth Table:

Inputs			Outputs	
Clear	**A**	**B**	**Q**	**$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎴
H	↓	H	⎍	⎴
↑ *	L	H	⎍	⎴

H = High Level

L = Low Level

X = Irrelavent

↑ = Transition from LOW–to–HIGH

↓ = Transition from HIGH–to–LOW

⎍ = One HIGH Level Pulse

⎴ = One LOW Level Pulse

***** This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logical “1” state prior to CLR going high. This latch is conditioned by taking either A or B low which $\overline{CLR}$ is in the inactive state.

Pin Connection Diagram