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NTE7474
Integrated Circuit
TTL, Dual D–Type Positive–Edge–Triggered Flip–Flop w/Preset and Clear

Description:

The NTE7474 contains two independent D–type positive–edge–triggered flip–flops in a 14–Lead DIP type package characterized for operating from 0° to +70°C. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive–going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

Absolute Maximum Ratings: (T_A = 0° to +70°C unless otherwise specified)

Supply Voltage (Note 1), V_{CC} 7V
Input Voltage, V_{IN} 5.5V
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Voltage values are with respect to network GND terminal.

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}		2	–	–	V
Low–Level Input Voltage	V_{IL}		–	–	0.8	V
High–Level Output Current	I_{OH}		–	–	–0.4	mA
Low–Level Output Current	I_{OL}		–	–	16	mA
Pulse Duration CLK High	t_w		30	–	–	ns
CLK Low			37	–	–	ns
$\overline{PRE}$ or $\overline{CLR}$ Low			30	–	–	ns
Input Setup Time Before CLK ↑	t_{su}		20	–	–	ns
Input Hold Time–Data After CLK ↑	t_h		5	–	–	ns
Operating Ambient Temperature	T_A		0	–	70	°C

Electrical Characteristics: (T_A = 0° to +70°C, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{I1} = −12mA	–	–	−1.5	V
Output High Voltage	V_{OH}	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 800mV, I_{OH} = −0.4mA	2.4	3.4	–	V
Output Low Voltage	V_{OL}	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 800mV, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = Max, V_I = 5.5V	–	–	1	mA
Input High Current	I_{IH}	V_{CC} = Max, V_I = 2.4V				
D			–	–	40	mA
$\overline{CLR}$			–	–	120	mA
All Others			–	–	80	mA
Input Low Current	I_{IL}	V_{CC} = Max, V_I = 0.4V				
D			–	–	−1.6	mA
$\overline{PRE}$ (Note 3)			–	–	−1.6	mA
$\overline{CLR}$ (Note 3)			–	–	−3.2	mA
CLK			–	–	−3.2	mA
Output Short Circuit Current	I_{OS}	V_{CC} = Max, Note 4	−18	–	−57	mA
Power Supply Current	I_{CC}	V_{CC} = Max, Note 5	–	8.5	15	mA

Note 2. All typical values are at V_{CC} = 5V, T_A = +25°C. For conditions shown as Min and Max, use the appropriate value specified under recommended operating conditions.

Note 3. Clear is tested with preset high and preset is tested with clear high.

Note 4. Not more than one output should be shorted at a time.

Note 5. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}			R_L = 400Ω, C_L = 15pF	15	25	–	MHz
Propagation Delay Time		$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$					
Low−to−High	t_{PLH}				–	–	25	ns
High−to−Low	t_{PHL}				–	–	40	ns
Propagation Delay Time		$\overline{CLK}$	Q or $\overline{Q}$					
Low−to−High	t_{PLH}				–	14	25	ns
High−to−Low	t_{PHL}				–	20	40	ns

Function Table:

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 6)	H (Note 6)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Note 6. The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not presist when either preset or clear returns to its inactive (high) level.

Pin Connection Diagram