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NTE7476
Integrated Circuit
TTL – Dual J–K Flip–Flop with Preset and Clear

Description:

The NTE7476 is a dual J–K flip–flop in a 16–Lead plastic DIP type package that contains two independent J–K positive–edge–triggered flip–flops with individual J–K clock, preset, and clear inputs. J–K input is loaded into the master while the clock is high and transferred to the slave on the high–to–low transition. J and K inputs must be stable while the clock is high.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–0.4	mA
Low–Level Output Current	I_{OL}	–	–	16	mA
Pulse Duration CLK High	t_w	20	–	–	ns
CLK Low		47	–	–	ns
$\overline{PRE}$ or $\overline{CLR}$ Low		25	–	–	ns
Setup Time Before CLK ↑	t_{su}	0	–	–	ns
Input Hold Time Data After CLK ↓	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −0.4mA	2.4	3.4		V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current J or K	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
All Other			–	–	80	μA
Low Level Input Current J or K	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
All Other (Note 4)			–	–	−3.2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6	–	10	20	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Clear is tested with preset high and preset is tested with clear high.

Note 5. Not more than one output should be shorted at a time.

Note 6. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 400Ω, C_L = 15pF	15	20	–	MHz
Propagation Delay Time (From $\overline{PRE}$ or $\overline{CLR}$ input to Any Q Output)	t_{PLH}		–	16	25	ns
	t_{PHL}		–	25	40	ns
Propagation Delay Time (From CLK input to Any Q Output)	t_{PLH}		–	16	25	ns
	t_{PHL}		–	25	40	ns

Function Tables:

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H †	H †
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

† This configuration is nonstable; that is, it will not persist when wither preset or clear returns to its inactive (high) level.

Pin Connection Diagram