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NTE74C922 & NTE74C923
Integrated Circuit
TTL– CMOS Key Encoders

Description:

The NTE74C922 (16–Key, 18–Lead DIP) and NTE74C923 (20–Key, 20–Lead DIP) CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on–chip pull–up devices which permit switches with up to 50kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two–key roll–over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3–STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features:

- 50kΩ Maximum Switch On Resistance
- On or Off Chip Clock
- On–Chip Row Pull–Up Devices
- 2 Key Roll–Over
- Keybounce Elimination with Single Capacitor
- Last Key Register at Outputs
- 3–STATE Output LPTTL Compatible
- Wide Supply range: 3V to 15V
- Low Power Consumption

Absolute Maximum Ratings: (Note 1)

Operating V_{CC} Range . . . . . 3V to 15V
V_{CC} 18V
Voltage at Any Pin . . . . . V_{CC}–0.3V to V_{CC}+0.3V
Power Dissipation, P_D 700mW
Operating Temperature Range . . . . . –40° to +85°C
Storage Temperature Range . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10 seconds) . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which the safety of he device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = −40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Positive−Going Threshold Voltage at OSC and KBM Inputs	V_{T+}	V_{CC} = 5V, $I_{IN} \geq$ 0.7mA		3.0	3.6	4.3	V
		V_{CC} = 10V, $I_{IN} \geq$ 1.4mA		6.0	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1mA		9.0	10.0	12.9	V
Negative−Going Threshold Voltage at OSC and KBM Inputs	V_{T-}	V_{CC} = 5V, $I_{IN} \geq$ 0.7mA		0.7	1.4	2.0	V
		V_{CC} = 10V, $I_{IN} \geq$ 1.4mA		1.4	3.2	4.0	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1mA		2.1	5.0	6.0	V
Logical “1” Input Voltage except OSC and KBM Inputs	$V_{IN(1)}$	V_{CC} = 5V		3.5	4.5	–	V
		V_{CC} = 10V		8.0	9.0	–	V
		V_{CC} = 15V		12.5	13.5	–	V
Logical “0” Input Voltage except OSC and KBM Inputs	$V_{IN(0)}$	V_{CC} = 5V		–	0.5	1.5	V
		V_{CC} = 10V		–	1.0	2.0	V
		V_{CC} = 15V		–	1.5	2.5	V
Row Pull−Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	I_{rp}	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		–	–2	–5	μA
		V_{CC} = 10V		–	–10	–20	μA
		V_{CC} = 15V		–	–22	–45	μA
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V, I_O = −10μA		4.5	–	–	V
		V_{CC} = 10V, I_O = −10μA		9.0	–	–	V
		V_{CC} = 15V, I_O = −10μA		13.5	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V, I_O = 10μA		–	–	0.5	V
		V_{CC} = 10V, I_O = 10μA		–	–	1.0	V
		V_{CC} = 15V, I_O = 10μA		–	–	1.5	V
Column “ON” Resistance at X1, X2, X3 and X54 Outputs	R_{on}	V_{CC} = 5V, V_O = 0.5V		–	500	1400	Ω
		V_{CC} = 10V, V_O = 1V		–	300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		–	200	500	Ω
Supply Current OSC at 0V, (one Y low)	I_{CC}	V_{CC} = 5V		–	0.55	1.1	mA
		V_{CC} = 10V		–	1.1	1.9	mA
		V_{CC} = 15V		–	1.7	2.6	mA
Logical “1” Input Current at Output Enable	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		–	0.005	1.0	μA
Logical “0” Input Current at Output Enable	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V		–1.0	–0.005	–	μA
CMOS/LPTTL Interface							
Except OSC and KBM Inputs	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Except OSC and KBM Inputs	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360μA,		2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360μA,		–	–	0.4	V
Output Drive (Short Circuit Current)							
Output Source Current (P−Channel)	I_{SOURCE}	V_{OUT} = 0V, T_A = +25C°C	V_{CC} = 5V	–1.75	–3.3	–	mA
			V_{CC} =10V	–8	–15	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{OUT} = V_{CC}, T_A = +25C°C	V_{CC} = 5V	1.75	3.6	–	mA
			V_{CC} =10V	8	16	–	mA

AC Electrical Characteristics: (T_A = +25°C, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay Time to Logical “0” or Logical “1” from D.A.	t_{pd0}, t_{pd1}	C_L = 50pF	V_{CC} = 5V	–	60	150	ns
			V_{CC} = 10V	–	35	80	ns
			V_{CC} = 15V	–	25	60	ns
Propagation Delay Time from Logical “0” or Logical “1” into High Impedance State	T_{0H}, t_{1H}	R_L = 10k, C_L = 10pF	V_{CC} = 5V	–	80	200	ns
			V_{CC} = 10V	–	65	150	ns
			V_{CC} = 15V	–	50	110	ns
Propagation Delay Time from High Impedance State into Logical “0” or Logical “1”	T_{0H}, t_{1H}	R_L = 10k, C_L = 50pF	V_{CC} = 5V	–	100	250	ns
			V_{CC} = 10V	–	55	125	ns
			V_{CC} = 15V	–	40	90	ns
Input Capacitance	C_{IN}	Any Input, Note 3		–	5.0	7.5	pF
3−STATE Output Capacitance	C_{OUT}	Any Output, Note 3		–	10	–	pF

Note 2. AC Parameters are guaranteed by DC correlated testing.
Note 3. Capacitance is guaranteed by periodic testing.

Truth Table:

Pin0 through Pin11

Data Out	Switch Position											
	0 Y1, X1	1 Y1, X2	2 Y1, X3	3 Y1, X4	4 Y2, X1	5 Y2, X2	6 Y2, X3	7 Y2, X4	8 Y3, X1	9 Y3, X2	10 Y3, X3	11 Y3, X4
A	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1	0	0	0	0
D	0	0	0	0	0	0	0	0	1	1	1	1
E (Note 4)	0	0	0	0	0	0	0	0	0	0	0	0

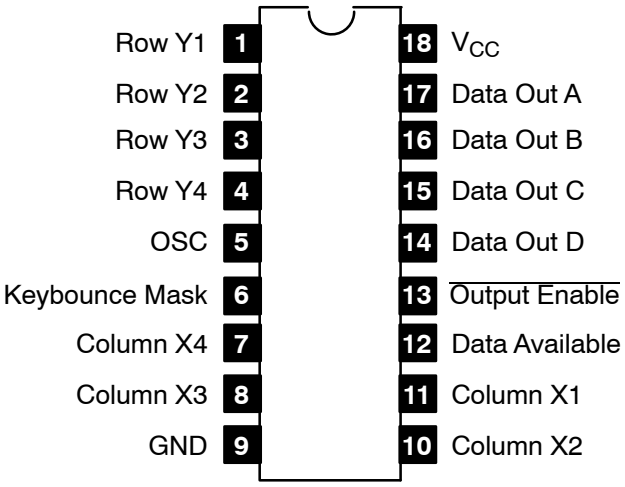
Pin12 through Pin19

Data Out	Switch Position							
	12 Y4, X1	13 Y4, X2	14 Y4, X3	15 Y4, X4	16 Y5 (Note 4), X1	17 Y5 (Note 4), X2	18 Y5 (Note 4), X3	19 Y5 (Note 4), X4
A	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1
C	1	1	1	1	0	0	0	0
D	1	1	1	1	0	0	0	0
E (Note 4)	0	0	0	0	1	1	1	1

Note 4. Omit for NTE74C922.

Pin Connection Diagram

NTE74C922



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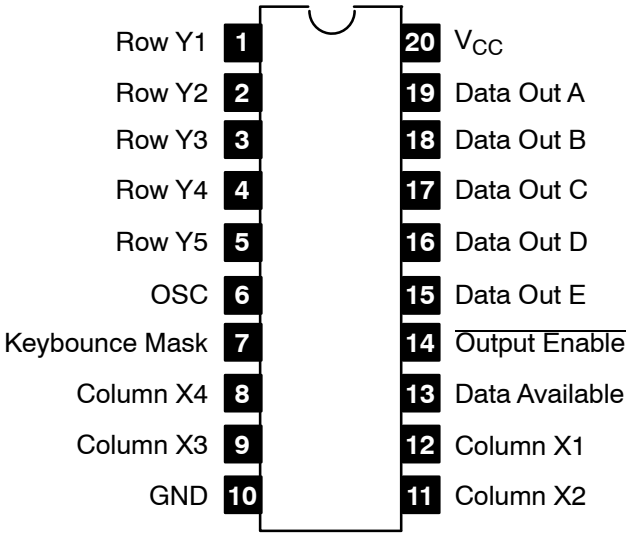

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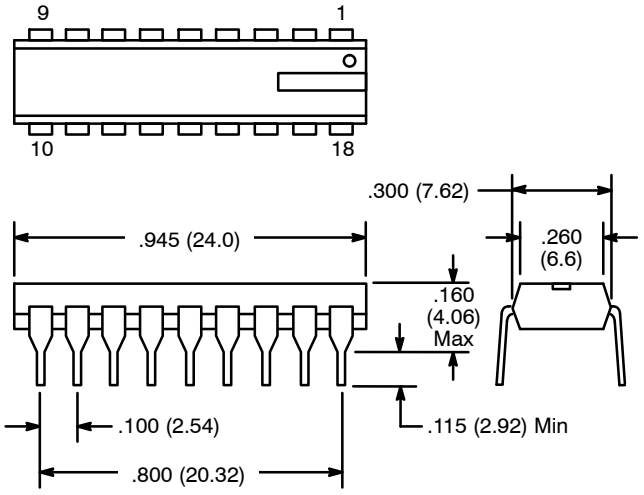

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