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NTE74LS76A Integrated Circuit TTL – Dual J–K Flip–Flop with Preset and Clear

Description:

The NTE74LS76A is a dual J–K flip–flop in a 16–Lead plastic DIP type package that contains two independent negative–edge–triggered flip–flops. The J and K inputs must be stable one set–up time prior to the high–to–low clock transitions for predictable operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_{stg}	–65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–0.4	mA
Low–Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	30	MHz
Pulse Duration CLK High	t_w	20	–	–	ns
\overline{PRE} or \overline{CLR} Low		25	–	–	ns
Setup Time Before CLK ↓ Data High or Low	t_{su}	20	–	–	ns
\overline{CLR} Inactive		20	–	–	ns
\overline{PRE} Inactive		25	–	–	ns
Hold Time Data After CLK ↓	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input Clamp Voltage	V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$	-	-	-1.5	V	
High Level Output Voltage	V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}, I_{OH} = -0.4\text{mA}$	2.7	3.4		V	
Low Level Output Voltage	V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}$	$I_{OL} = 4\text{mA}$	-	0.25	0.4	V
			$I_{OL} = 8\text{mA}$	-	0.35	0.5	V
Input Current J or K $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ CLK	I_I	$V_{CC} = \text{MAX}, V_I = 7\text{V}$	-	-	0.1	mA	
			-	-	0.3	mA	
			-	-	0.4	mA	
High Level Input Current J or K $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ CLK	I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$	-	-	20	μA	
			-	-	60	μA	
			-	-	80	μA	
Low Level Input Current J or K All Other	I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	-	-	-0.4	mA	
			-	-	-0.8	mA	
Short-Circuit Output Current	I_{OS}	$V_{CC} = \text{MAX}, \text{Note 4, Note 5}$	-20	-	-100	mA	
Supply Current	I_{CC}	$V_{CC} = \text{MAX}, \text{Note 6}$	-	4	6	mA	

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$.

Note 4. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Note 5. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.125\text{V}$ and the minimum and maximum limits reduced to one half of their stated values.

Note 6. With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics: ($V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	$R_L = 2\text{k}\Omega, C_L = 15\text{pF}$	20	45	-	MHz
Propagation Delay Time (From $\overline{\text{PRE}}, \overline{\text{CLR}}$ or CLK input to Any Q Output)	t_{PLH}		-	15	20	ns
	t_{PHL}		-	15	20	ns

Function Tables:

Inputs					Outputs	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H †	H †
H	H	↓	L	L	Q_0	\overline{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	\overline{Q}_0

† This configuration is nonstable; that is, it will not persist when wither preset or clear returns to its inactive (high) level.

Pin Connection Diagram

