NTGD3149C

Power MOSFET
Complementary, 20 V, +3.5/−2.7 A, TSOP−6 Dual

Features
- Complementary N−Channel and P−Channel MOSFET
- Small Size (3 x 3 mm) Dual TSOP−6 Package
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb−Free Device

Applications
- DC−DC Conversion Circuits
- Load/Power Switching with Level Shift

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage (N−Ch & P−Ch)			V_{GS}	±8	V
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C T_A = 85°C	I_D	3.2 2.3	A
	t ≤ 5 s	T_A = 25°C		3.5	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C T_A = 85°C	I_D	2.4 1.7	A
	t ≤ 5 s	T_A = 25°C		2.7	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.9	W
	t ≤ 5 s			1.1	
Pulsed Drain Current	N−Ch	t_p = 10 μs	I_{DM}	11	A
	P−Ch			8.0	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	0.8	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	140	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 1)	$R_{\theta JA}$	110	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

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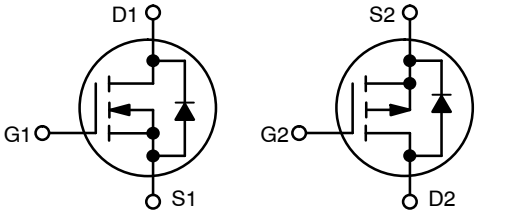
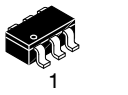
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX (Note 1)
N−Ch 20 V	60 mΩ @ 4.5 V	3.5 A
	90 mΩ @ 2.5 V	
P−Ch −20 V	110 mΩ @ 4.5 V	−2.7 A
	145 mΩ @ 2.5 V	

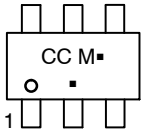


N−CHANNEL MOSFET **P−CHANNEL MOSFET**



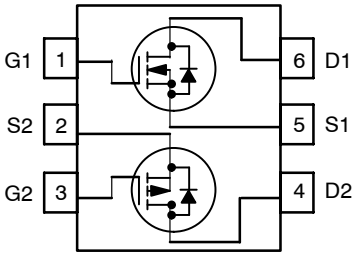
TSOP−6
CASE 318G
STYLE 13

MARKING DIAGRAM



CC = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = −250 μA	−20			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N				1.1		mV/°C
		P				1.1		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25 °C			1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −16 V				−1.0	
		N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 85 °C			10	
		P	V_{GS} = 0 V, V_{DS} = −16 V				−10	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±8 V				±100	nA
		P	V_{DS} = 0 V, V_{GS} = ±8 V				±100	
ON CHARACTERISTICS (Note 2)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.4		1.0	V
		P		I_D = −250 μA	−0.4		−1.0	
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V , I_D = 3.5 A			41	60	mΩ
		P	V_{GS} = −4.5 V , I_D = −2.7 A			83	110	
		N	V_{GS} = 2.5 V , I_D = 2.9 A			51	90	
		P	V_{GS} = −2.5 V , I_D = −2.4 A			104	145	
		N	V_{GS} = 1.8 V , I_D = 2.2 A			67	150	
		P	V_{GS} = −1.8 V , I_D = −1.9 A			143	220	
Forward Transconductance	g_{FS}	N	V_{DS} = 10 V , I_D = 3.5 A			4.7		S
		P	V_{DS} = −10 V , I_D = −2.7 A			5.1		
CHARGES AND CAPACITANCES								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V	V_{DS} = 10 V		387		pF
Output Capacitance	C_{OSS}					73		
Reverse Transfer Capacitance	C_{RSS}					43		
Input Capacitance	C_{ISS}	P		V_{DS} = −10 V		509		
Output Capacitance	C_{OSS}					76		
Reverse Transfer Capacitance	C_{RSS}					40		
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 2.0 A R_G = 6 Ω			4.6	5.5	nC
Threshold Gate Charge	$Q_{G(TH)}$					0.3		
Gate−to−Source Gate Charge	Q_{GS}					0.7		
Gate−to−Drain “Miller” Charge	Q_{GD}					1.2		
Total Gate Charge	$Q_{G(TOT)}$	P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −1.0 A R_G = 6 Ω			5.2	5.5	
Threshold Gate Charge	$Q_{G(TH)}$					0.4		
Gate−to−Source Gate Charge	Q_{GS}					1.0		
Gate−to−Drain “Miller” Charge	Q_{GD}					1.2		

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 3)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 1.0 A, R_G = 6.0 Ω			6.5		ns
Rise Time	t_r					3.8		
Turn−Off Delay Time	$t_{d(OFF)}$					16.4		
Fall Time	t_f					2.4		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −1.0 A, R_G = 6.0 Ω			7.0		
Rise Time	t_r					5.3		
Turn−Off Delay Time	$t_{d(OFF)}$					33.3		
Fall Time	t_f					29.5		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25 °C	I_S = 0.8 A		0.7	1.2	V
		P		I_S = −0.8 A		−0.7	−1.2	
Reverse Recovery Time	t_{RR}	N	V_{GS} = 0 V, dI_S / dt = 100 A/μs			7.7		ns
Charge Time	t_a					4.5		
Discharge Time	t_b					3.2		
Reverse Recovery Charge	Q_{RR}					1.9		nC
Reverse Recovery Time	t_{RR}	P	V_{GS} = 0 V, dI_S / dt = 100 A/μs			11.4		ns
Charge Time	t_a					7.5		
Discharge Time	t_b					3.9		
Reverse Recovery Charge	Q_{RR}					4.7		nC

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTGD3149CT1G	TSOP6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS (N−CHANNEL)

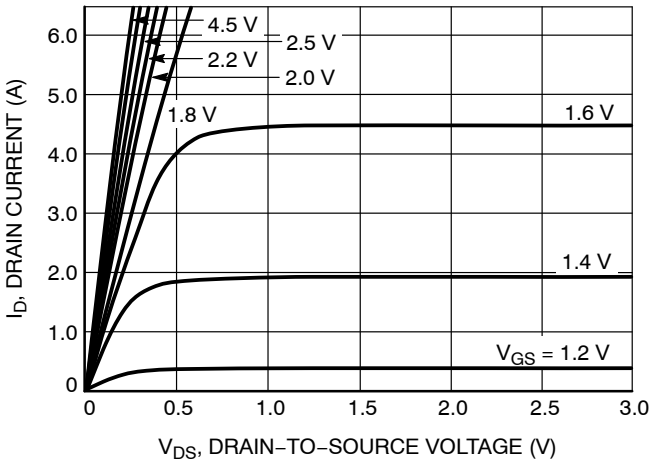


Figure 1. Nch On−Region Characteristics

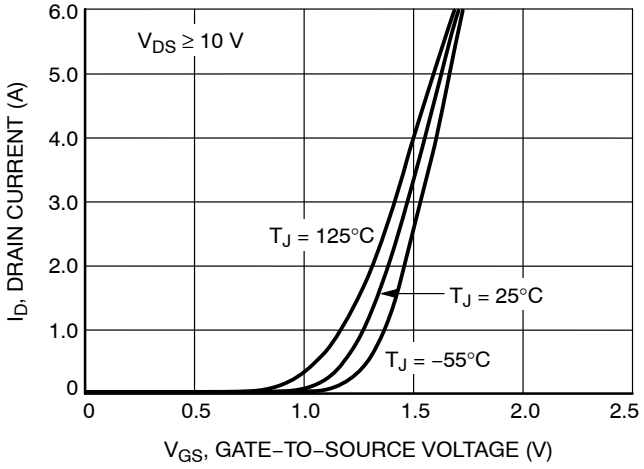


Figure 2. Nch Transfer Characteristics

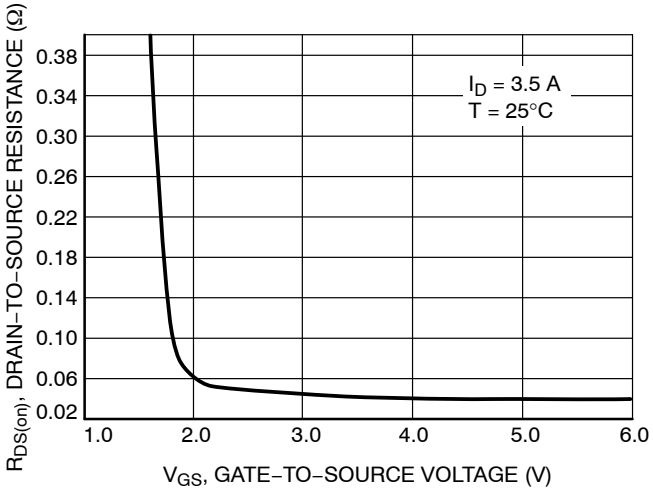


Figure 3. Nch On−Resistance vs. Gate Voltage

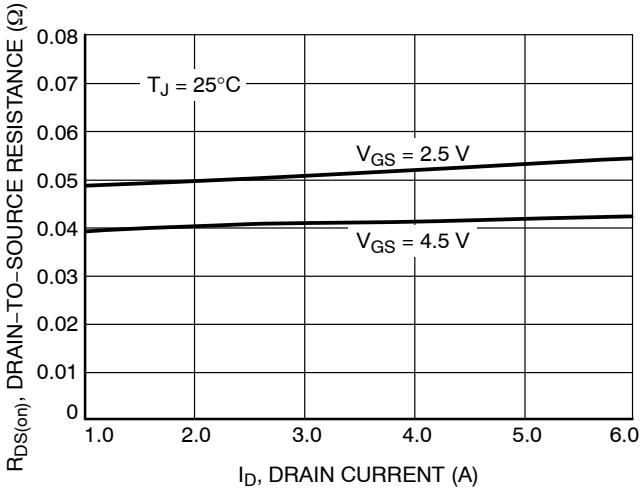


Figure 4. Nch On−Resistance vs. Drain Current and Gate Voltage

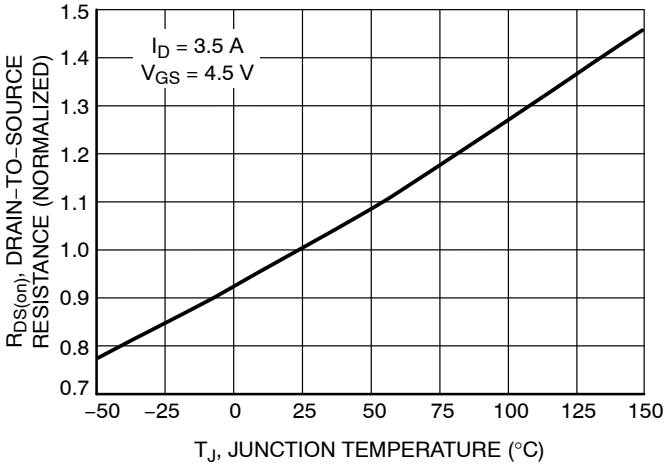


Figure 5. Nch On−Resistance Variation with Temperature

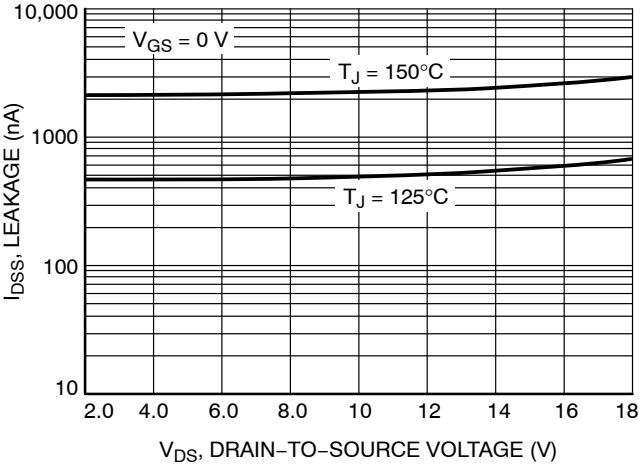


Figure 6. Nch Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (N−CHANNEL)

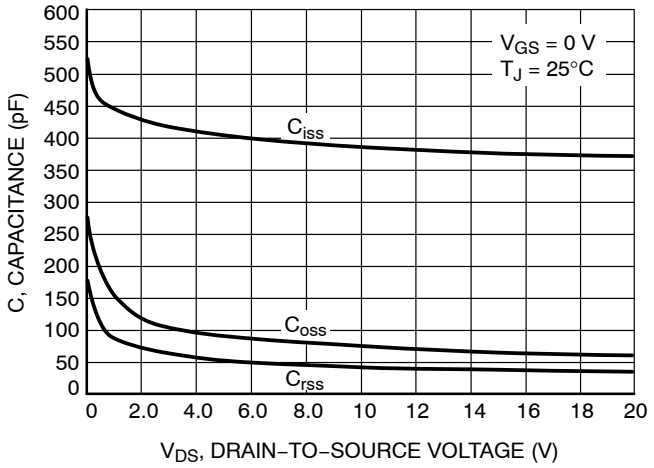


Figure 7. Nch Capacitance Variation

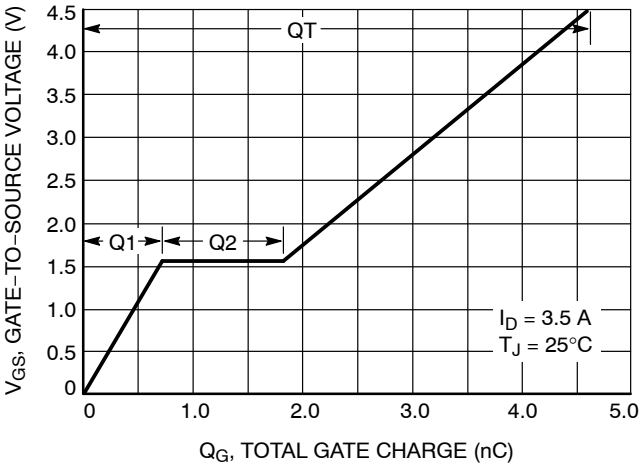


Figure 8. Nch Gate−to−Source Voltage vs. Total Charge

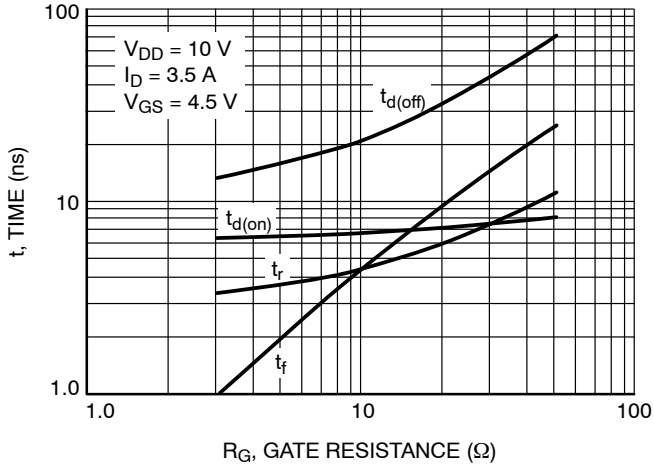


Figure 9. Nch Resistive Switching Time Variation vs. Gate Resistance

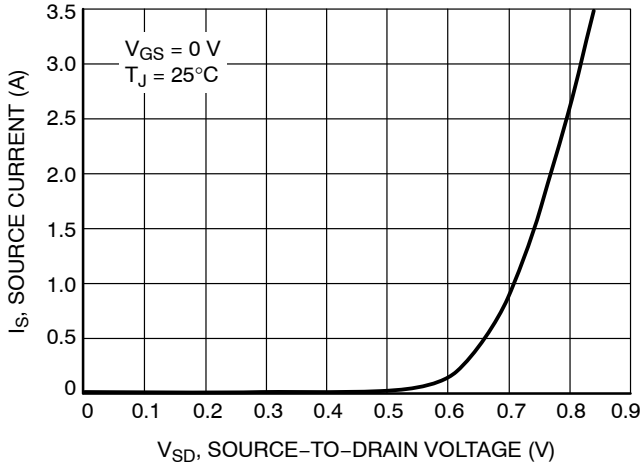


Figure 10. Nch Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (P−CHANNEL)

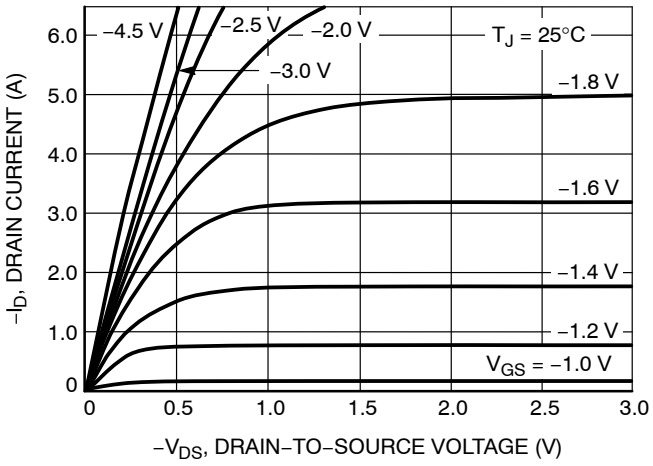


Figure 11. Pch On−Region Characteristics

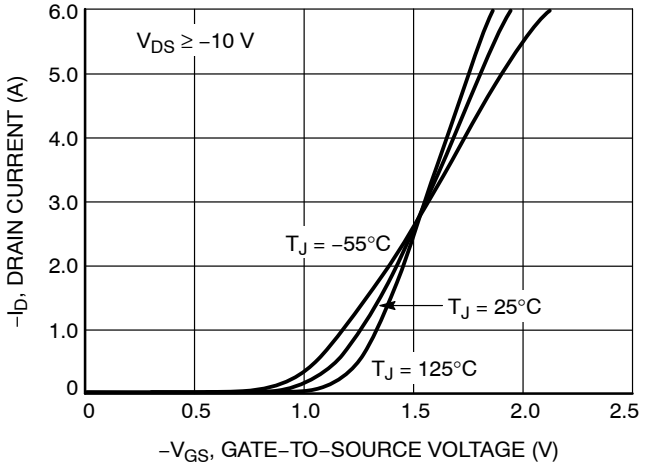


Figure 12. Pch Transfer Characteristics

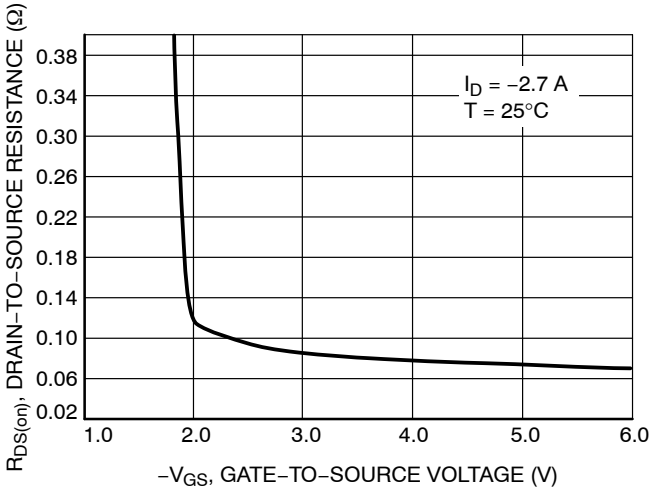


Figure 13. Pch On−Resistance vs. Gate Voltage

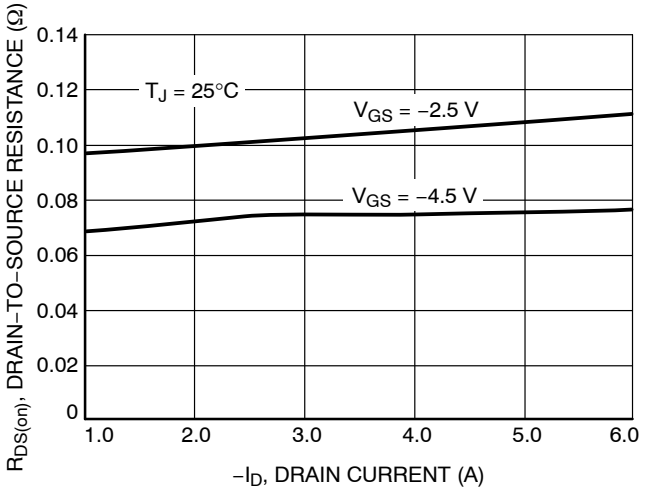


Figure 14. Pch On−Resistance vs. Drain Current and Gate Voltage

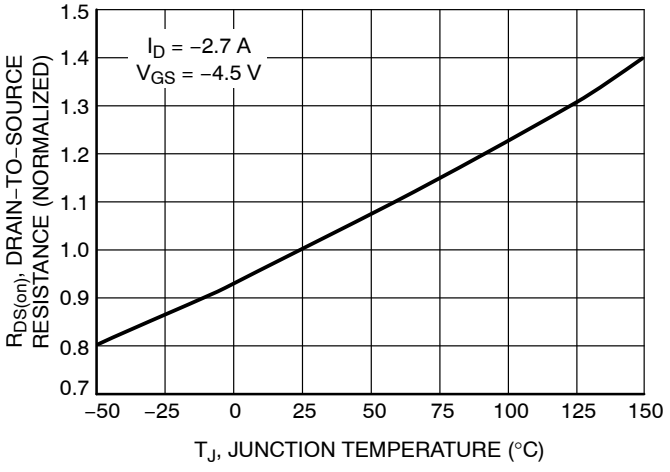


Figure 15. Pch On−Resistance Variation with Temperature

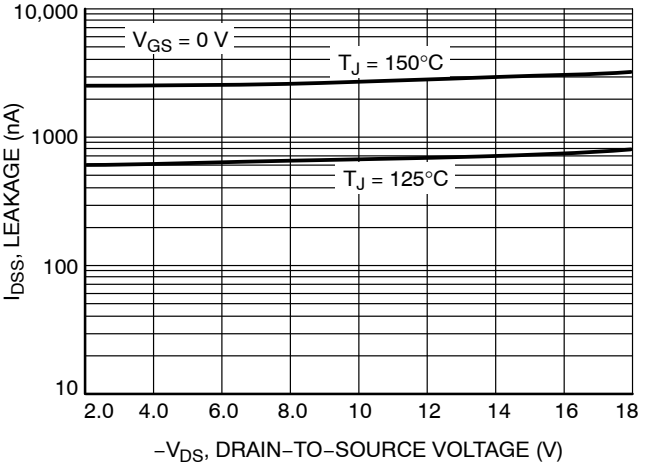


Figure 16. Pch Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (P−CHANNEL)

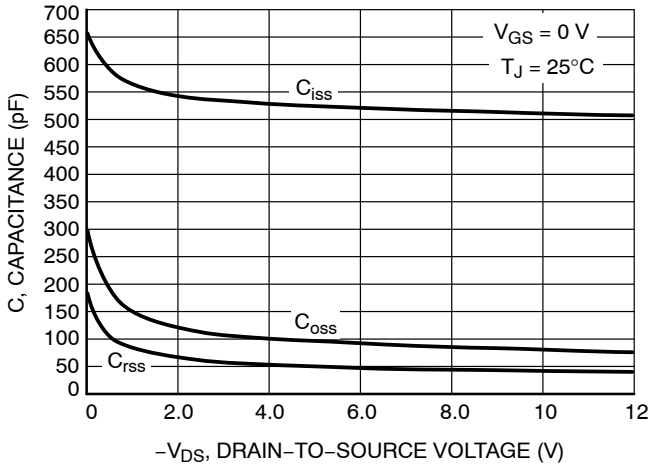


Figure 17. Pch Capacitance Variation

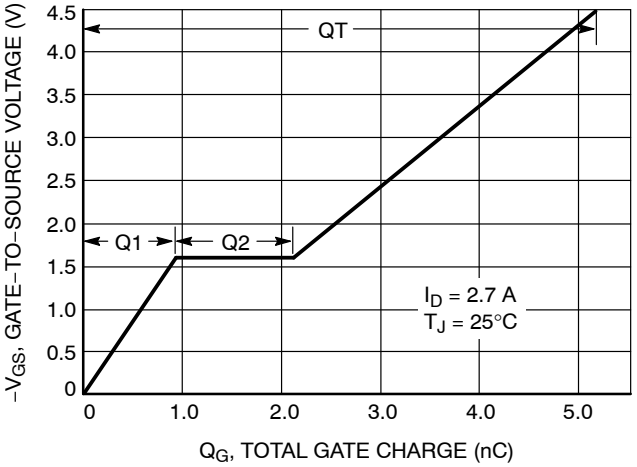


Figure 18. Pch Gate−to−Source Voltage vs. Total Charge

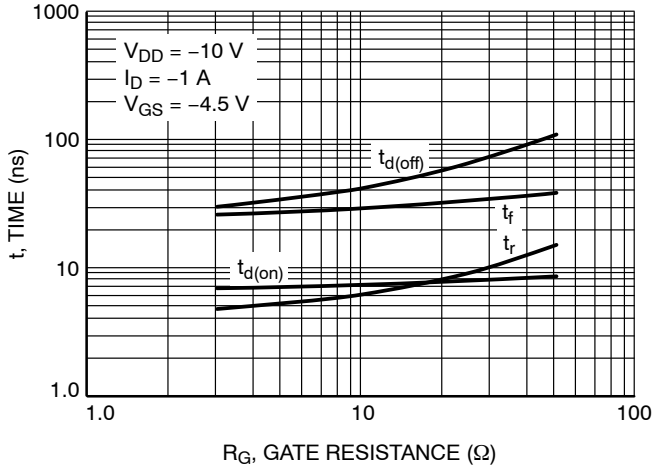


Figure 19. Pch Resistive Switching Time Variation vs. Gate Resistance

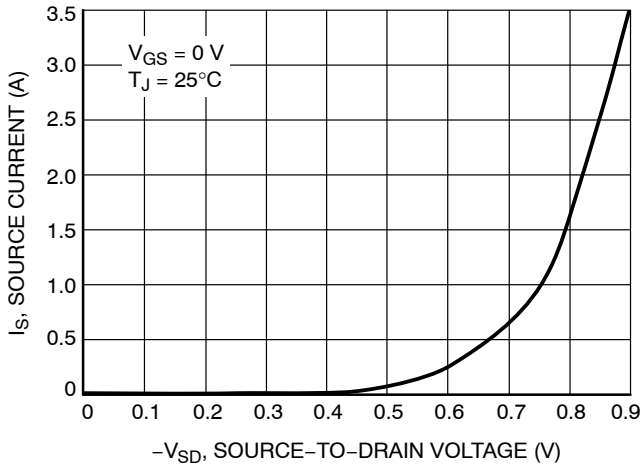
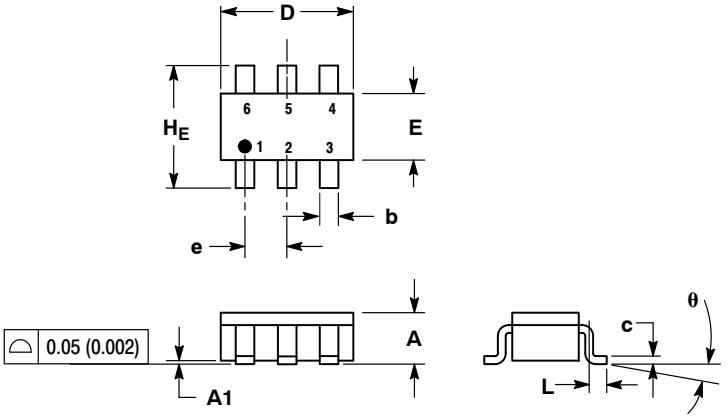


Figure 20. Pch Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE S

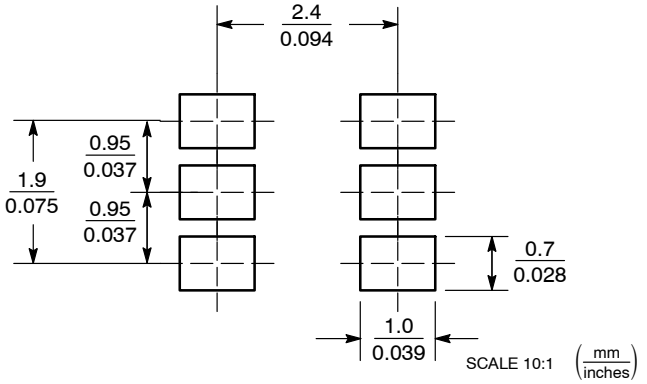


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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