NTGS3441P

Power MOSFET

−20 V, −3.16 A, Single P−Channel TSOP−6

Features

- Ultra Low $R_{DS(on)}$ to Improve Conduction Loss
- Low Gate Charge to Improve Switching Losses
- TSOP−6 Surface Mount Package
- This is a Pb−Free Device

Applications

- High Side Switch in DC−DC Converters
- Battery Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−20	V
Gate−to−Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−2.5	A
		T_A = 85°C		−1.8	
	t = 10 s	T_A = 25°C		−3.16	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.98	W
	t = 10 s			1.60	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−1.8	A
		T_A = 85°C		−1.3	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.51	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−13	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	−1.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0751 in sq)

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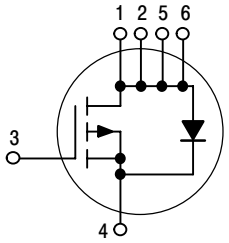
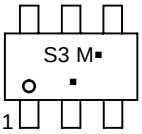
$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
−20 V	91 mΩ @ 4.5 V	−3.16 A
	144 mΩ @ 2.7 V	
	188 mΩ @ 2.5 V	

P−Channel



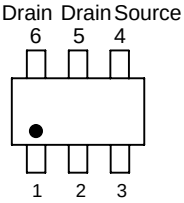
MARKING DIAGRAM

TSOP−6
CASE 318G
STYLE 1



PT = Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTGS3441PT1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Ambient – Steady State (Note 3)	$R_{\theta JA}$	128	°C/W
Junction−to−Ambient – t = 10 s (Note 3)	$R_{\theta JA}$	78	
Junction−to−Ambient – Steady State (Note 4)	$R_{\theta JA}$	244	

3. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
4. Surface−mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				16		mV/ °C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −20 V	T_J = 25°C			−1	μA
			T_J = 125°C			−10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		0.6		1.6	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				3.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = −3.0 A			91	110	mΩ
		V_{GS} = 2.7 V, I_D = −1.5 A			144	165	
		V_{GS} = 2.5 V, I_D = −1.5 A			188		
Forward Transconductance	g_{FS}	V_{DS} = −15 V, I_D =−1.5 A			4.0		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = −15 V			345		pF
Output Capacitance	C_{OSS}				150		
Reverse Transfer Capacitance	C_{RSS}				40		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = −10 V; I_D = −3.0 A			3.25	6.0	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.3		
Gate−to−Source Charge	Q_{GS}				0.6		
Gate−to−Drain Charge	Q_{GD}				1.4		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = −10 V, I_D = −1.5 A, R_G = 4.7 Ω			7.0	12	ns
Rise Time	T_r				14	25	
Turn−Off Delay Time	$t_{d(OFF)}$				13	25	
Fall Time	T_f				4.0	8.0	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −3.0 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = −3.0 A			25		ns
Charge Time	T_a				10		
Discharge Time	T_b				15		
Reverse Recovery Charge	Q_{RR}				15		nC

5. Switching characteristics are independent of operating junction temperatures
6. Pulse Test: pulse width = 300 μs, duty cycle = 2%

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

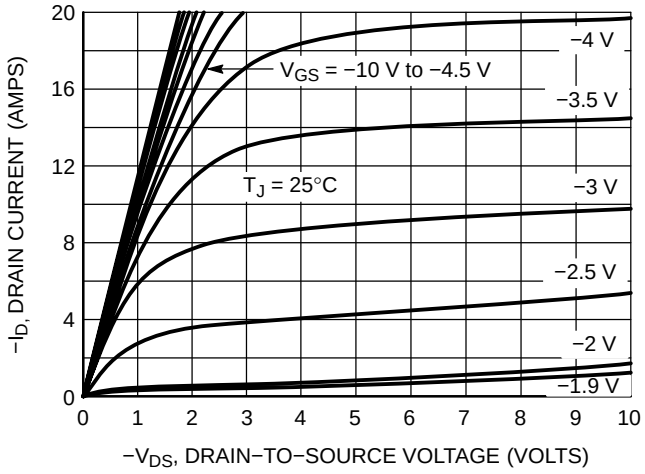


Figure 1. On−Region Characteristics

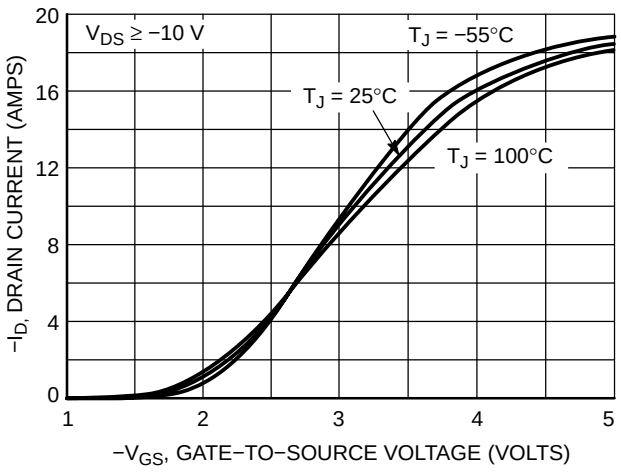


Figure 2. Transfer Characteristics

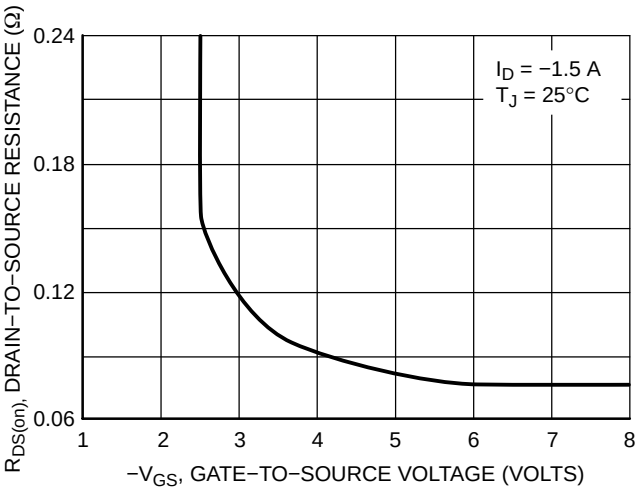


Figure 3. On−Resistance vs. Gate−to−Source Voltage

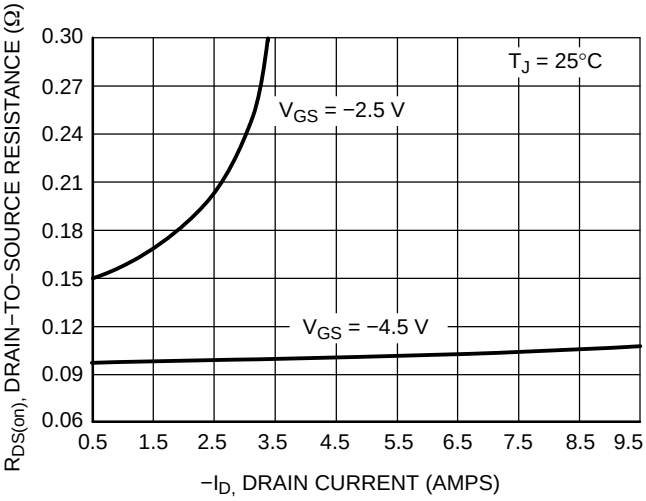


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

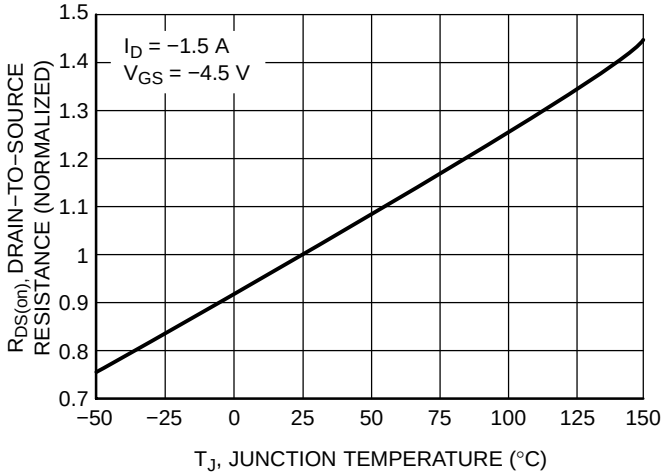


Figure 5. On−Resistance Variation with Temperature

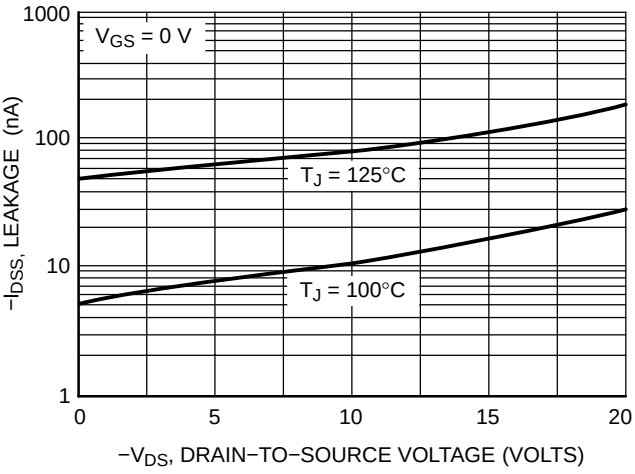


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

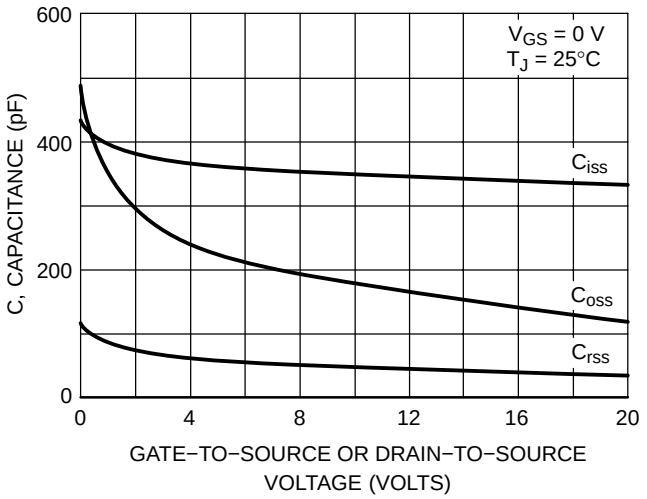


Figure 7. Capacitance Variation

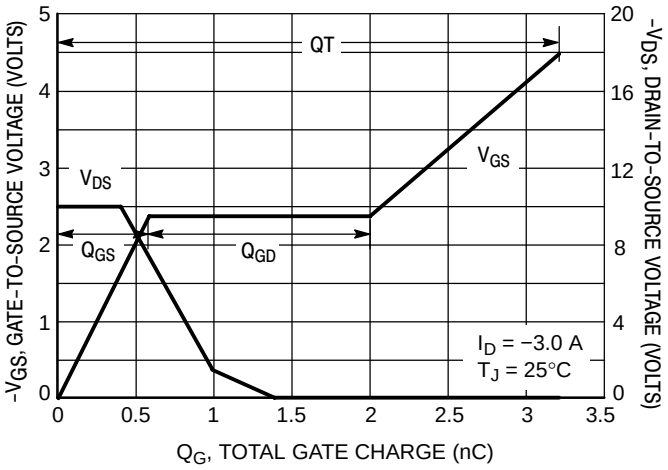


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

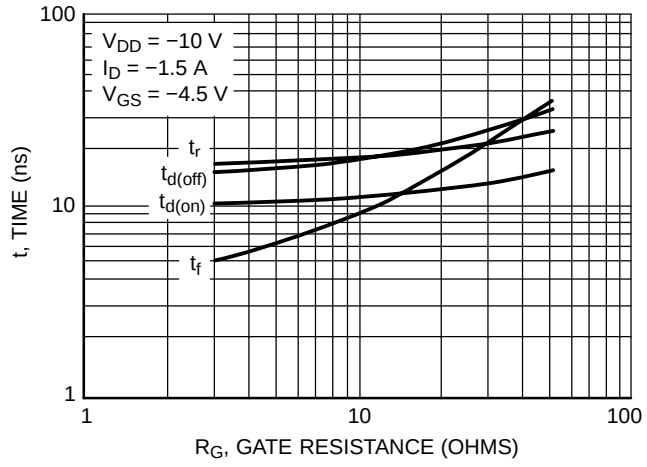


Figure 9. Gate Threshold Voltage Variation with Temperature

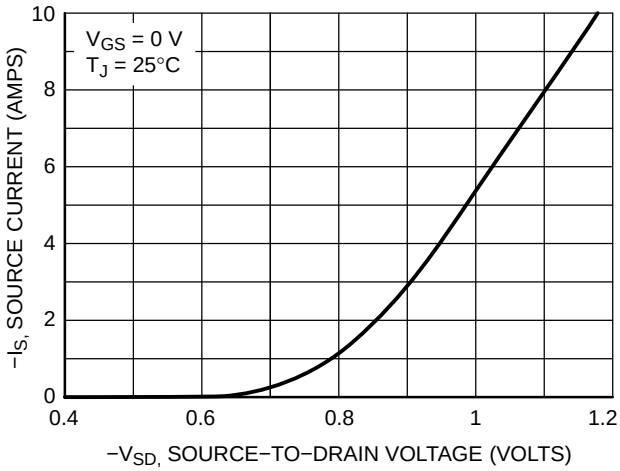
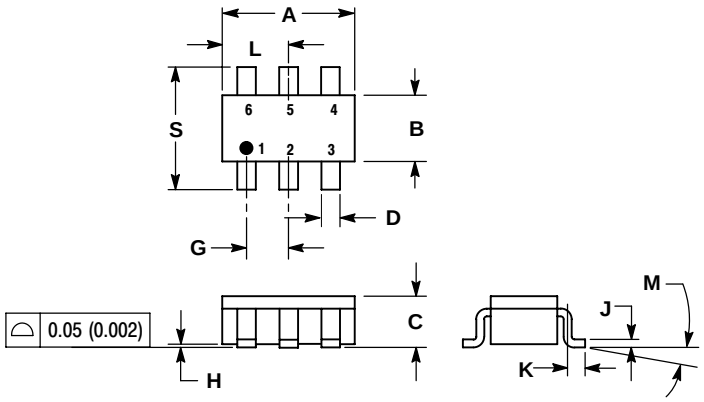


Figure 10. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE N

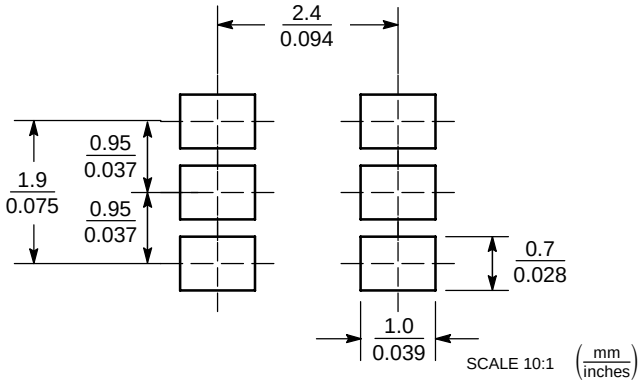


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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