NTH4302

Product Preview

HD3e Quad N-Channel

The NTH4302 is the first integrated Quad FET in a single package. It is the integration of 4 planar TMOS devices. It uses the latest HD3e TMOS technology from ON Semiconductor, with very high cell density and improved switching capability

The NTH4302 is a 16-pin leadless device packaged in the new PInPAK™ from ON Semiconductor. The PInPAK is a new flexible power package that uses the MAP process. The NTH4302 uses the same MOSFET as the NTD60N02R. However, with the PInPAK package, various other pairs of MOSFETs can be used to create additional custom applications.

Features

- Ultra Low R_{DS}(on) Provides Higher Efficiency
- Very Fast Switching due to Planar Technology and Leadless Package
- 200% Footprint Reduction Compared to Similar DPAK Solution for the Same Power
- Up to 80 Amp per FET
- Very Low V_f (0.8 mV) Ideal for Synchronous Rectification
- Specifically Designed for DC-DC Buck Converter in VRM9.1 Application (80 Amp Per Phase, 500 khz)

Application

- DC-DC Converter
- Motherboard/Server Buck Converter
- Telecom/Industrial Power Supply
- Automotive Motor Drive
- H-Bridge

Application Note AND8086/D, “Board Mounting Notes for Quad Flat-Pack No-Lead Package (QFN)”, is available on our web site www.onsemi.com.

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http://onsemi.com

QUAD TMOS POWER MOSFET
40 AMPERES
24 VOLTS
$R_{DS(on)}$ = 7.5 mΩ
C_{iss} = 2050 pF
$R_{\theta JC}$ = 1.3 °C/W

CASE TBD
PInPAK

MARKING DIAGRAM

TBD

xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PINOUT DIAGRAM

TBD

ORDERING INFORMATION

Device	Package	Shipping
NTH4301	ONiPAK	TBD

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

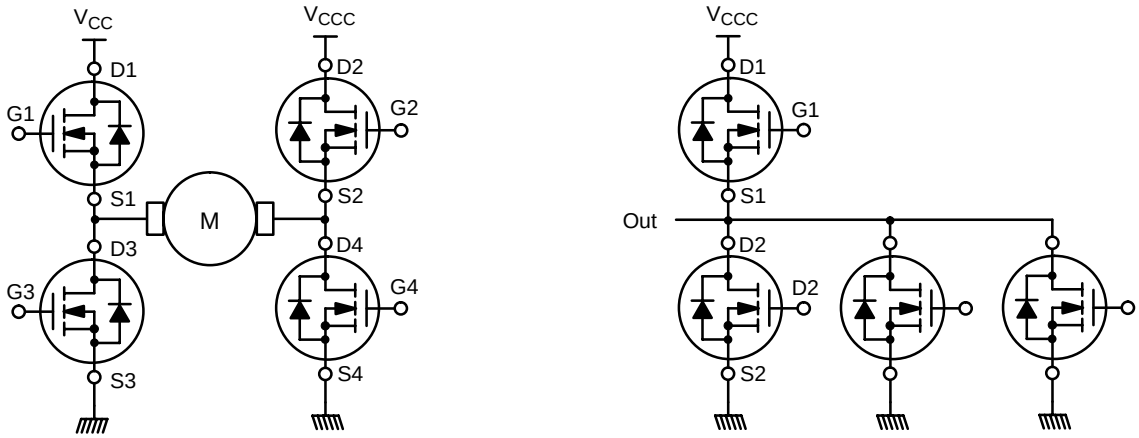

Figure 1.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	24	Vdc
Drain-to-Gate Voltage	V_{DGR}	24	Vdc
Gate-to-Source Voltage	V_{GS}	±20	Vdc
Operating and Storage Temperature	T_J and T_{stg}	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy - Starting T_J = 25°C (Note 1) (V_{DD} = 25 V_{dc}, V_{GS} = 5 V_{dc}, L = 0.1 mH, I_L(pk) = 20 A, R_g = 1 KΩ)	E_{AS}	450	mJ
Drain Current - Continuous @ T_A = 25°C - Continuous @ T_A = 70°C - Single Pulse (t_p ≤ 10 μs)	I_D I_D I_{DM}	30 TBD TBD	A_{dc}
Total Power Dissipation, t ≤ 10 seconds Linear Derating Factor	P_D @ T_A = 25°C	TBD	W mW/°C
Thermal Resistance - Junction-to-Case - Junction-to-Ambient - Junction-to-Ambient (Note 1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.5 30 TBD	°C/W

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μA) Positive Temperature Coefficient		$V_{(BR)DSS}$	24 -	- 25	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = 30 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = 30 Vdc, T_J = 125°C)		I_{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	-	-	±100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Negative Threshold Temperature Coefficient		$V_{GS(th)}$	1.0 -	1.9 -3.8	3.0 -	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc) (V_{GS} = 10 Vdc, I_D = 10 Adc) (V_{GS} = 4.5 Vdc, I_D = 5.0 Adc)		$R_{DS(on)}$	- - -	0.0078 0.0078 0.010	0.010 0.010 0.013	Ω
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 10 Adc)		g_{FS}	-	20	-	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	-	2050	2400	pF
Output Capacitance		C_{oss}	-	640	800	
Reverse Transfer Capacitance		C_{rss}	-	225	310	
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	(V_{DD} = 25 Vdc, I_D = 1.0 Vdc, V_{GS} = 10 Adc, R_G = 6.0 Ω)	$t_{d(on)}$	-	11	20	ns
Rise Time		t_r	-	15	25	
Turn-Off Delay Time		$t_{d(off)}$	-	85	130	
Fall Time		t_f	-	55	90	
Turn-On Delay Time	(V_{DD} = 25 Vdc, I_D = 1.0 Vdc, V_{GS} = 10 Adc, R_G = 2.5 Ω)	$t_{d(on)}$	-	11	20	ns
Rise Time		t_r	-	13	20	
Turn-Off Delay Time		$t_{d(off)}$	-	55	90	
Fall Time		t_f	-	40	75	
Turn-On Delay Time	(V_{DD} = 24 Vdc, I_D = 20 Vdc, V_{GS} = 10 Adc, R_G = 2.5 Ω)	$t_{d(on)}$	-	15	-	ns
Rise Time		t_r	-	25	-	
Turn-Off Delay Time		$t_{d(off)}$	-	40	-	
Fall Time		t_f	-	58	-	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	-	55	80	nC
		Q_{gs} (Q1)	-	5.5	-	
		Q_{gd} (Q2)	-	15	-	
BODY-DRAIN DIODE RATINGS (Note 3)						
Diode Forward On-Voltage (I_S = 2.3 Adc, V_{GS} = 0 Vdc) (I_S = 20 Adc, V_{GS} = 0 Vdc) (I_S = 2.3 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		V_{SD}	- - -	0.75 0.90 0.65	1.0 - -	Vdc
Reverse Recovery Time	(I_S = 2.3 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	-	30	65	ns
		t_a	-	20	-	
		t_b	-	19	-	
Reverse Recovery Stored Charge		Q_{rr}	-	0.043	-	μC

2. Switching characteristics are independent of operating junction temperature.
3. Indicates Pulse Test: Pulse Width ≤ 300 μsec max, Duty Cycle ≤ 2%.

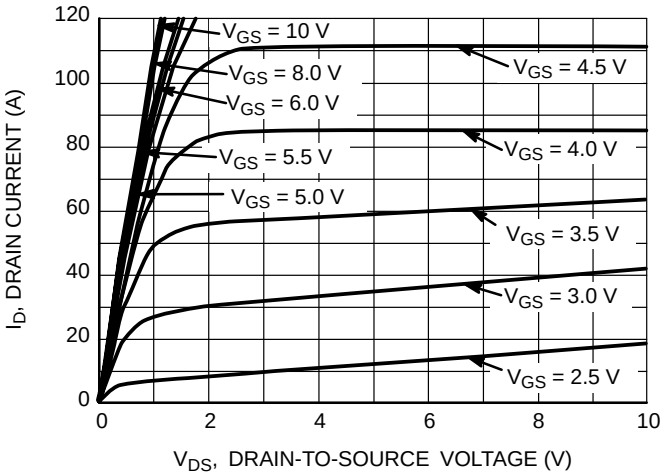

Figure 2. On-Region Characteristics

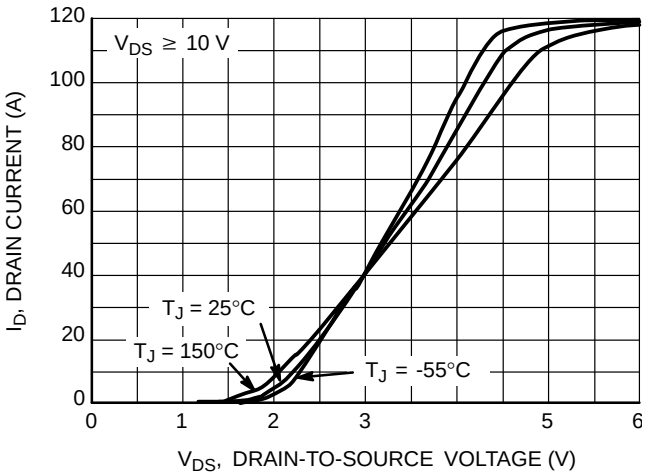

Figure 3. Transfer Characteristics

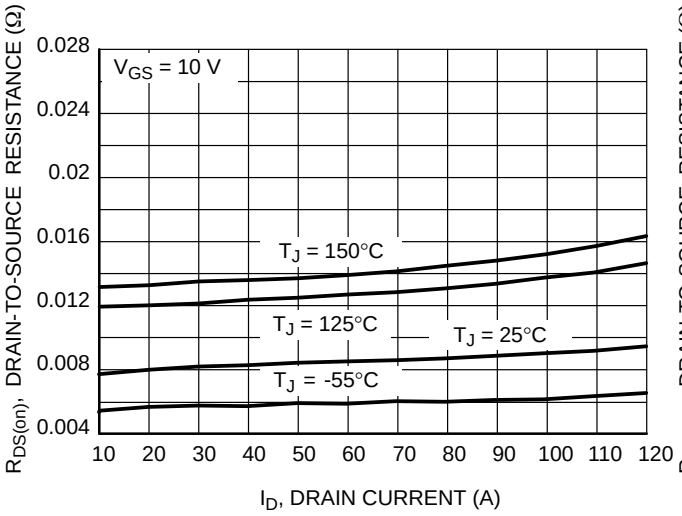

Figure 4. On-Resistance versus Drain Current and Temperature

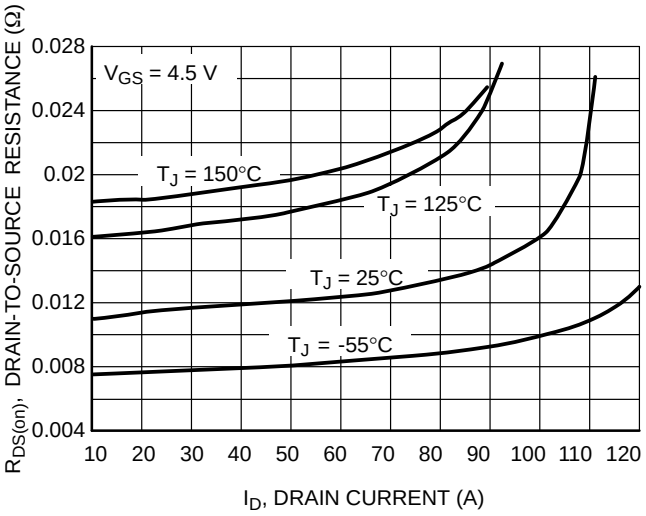

Figure 5. On-Resistance versus Drain Current and Temperature

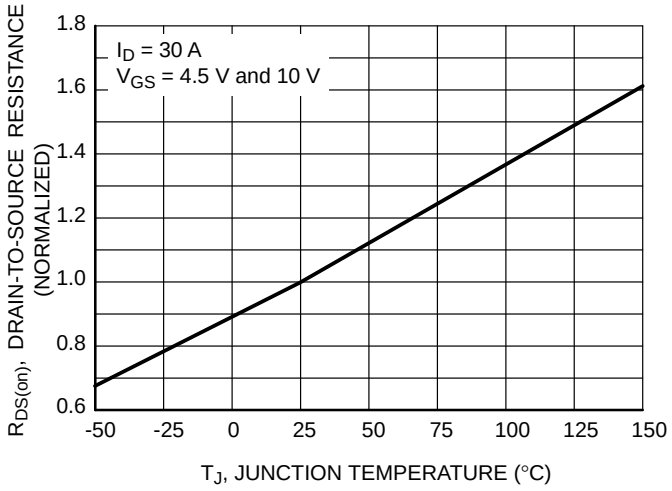

Figure 6. On-Resistance Variation with Temperature

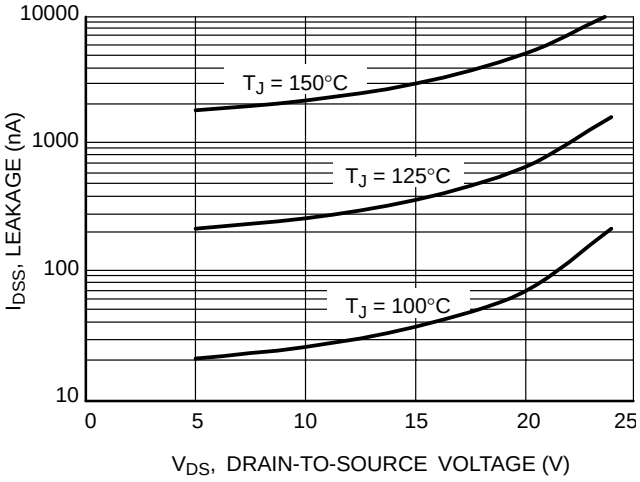

Figure 7. Drain-to-Source Leakage Current versus Voltage

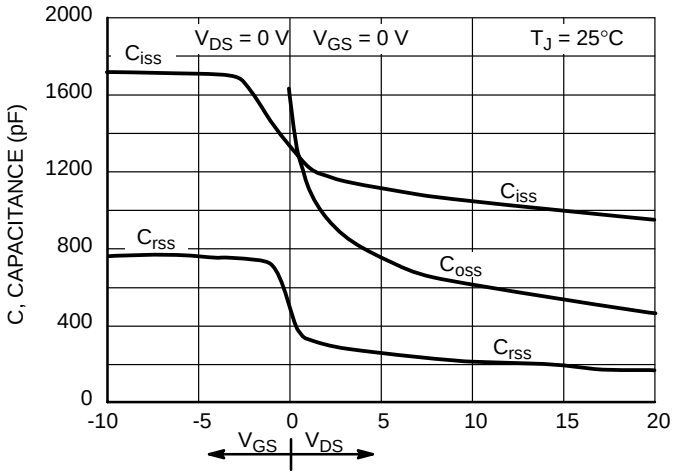

Figure 8. Capacitance Variation

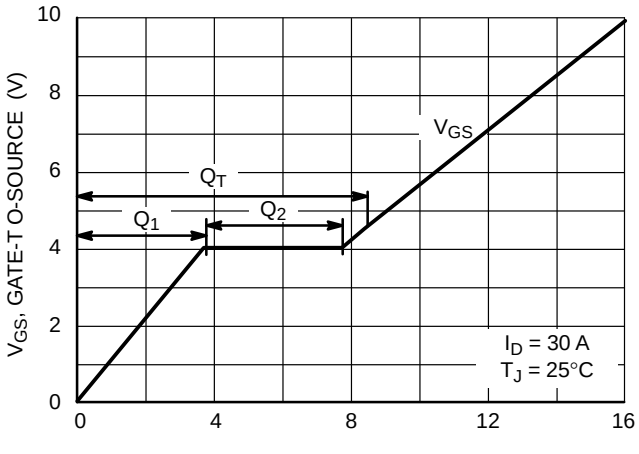

Figure 9. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

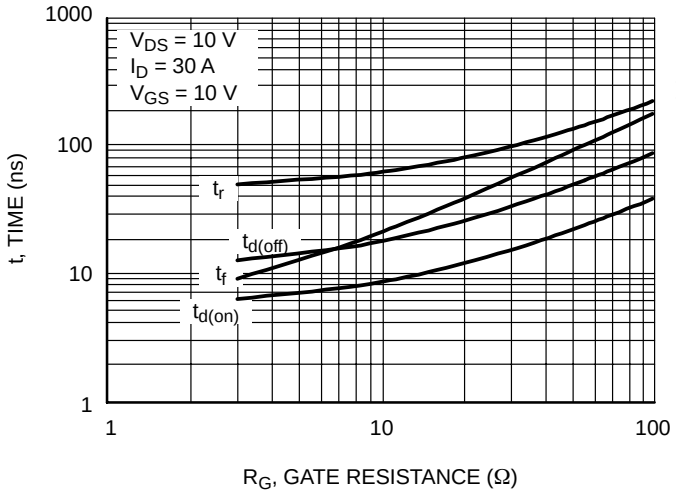

Figure 10. Resistive Switching Time Variation versus Gate Resistance

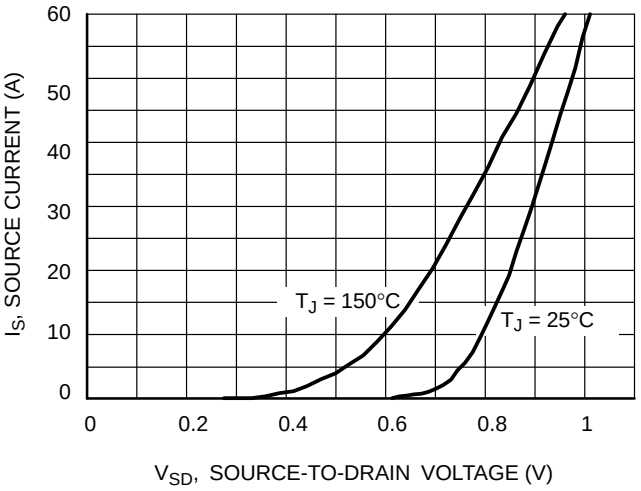

Figure 11. Diode Forward Voltage versus Current

PACKAGE DIMENSIONS

PInPAK
CASE TBD
ISSUE O

PInPAK is a registered trademark of Semiconductor Components Industries, LLC (SCILLC).

PUBLICATION ORDERING INFORMATION

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