# PowerPhase, Dual N-Channel SO8FL

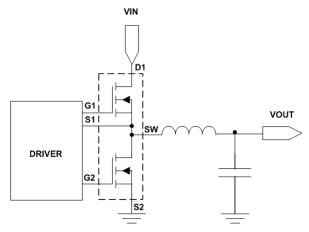
30 V, High Side 20 A / Low Side 26 A

#### **Features**

- Co-Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Applications**

- DC-DC Converters
- System Voltage Rails
- Point of Load



**Figure 1. Typical Application Circuit** 

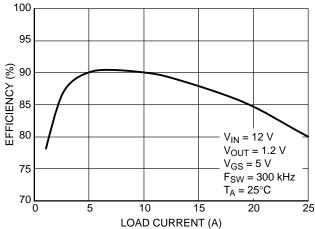


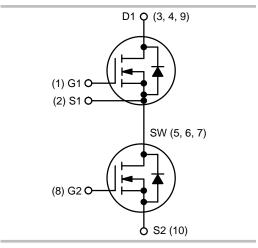
Figure 2. Typical Efficiency Performance POWERPHASEGEVB Evaluation Board



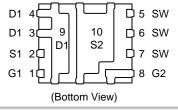
# ON Semiconductor®

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V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
Q1 Top FET	5.4 mΩ @ 10 V	20.4
30 V	8.1 mΩ @ 4.5 V	20 A
Q2 Bottom	3.1 mΩ @ 10 V	26 A
FET 30 V	4.3 mΩ @ 4.5 V	26 A



#### **PIN CONNECTIONS**



#### MARKING DIAGRAM





4C87N = Specific Device Code A = Assembly Location Y = Year

W = Work Week
ZZ = Lot Traceability

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 10 of this data sheet.

# **MAXIMUM RATINGS** ( $T_J = 25^{\circ}C$ unless otherwise stated)

Parameter		Symbol	Value	Unit			
Drain-to-Source Voltage	Q1	V <sub>DSS</sub>	30	V			
Drain-to-Source Voltage	Q2						
Gate-to-Source Voltage	Q1	$V_{GS}$	±20	V			
Gate-to-Source Voltage			Q2				
Continuous Drain Current R <sub>θJA</sub> (Note 1)		T <sub>A</sub> = 25°C	Q1	I <sub>D</sub>	15.4		
		T <sub>A</sub> = 85°C			11.1	1 ,	
		T <sub>A</sub> = 25°C	Q2		19.5	A	
		T <sub>A</sub> = 85°C			14.1	1	
Power Dissipation		T <sub>A</sub> = 25°C	Q1	$P_{D}$	1.89	W	
RθJA (Note 1)			Q2				
Continuous Drain Current $R_{\theta JA} \le 10 \text{ s (Note 1)}$		T <sub>A</sub> = 25°C	Q1	I <sub>D</sub>	21.0		
		T <sub>A</sub> = 85°C			15.1	1 .	
	Steady	T <sub>A</sub> = 25°C	Q2		26.6	A	
	State	T <sub>A</sub> = 85°C			19.2		
Power Dissipation		T <sub>A</sub> = 25°C	Q1	$P_{D}$	3.51	W	
$R_{\theta JA} \le 10 \text{ s (Note 1)}$			Q2				
Continuous Drain Current		T <sub>A</sub> = 25°C	Q1	I <sub>D</sub>	11.7		
R <sub>θJA</sub> (Note 2)		T <sub>A</sub> = 85°C			8.5	1	
		T <sub>A</sub> = 25°C	Q2		14.9	A	
		T <sub>A</sub> = 85°C			10.7	1	
Power Dissipation		T <sub>A</sub> = 25 °C	Q1	$P_{D}$	1.10	W	
R <sub>θJA</sub> (Note 2)			Q2				
Pulsed Drain Current	•	T <sub>A</sub> = 25°C	Q1	I <sub>DM</sub>	160	Α	
		t <sub>p</sub> = 10 μs	Q2		260	1	
Operating Junction and Storage Temperature	Q1	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C			
	Q2						
Source Current (Body Diode)	Q1	I <sub>S</sub>	10	Α			
	Q2		10	1			
Drain to Source DV/DT		dV/dt	6	V/ns			
Single Pulse Drain-to-Source Avalanche Energy (T.	Q1	EAS	20	mJ			
$V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, L = 0.1 \text{ mH}, R_G = 25 \Omega$	Q2	EAS	45	1			
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C			

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface—mounted on FR4 board using 1 sq—in pad, 2 oz Cu.

2. Surface—mounted on FR4 board using the minimum recommended pad size of 100 mm<sup>2</sup>.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	66.0	
Junction-to-Ambient - Steady State (Note 4)	$R_{\theta JA}$	113.7	°C/W
Junction-to-Ambient - (t ≤ 10 s) (Note 3)	$R_{\theta JA}$	35.6	

#### **ELECTRICAL CHARACTERISTICS** (T<sub>.1</sub> = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Co	ondition	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•	•			•	•	•	
Drain-to-Source Break-	Q1	.,	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		30			V
down Voltage	Q2	V <sub>(BR)DSS</sub>			30			
Drain-to-Source Break-	Q1	V <sub>(BR)DSS</sub>				15.8		mV /
down Voltage Temperature Coefficient	Q2	/T <sub>J</sub>				15.3		¯ °c′
Zero Gate Voltage Drain	Q1	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25°C				1	
Current			$V_{DS} = 24 \text{ V}$	T <sub>J</sub> = 125°C			10	μΑ
	Q2		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C			1	, pur
Gate-to-Source Leakage	Q1	I <sub>GSS</sub>	V <sub>GS</sub> = 0 V, V	VDS = ±20 V			100	^
Current Q2						100	nA	
ON CHARACTERISTICS (Not	e 5)							
Gate Threshold Voltage	Q1	V <sub>GS(TH)</sub>	$V_{GS} = VDS$ , $I_D = 250 \mu A$		1.3		2.2	V
	Q2				1.3		2.2	
Negative Threshold Temperature Coefficient	Q1	V <sub>GS(TH)</sub> / T <sub>J</sub>				5.0		mV /
ature Coemcient	Q2	IJ				5.1		°C
Drain-to-Source On Resistance	Q1	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}$	I <sub>D</sub> = 30 A		4.3	5.4	
ance			$V_{GS} = 4.5 \text{ V}$	I <sub>D</sub> = 18 A		6.5	8.1	]
	Q2		$V_{GS} = 10 \text{ V}$	I <sub>D</sub> = 30 A		2.5	3.1	mΩ
			$V_{GS} = 4.5 \text{ V}$ $I_D = 30 \text{ A}$			3.4	4.3	
CAPACITANCES								
Input Capacitance	Q1	C <sub>ISS</sub>				1252		
Input Capacitance Q2		UISS				1939		
Output Capacitanas	Q1	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 15 V			610		pF
Output Capacitance —		OSS	v <sub>GS</sub> = 0 v, 1 = 1 lvl⊓z, v <sub>DS</sub> = 15 v			1055		J P'
Reverse Capacitance	Capacitance C <sub>RSS</sub>			129				
Novorso Capacitanice	Q2	CKSS				49		1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

Surface–mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
 Surface–mounted on FR4 board using the minimum recommended pad size of 100 mm<sup>2</sup>.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition		Min	Тур	Max	Unit
CHARGES, CAPACITANCES	CHARGES, CAPACITANCES & GATE RESISTANCE							
T. 10 . 0	Q1				10.9			
Total Gate Charge	Q2	$Q_{G(TOT)}$				13.8		
Three-chieff Code Observe	Q1	0				1.2		
Threshold Gate Charge	Q2	Q <sub>G(TH)</sub>		45.77.1 00.4		2.0		
Cata ta Causa Chassa	Q1	0	$V_{GS} = 4.5 \text{ V}, V_{DS}$	$= 15 \text{ V}; I_D = 30 \text{ A}$		3.4		nC
Gate-to-Source Charge	Q2	$Q_GS$				5.5		
Cata to Drain Charge	Q1	0				5.4		
Gate-to-Drain Charge	Q2	$Q_GD$				3.6		
Total Cata Charms	Q1	0	V 40.V.V	45.1/-1 20.4		22.2		0
Total Gate Charge	Q2	$Q_{G(TOT)}$	$V_{GS} = 10 \text{ V}, V_{DS}$	= 15 V; I <sub>D</sub> = 30 A		30.3		nC
Cata Basistanas	Q1	$R_{G}$	т	25°C		1.0		0
Gate Resistance	Q2		T <sub>A</sub> =	25°C		1.0		Ω
SWITCHING CHARACTERISTICS (Note 6)								
Turn On Dolov Time	Q1					8.9		
Turn-On Delay Time	Q2	t <sub>d(ON)</sub>			10.6			
Rise Time	Q1	,				21.2		
Rise Time	Q2	t <sub>r</sub>	$V_{GS} = 4.5 \text{ V},$	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$		4.6		
Turn Off Dolov Time	Q1	4	$I_D = 15 A, I$	$R_G = 3.0 \Omega$		15.3		ns
Turn-Off Delay Time	Q2	t <sub>d(OFF)</sub>				21		
Fall Time	Q1	+				4.4		
rali Tillie	Q2	t <sub>f</sub>				4.9		
SWITCHING CHARACTERIS	TICS (No	te 6)						
Turn-On Delay Time	Q1	<b>+</b>				6.7		
Turn-On Delay Time	Q2	t <sub>d(ON)</sub>				8.1		
Rise Time	Q1	+				19.5		
Kise Time	Q2	t <sub>r</sub>	V <sub>GS</sub> = 10 V,	V <sub>DS</sub> = 15 V,		15		ns
Turn-Off Delay Time	Q1	t	$I_{D} = 15 \text{ A}, I$	$R_G = 3.0 \Omega$		20.1		113
Turri-Oil Delay Time	Q2 t <sub>d(OFF)</sub>	'd(OFF)	t <sub>f</sub>			26.2		
Fall Time	Q1	+.				2.8		
rali fillie	Q2	чf				3.1		
DRAIN-SOURCE DIODE CHARACTERISTICS								
	Q1		V <sub>GS</sub> = 0 V,	$T_J = 25^{\circ}C$		0.82		
Forward Voltage	١٧١	V	I <sub>S</sub> = 10 A	$T_J = 125$ °C		1.15		V
i oi waiu voilage	02	V SD	$V_{SD}$ $V_{GS} = 0 V$	$T_J = 25^{\circ}C$		0.8		
Q2	$I_S = 10 \text{ A}$ $T_J = 125^{\circ}\text{C}$		1.10					

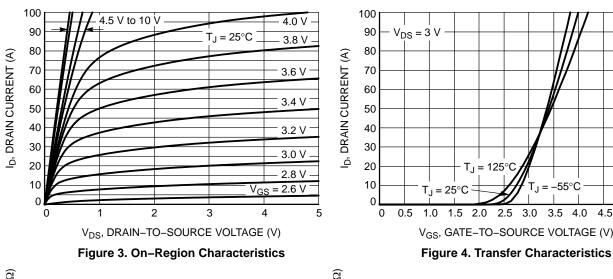
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ . 6. Switching characteristics are independent of operating junction temperatures.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Тур	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
Boyoroo Boooyory Timo	Q1	4	.		29.1		
Reverse Recovery Time	Q2	t <sub>RR</sub>			40.2		
Chargo Timo	Q1	to	ta		14.2		ns
Charge Time	Q2	tb			19.5		
Discharge Time	Q1		$V_{GS} = 0 \text{ V}, d_{IS}/d_t = 100 \text{ A/}\mu\text{s}, I_S = 30 \text{ A}$		14.6		
Discharge Time	Q2		LD		20.6		
Dayoraa Dagayary Charga	Q1	0			21		
Reverse Recovery Charge	Q2	$Q_{RR}$			39		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 5. Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ . 6. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS - Q1**



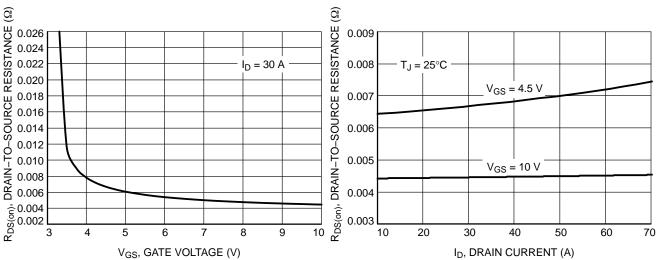


Figure 5. On-Resistance vs. Gate-to-Source Voltage

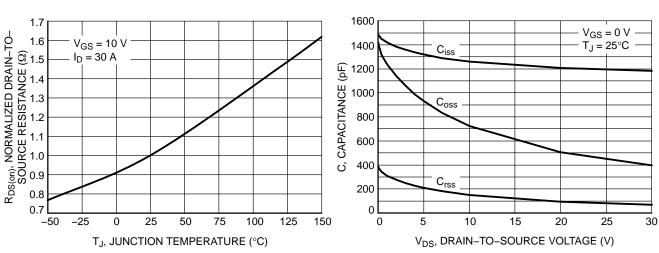


Figure 7. On-Resistance Variation with **Temperature** 

Figure 8. Capacitance Variation

Figure 6. On-Resistance vs. Drain Current and **Gate Voltage** 

3.5 4.0 4.5 5.0 5.5

#### **TYPICAL CHARACTERISTICS - Q1**

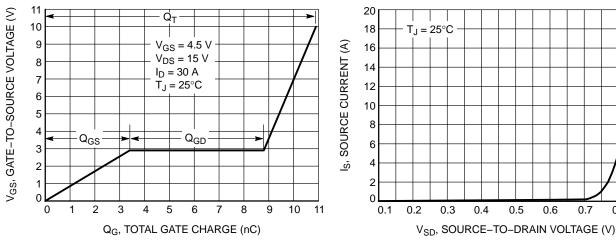


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

Figure 10. Diode Forward Voltage vs. Current

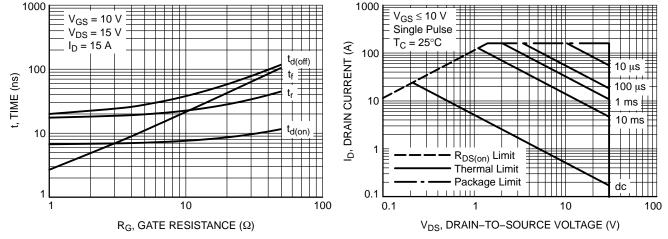


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

Figure 12. Maximum Rated Forward Biased Safe Operating Area

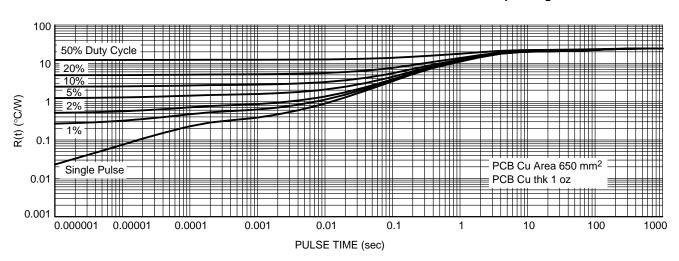


Figure 13. Thermal Characteristics

#### **TYPICAL CHARACTERISTICS - Q2**

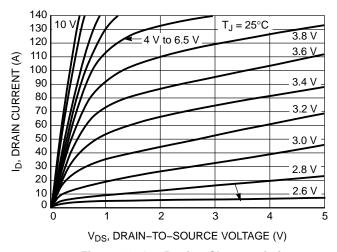


Figure 14. On-Region Characteristics

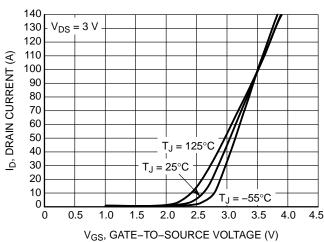


Figure 15. Transfer Characteristics

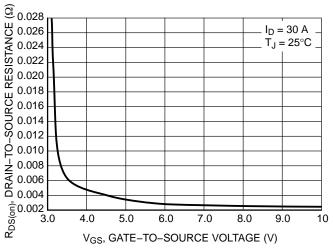


Figure 16. On-Resistance vs. V<sub>GS</sub>

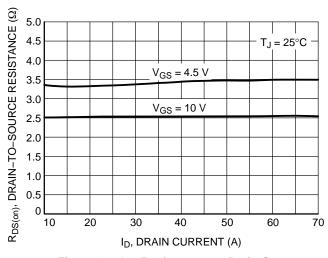


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

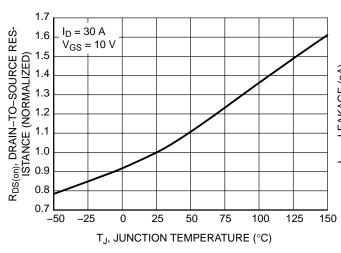


Figure 18. On–Resistance Variation with Temperature

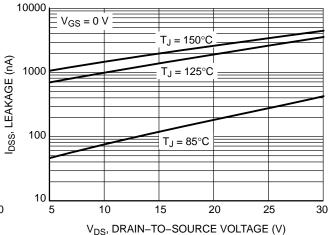


Figure 19. Drain-to-Source Leakage Current vs. Voltage

# **TYPICAL CHARACTERISTICS - Q2**

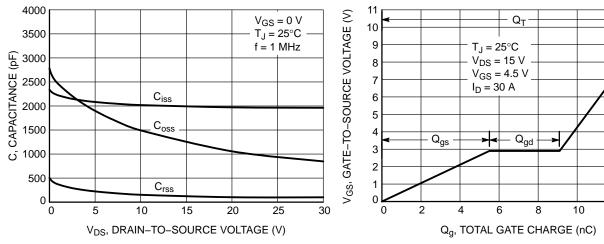


Figure 20. Capacitance Variation

Figure 21. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

12

14

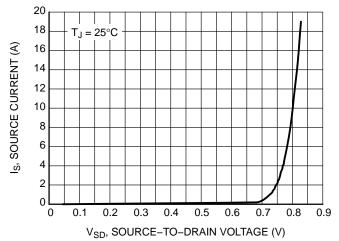


Figure 22. Diode Forward Voltage vs. Current

#### **TYPICAL CHARACTERISTICS - Q2**

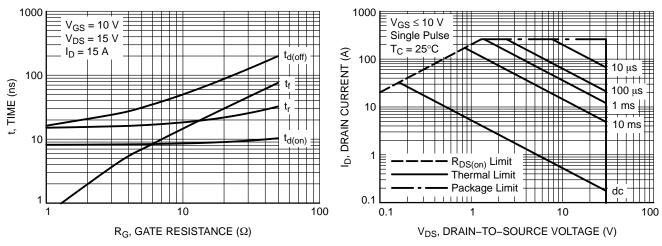


Figure 23. Resistive Switching Time Variation vs. Gate Resistance

Figure 24. Maximum Rated Forward Biased Safe Operating Area

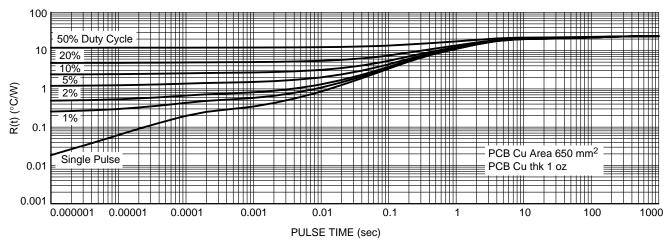


Figure 25. Thermal Characteristics

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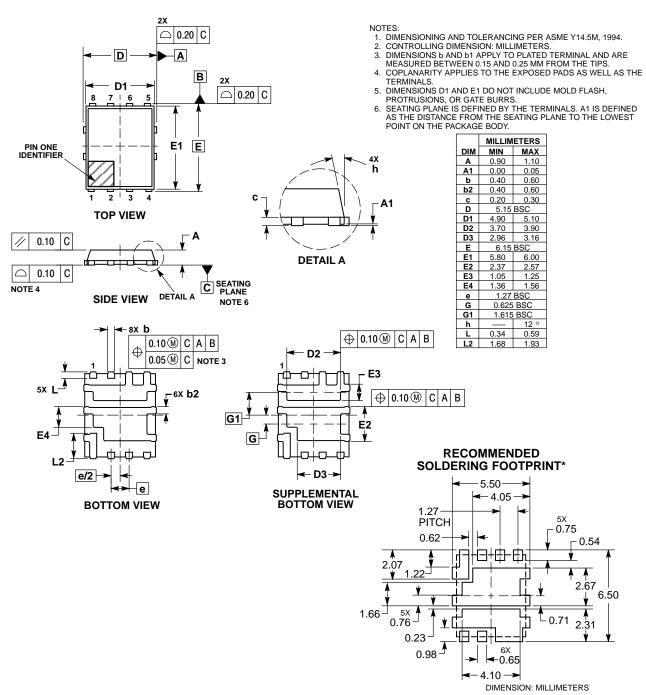
Device	Package	Shipping <sup>†</sup>
NTMFD4C87NT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NTMFD4C87NT3G	DFN8 (Pb-Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

# DFN8 5x6, 1.27P PowerPhase FET CASE 506CR

ISSUE B



<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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