

NTMFS4708N

Power MOSFET

30 V, 19 A, Single N-Channel, SOIC-8 FL

Features

- Fast Switching Times
- Low Gate Charge
- Low $R_{DS(on)}$
- Low Inductance SOIC-8 Package
- These are Pb-Free Devices

Applications

- Notebooks, Graphics Cards
- DC-DC Converters
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D 11.5	A
		$T_A = 85^\circ\text{C}$		
		$t \leq 10\text{ s}$, $T_A = 25^\circ\text{C}$		
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D 2.2	W
		$t \leq 10\text{ s}$	6.25	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D 7.8	A
		$T_A = 85^\circ\text{C}$	5.6	
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D 1.0	W
Pulsed Drain Current	$t_p \leq 10\ \mu\text{s}$	I_{DM} 58	A	
Operating Junction and Storage Temperature	T_J , T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	6.25	A	
Single Pulse Drain-to-Source Avalanche Energy. $V_{DD} = 25\text{ V}$, $V_{GS} = 10\text{ V}$, $I_{PK} = 7.0\text{ A}$, $L = 10\text{ mH}$, $R_G = 25\ \Omega$	E_{AS}	245	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	56.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	20	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	124	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq).

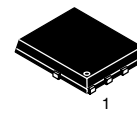
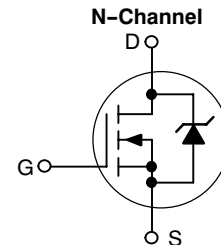


www.DataSheet4U.com

ON Semiconductor®

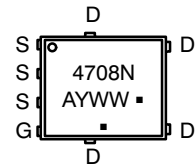
http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
30 V	7.3 m Ω @ 10 V	19 A
	10.1 m Ω @ 4.5 V	



SOIC-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM & PIN ASSIGNMENT



4708N = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4708NT1G	SOIC-8 FL (Pb-Free)	1500 / \bar{a} pe & Reel
NTMFS4708NT3G	SOIC-8 FL (Pb-Free)	5000 / \bar{a} pe & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFS4708N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			10		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25°C		1.0	μA
			T _J = 125°C		50	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 11.5 A		7.3	10	mΩ
		V _{GS} = 4.5 V, I _D = 9.5 A		10.1	14	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 11.5 A		23		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 24 V		970		pF
Output Capacitance	C _{OSS}			440		
Reverse Transfer Capacitance	C _{RSS}			115		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 11.5 A		10	15	nC
Threshold Gate Charge	Q _{G(TH)}			1.3		
Gate-to-Source Charge	Q _{GS}			2.6		
Gate-to-Drain Charge	Q _{GD}			4.8		
Gate Resistance	R _G			1.95		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 15 V, I _D = 1.0 A, R _G = 3.0 Ω		6.7		ns
Rise Time	t _r			4.3		
Turn-Off Delay Time	t _{d(off)}			20		
Fall Time	t _f			16		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 6.25 A	T _J = 25°C	0.78	1.0	V
			T _J = 125°C	0.60		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 6.25 A		32		ns
Charge Time	t _a			15.5		
Discharge Time	t _b			16.5		
Reverse Recovery Charge	Q _{RR}			24		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTMFS4708N

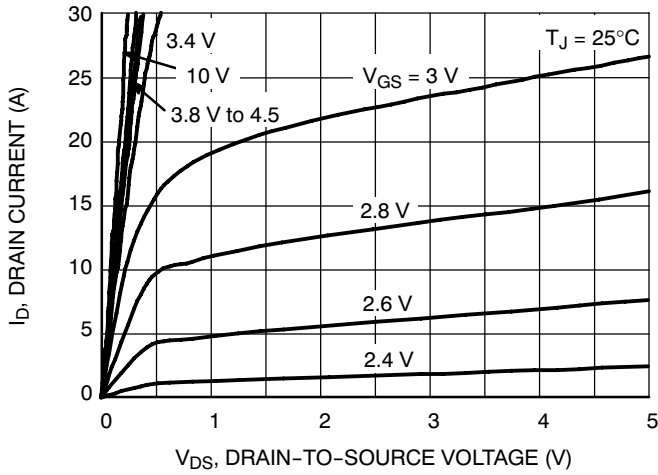


Figure 1. On-Region Characteristics

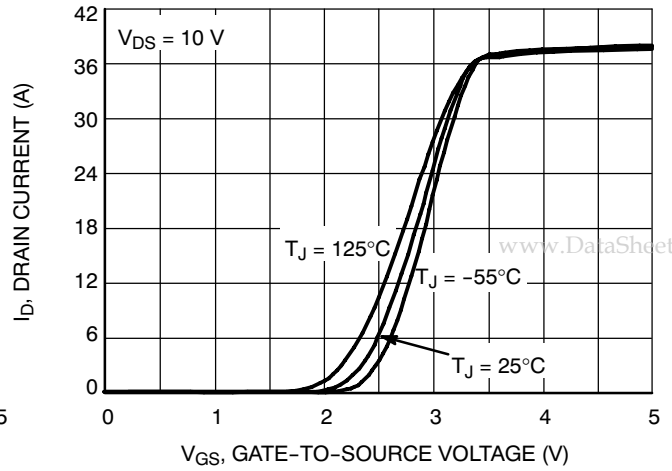


Figure 2. Transfer Characteristics

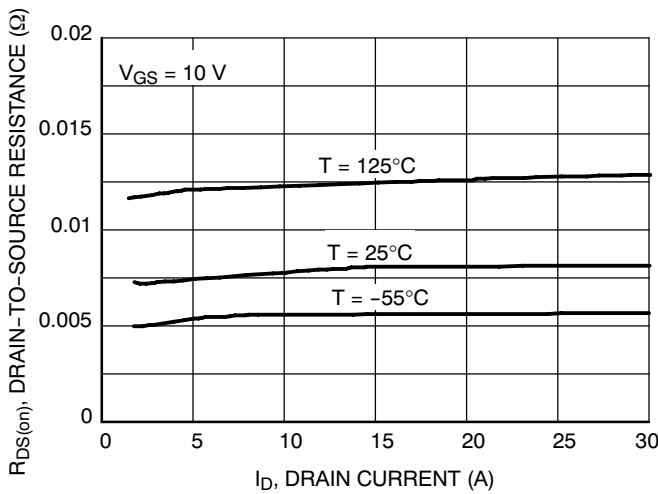


Figure 3. On-Resistance versus Drain Current and Temperature

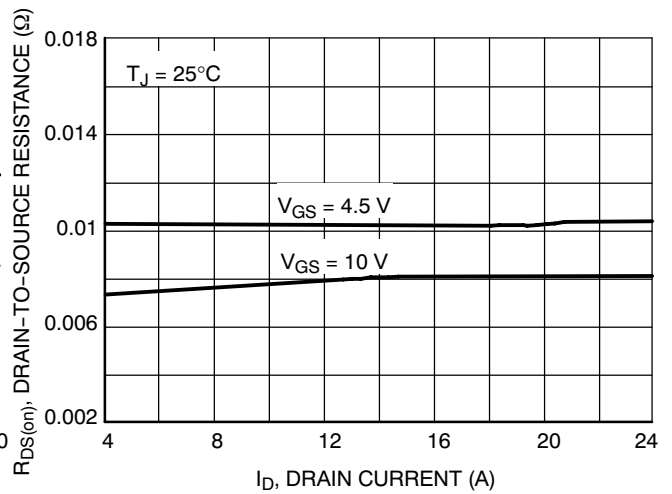


Figure 4. On-Resistance versus Drain Current and Gate Voltage

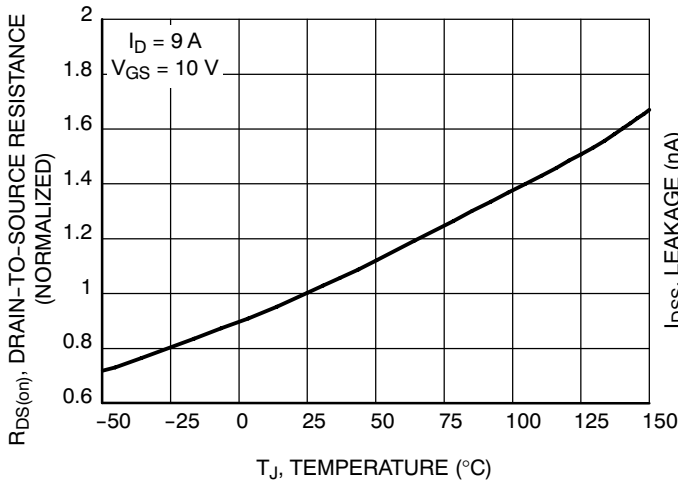


Figure 5. On-Resistance Variation with Temperature

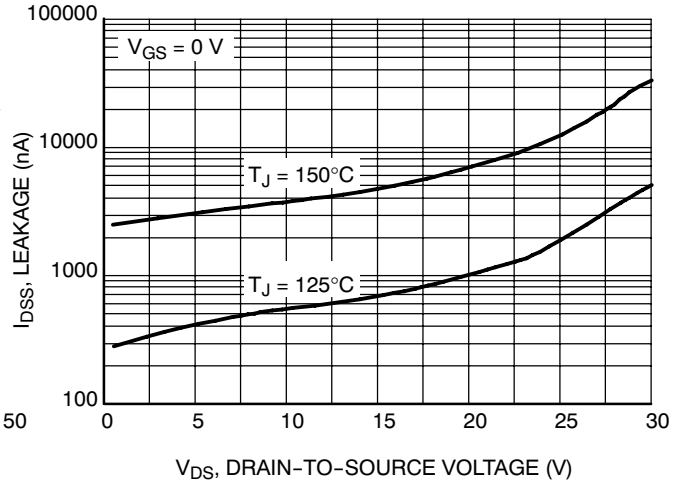


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTMFS4708N

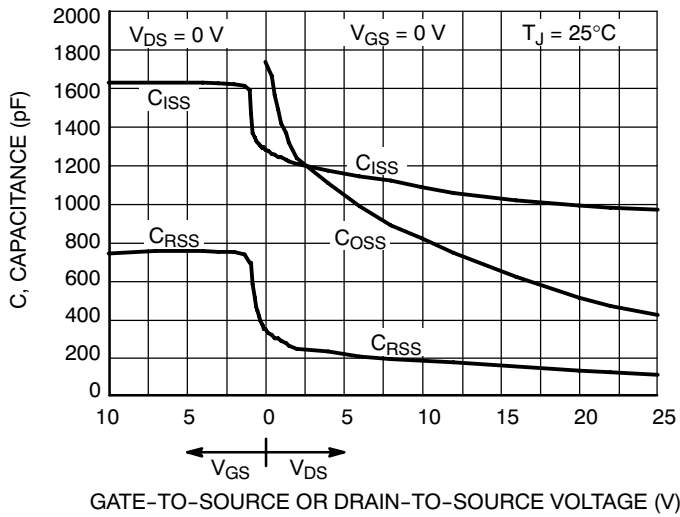


Figure 7. Capacitance Variation

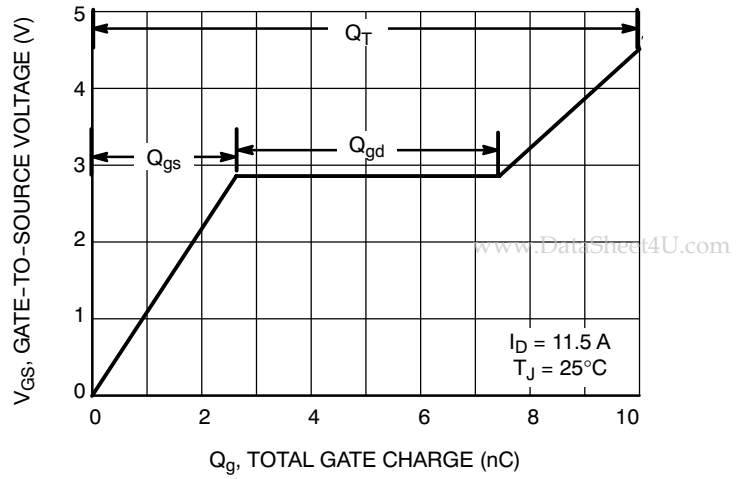


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

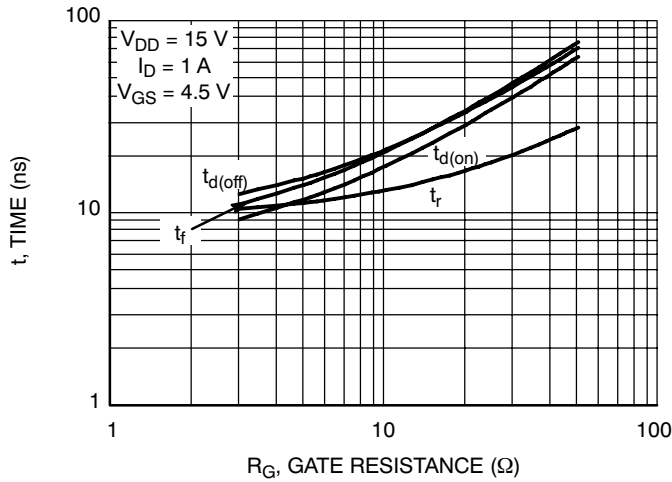


Figure 9. Resistive Switching Time Variation versus Gate Resistance

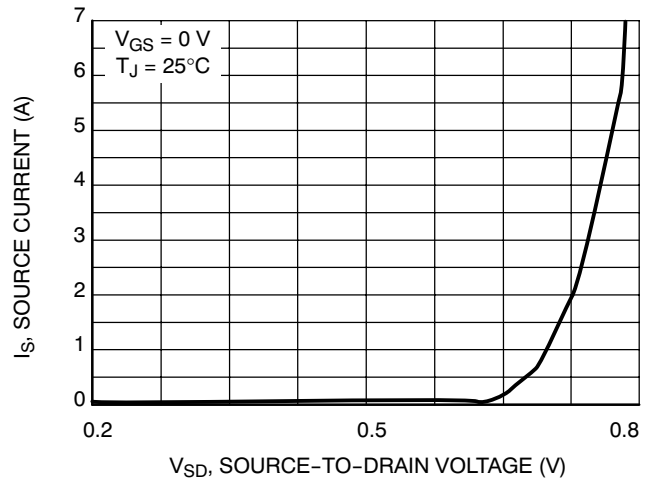


Figure 10. Diode Forward Voltage versus Current

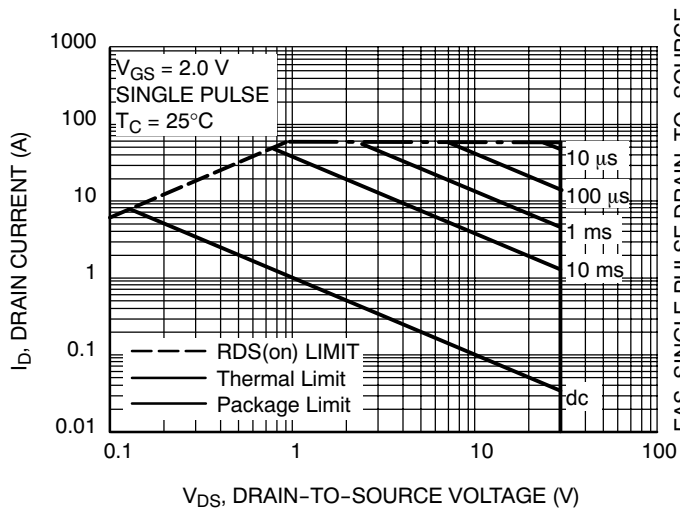


Figure 11. Maximum Rated Forward Biased Safe Operating Area

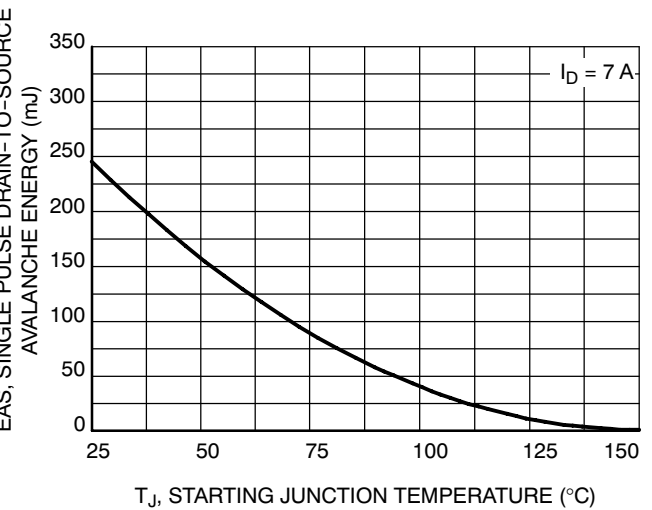
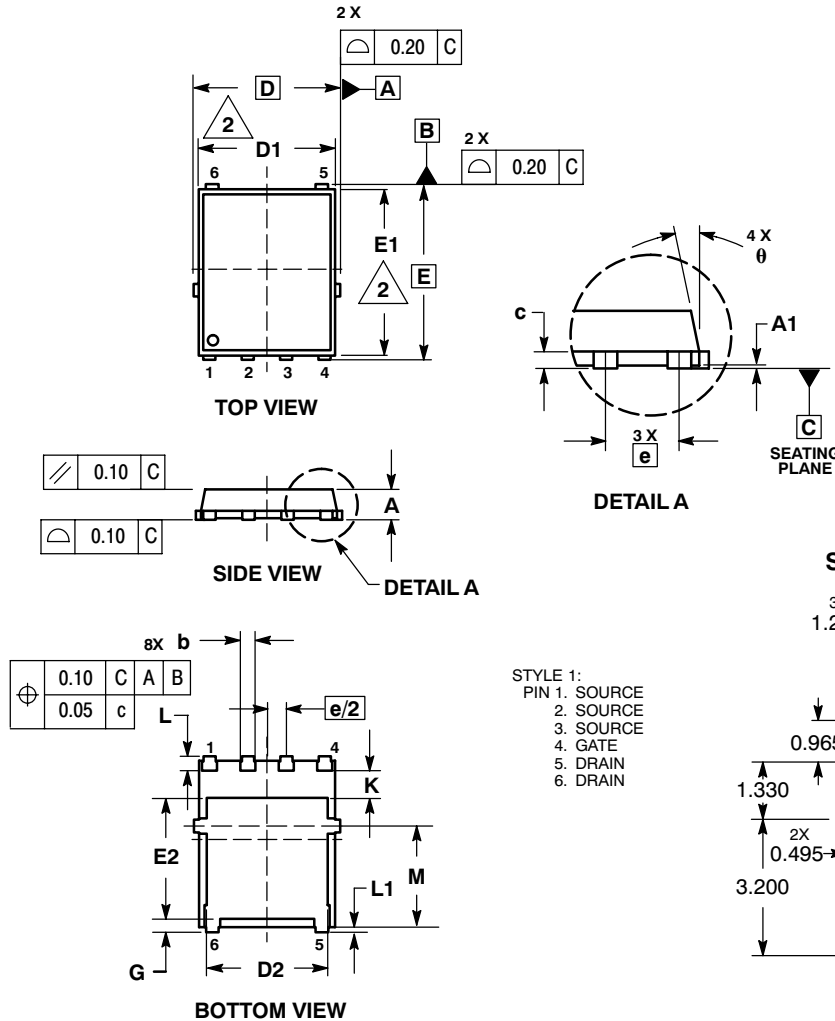


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

NTMFS4708N

PACKAGE DIMENSIONS

DFN6 5x6, 1.27P (SO8 FL)
CASE 488AA-01
ISSUE C

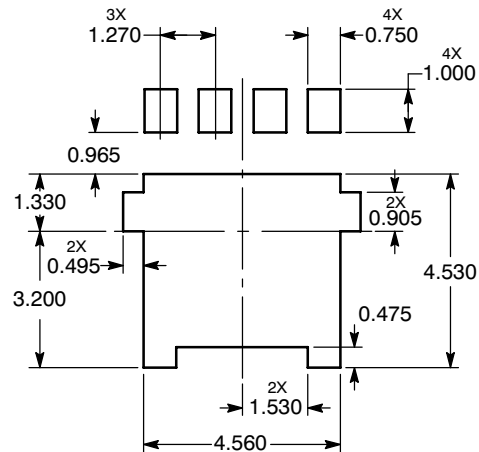


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	0.51	---	---
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
theta	0°	---	12°

SOLDERING FOOTPRINT*



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
RD, Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative