Power MOSFET

30 V, 52 A, Single N-Channel, SO-8 FL

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

			1			
Parameter			Symbol	Value	Unit	
Drain-to-Source Volt	age		V_{DSS}	30	V	
Gate-to-Source Volta	age		V_{GS}	±20	V	
Continuous Drain Current R _{B.IA}		T _A = 25°C	I _D	16.4	Α	
(Note 1)	Steady State T _A = 25° Package and Storage	$T_A = 80^{\circ}C$		12.3		
Power Dissipation $R_{\theta JA}$ (Note 1)		T _A = 25°C	P _D	2.51	W	
Continuous Drain		$T_A = 25^{\circ}C$	I _D	25.3	Α	
Current $R_{\theta JA} \le 10 \text{ s}$ (Note 1)		T _A = 80°C		19.0		
Power Dissipation $R_{\theta JA} \le 10 \text{ s (Note 1)}$		T _A = 25°C	P _D	6.0	W	
Continuous Drain Current R _{0.1A}	State	T _A = 25°C	I _D	9.0	Α	
(Note 2)	Steady State TA = 25°C Package and Storage dy Diode) dt to-Source Av $V_{GS} = 10 \text{ V, I}$	T _A = 80°C		6.8		
Power Dissipation $R_{\theta JA}$ (Note 2)		T _A = 25°C	P _D	0.76	W	
Continuous Drain Current R _{0.IC}		$T_C = 25^{\circ}C$	I _D	52	Α	
(Note 1)		T _C =80°C		39		
Power Dissipation $R_{\theta JC}$ (Note 1)		T _C = 25°C	P _D	25.5	W	
Pulsed Drain Current	$T_A = 25^{\circ}$	$^{\circ}$ C, $t_{p} = 10 \ \mu s$	I _{DM}	146	Α	
Current Limited by Pa	ckage	$T_A = 25^{\circ}C$	I _{Dmax}	80	Α	
Operating Junction ar Temperature	nd Storage		T _J , T _{STG}	–55 to +150	°C	
Source Current (Body	/ Diode)		IS	23	Α	
Drain to Source dV/dt		dV/d _t	7.0	V/ns		
Single Pulse Drain–to–Source Avalanche Energy (T _J = 25° C, V _{GS} = 10 V, I _L = 29 A _{pk} , L = 0.1 mH, R _{GS} = 25 Ω) (Note 3)		E _{AS}	42	mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

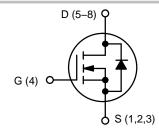
- 1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- 2. Surface—mounted on FR4 board using the minimum recommended pad size.
- 3. Parts are 100% tested at $T_J = 25$ °C, $V_{GS} = 10$ V, $I_L = 20$ A_{pk} , EAS = 20 mJ.



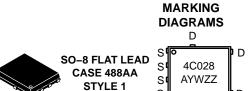
ON Semiconductor®

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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
30 V	4.73 mΩ @ 10 V	52 A
30 V	7.0 mΩ @ 4.5 V	32 A



N-CHANNEL MOSFET



A = Assembly Location

Y = Year W = Work Week ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFS4C028NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4C028NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.9	
Junction-to-Ambient - Steady State (Note 4)	$R_{\theta JA}$	49.8	°C/W
Junction-to-Ambient - Steady State (Note 5)	$R_{\theta JA}$	164.6	*C/vv
Junction–to–Ambient – (t ≤ 10 s) (Note 4)	$R_{\theta JA}$	21.0	

- 4. Surface–mounted on FR4 board using 1 sq-in pad, 1 oz Cu.5. Surface–mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•						•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage (transient)	V _{(BR)DSSt}	$V_{GS} = 0 \text{ V}, I_{D(aval)} = 8.4 \text{ A},$ $T_{case} = 25^{\circ}\text{C}, t_{transient} = 100 \text{ ns}$		34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				14.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}				1.0		
			T _J = 125°C			10	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$				±100	nA
ON CHARACTERISTICS (Note 6)					-		
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		1.3		2.1	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				4.8		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A		3.9	4.73	<u> </u>
	V _{GS} = 4.5 V I _D = 18 A 5.8	5.8	7.0	mΩ			
Forward Transconductance	9FS	V _{DS} = 1.5 V, I _D = 15 A			50		S
Gate Resistance	R_{G}	T _A = 25°C		0.3	1.0	2.0	Ω
CHARGES AND CAPACITANCES	•				•		•
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 15 V			1252		pF
Output Capacitance	C _{OSS}				610		
Reverse Transfer Capacitance	C _{RSS}				126		
Capacitance Ratio	C _{RSS} /C _{ISS}	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz			0.101		
Total Gate Charge	$Q_{G(TOT)}$				10.9		
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}; I_D = 30 \text{ A}$			1.9		nC
Gate-to-Source Charge	Q_GS				3.4		
Gate-to-Drain Charge	Q_{GD}				5.4		
Gate Plateau Voltage	V_{GP}				3.1		V
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V; I _D = 30 A			22.2		nC
SWITCHING CHARACTERISTICS (Note 7)							
Turn-On Delay Time	t _{d(ON)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$ $I_{D} = 15 \text{ A}, R_{G} = 3.0 \Omega$			10		
Rise Time	t _r				32		ns
Turn-Off Delay Time	t _{d(OFF)}				16		
Fall Time	t _f				6.0		

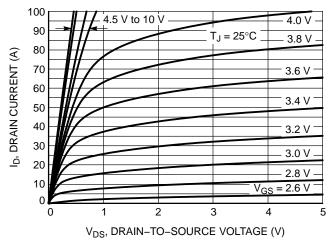
- 6. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$.
 7. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
SWITCHING CHARACTERISTICS (N	lote 7)			•	•	•	
Turn-On Delay Time	t _{d(ON)}	V_{GS} = 10 V, V_{DS} = 15 V, I_{D} = 15 A, R_{G} = 3.0 Ω			7.0		- ns
Rise Time	t _r				28		
Turn-Off Delay Time	t _{d(OFF)}				20		
Fall Time	t _f				4.0		
DRAIN-SOURCE DIODE CHARACT	ERISTICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 V$	$V_{GS} = 0 \text{ V}, \qquad T_{J} = 25^{\circ}\text{C}$		0.79	1.1	V
		$V_{GS} = 0 \text{ V},$ $I_{S} = 10 \text{ A}$	T _J = 125°C		0.65		
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, dIS/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 30 \text{ A}$			31		
Charge Time	t _a				15		ns
Discharge Time	t _b				16		1
Reverse Recovery Charge	Q_{RR}				15		nC

^{6.} Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

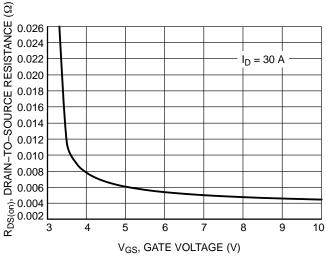
TYPICAL CHARACTERISTICS



100 90 $V_{DS} = 5 V$ 80 ID, DRAIN CURRENT (A) 70 60 50 40 30 20 $T_J = 125^{\circ}C$ 10 $T_J = -55^{\circ}C$ $T_J = 25^{\circ}C$ 0.5 2.5 3.0 3.5 4.0 1.0 1.5 2.0 V_{GS}, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



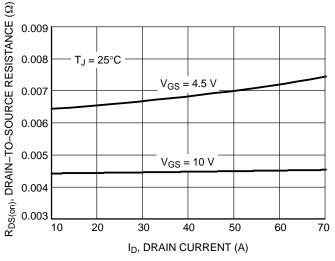
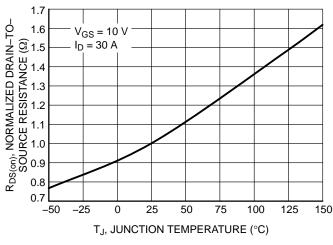


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



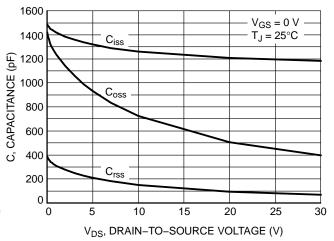


Figure 5. On–Resistance Variation with Temperature

Figure 6. Capacitance Variation

TYPICAL CHARACTERISTICS

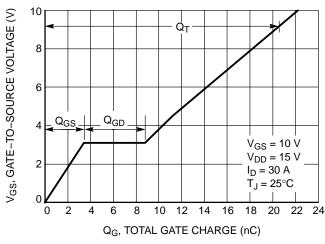


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

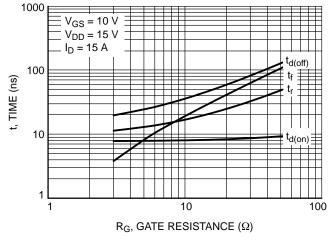


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

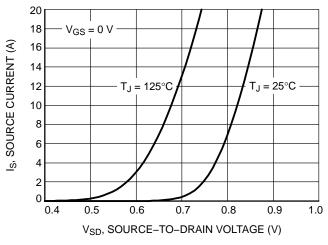


Figure 9. Diode Forward Voltage vs. Current

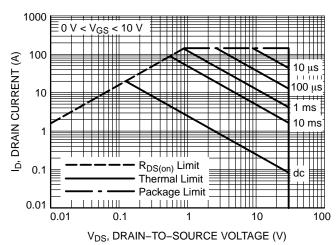


Figure 10. Maximum Rated Forward Biased Safe Operating Area

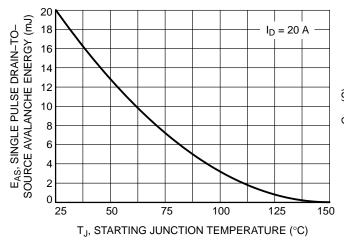


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

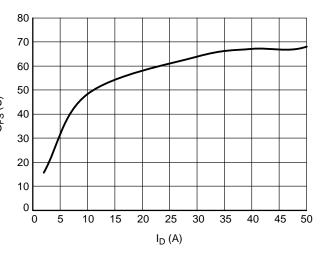


Figure 12. G_{FS} vs. I_D

TYPICAL CHARACTERISTICS

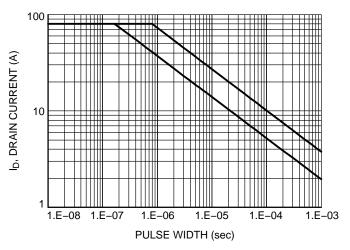


Figure 13. Avalanche Characteristics

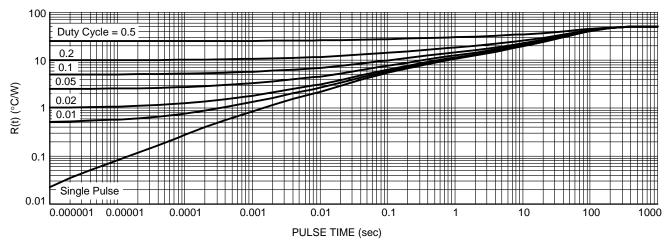
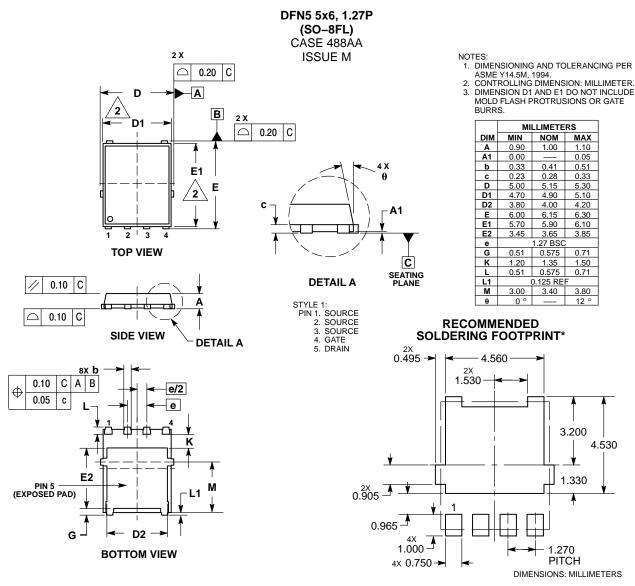


Figure 14. Thermal Response

PACKAGE DIMENSIONS



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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