

# NTMFS5834NL, NVMFS5834NL

## Power MOSFET

40 V, 75 A, 9.3 mΩ, Single N-Channel

### Features

- Low  $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- NVMF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DS}$	40	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	14	A
		$T_A = 100^\circ\text{C}$	12	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	3.6	W
		$T_A = 100^\circ\text{C}$	2.5	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	75	A
		$T_C = 100^\circ\text{C}$	63	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	$T_C = 25^\circ\text{C}$	107	W
		$T_C = 100^\circ\text{C}$	75	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	276	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	75	A	
Single Pulse Drain-to-Source Avalanche Energy ( $L = 0.1 \text{ mH}$ )	EAS	48	mJ	
	IAS	31	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL RESISTANCE MAXIMUM RATINGS

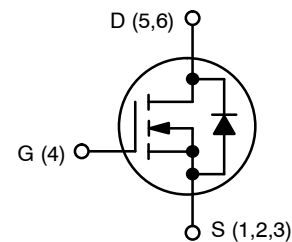
Parameter	Symbol	Value	Unit
Junction-to-Case (Bottom) (Note 1)	$R_{\theta JC}$	1.4	$^\circ\text{C/W}$
Junction-to-Case (Top) (Note 1)	$R_{\theta JC}$	4.5	
Junction-to-Ambient Steady State (Note 1)	$R_{\theta JA}$	41	
Junction-to-Ambient Steady State (Note 2)	$R_{\theta JA}$	75	



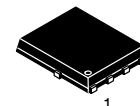
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	9.3 mΩ @ 10 V	75 A
	13.6 mΩ @ 4.5 V	

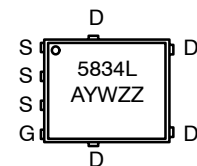


N-CHANNEL MOSFET



DFN5  
(SO-8FL)  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS5834NLT1G	DFN5 (Pb-Free)	1500/Tape & Reel
NVMFS5834NLT1G	DFN5 (Pb-Free)	1500/Tape & Reel
NVMFS5834NLT3G	DFN5 (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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1. Surface-mounted on FR4 board using 1 sq-in pad  
(Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using 0.155 in sq (100mm<sup>2</sup>) pad size.

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			34.7		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25\text{ °C}$		1.0	$\mu\text{A}$
			$T_J = 125\text{ °C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		3.0	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.7		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$		7.1	9.3	mΩ
		$V_{GS} = 4.5\text{ V}$	$I_D = 20\text{ A}$		11.3	13.6	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}$		29		S	

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		1231		pF
Output Capacitance	$C_{OSS}$			198		
Reverse Transfer Capacitance	$C_{RSS}$			141		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 20\text{ A}$		24		nC
Total Gate Charge	$Q_{G(TOT)}$			12		
Threshold Gate Charge	$Q_{G(TH)}$			1.0		
Gate-to-Source Charge	$Q_{GS}$			4.2		
Gate-to-Drain Charge	$Q_{GD}$			6.3		
Plateau Voltage	$V_{GP}$			3.4		
Gate Resistance	$R_G$			0.7		Ω

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 20\text{ A}, R_G = 2.5\ \Omega$		10		ns
Rise Time	$t_r$			56.4		
Turn-Off Delay Time	$t_{d(OFF)}$			17.4		
Fall Time	$t_f$			6.6		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$	$T_J = 25\text{ °C}$	0.84	1.2	V
			$T_J = 125\text{ °C}$	0.72		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 20\text{ A}$		18		ns
Charge Time	$t_a$			10		
Discharge Time	$t_b$			8.0		
Reverse Recovery Charge	$Q_{RR}$			108		

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

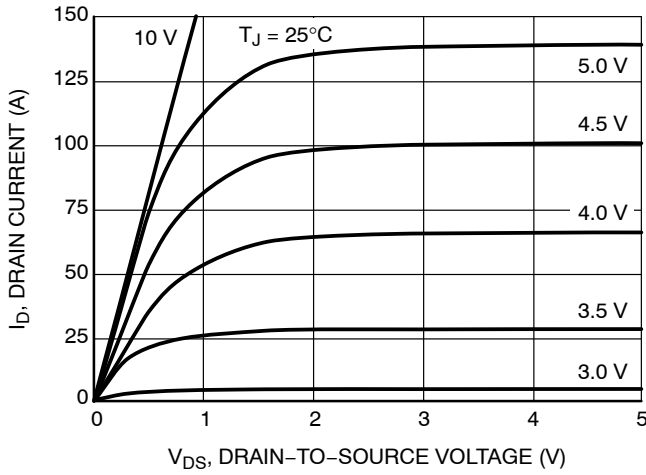


Figure 1. On-Region Characteristics

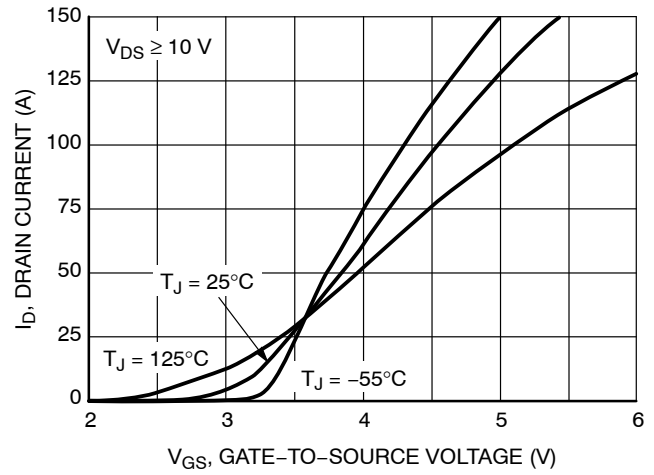


Figure 2. Transfer Characteristics

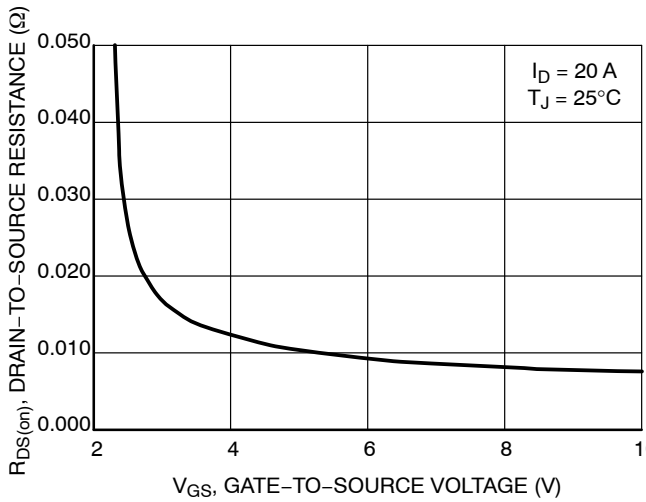


Figure 3. On-Resistance vs. Gate-to-Source Voltage

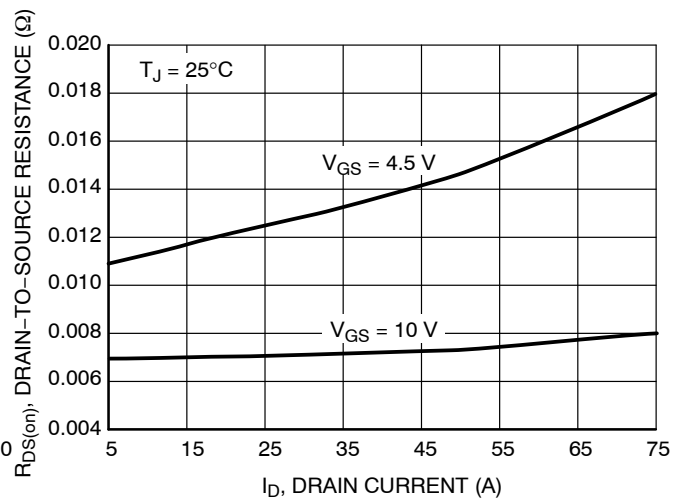


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

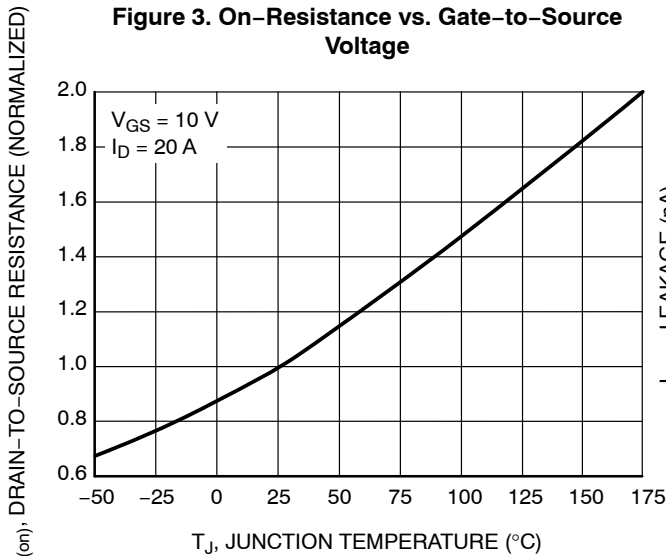


Figure 5. On-Resistance Variation with Temperature

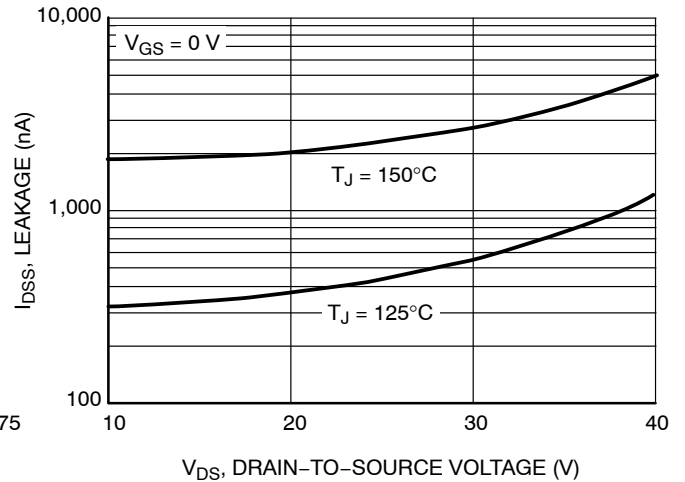


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

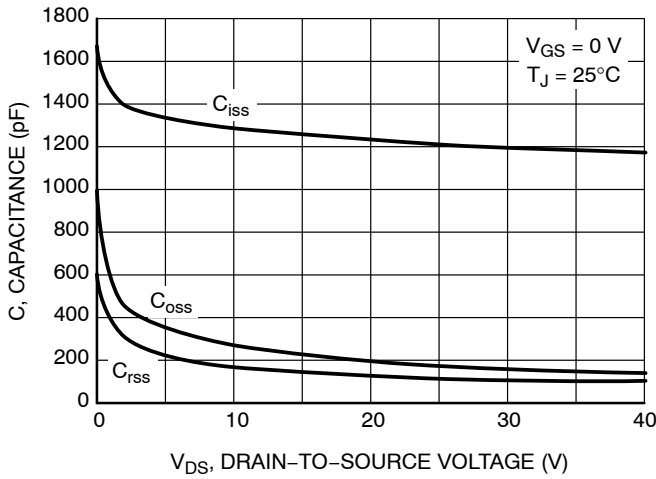


Figure 7. Capacitance Variation

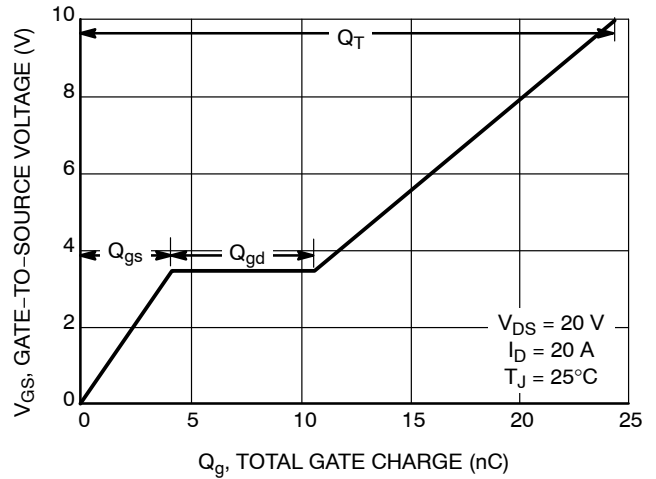


Figure 8. Gate-to-Source Voltage vs. Total Charge

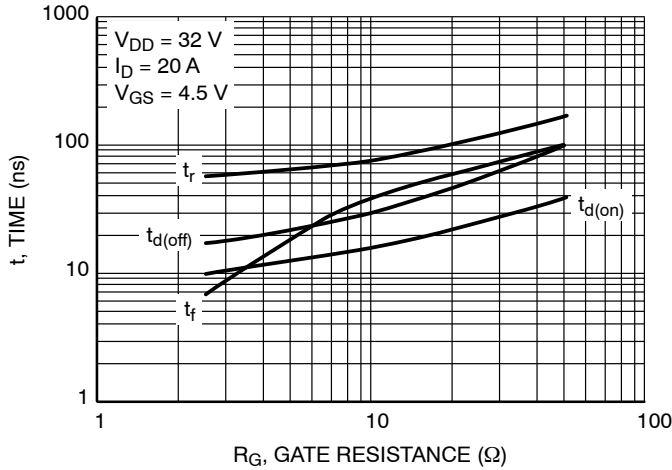


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

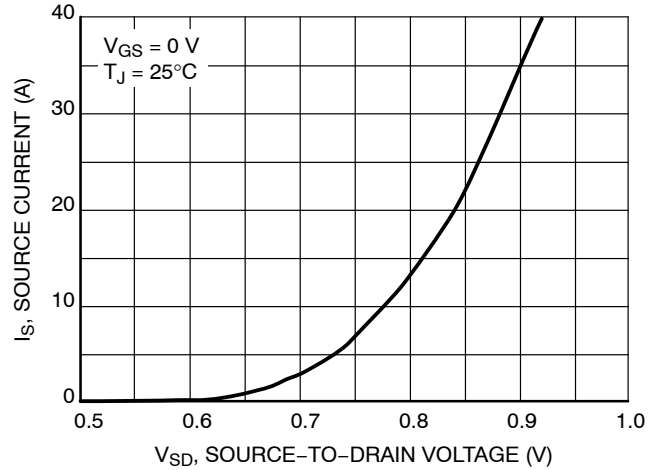


Figure 10. Diode Forward Voltage vs. Current

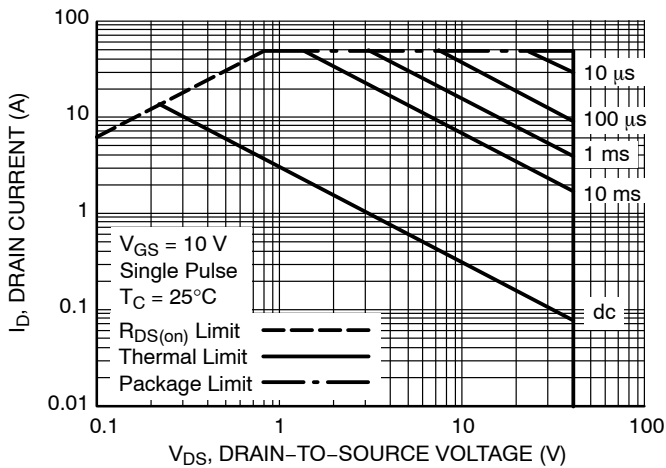


Figure 11. Maximum Rated Forward Biased Safe Operating Area

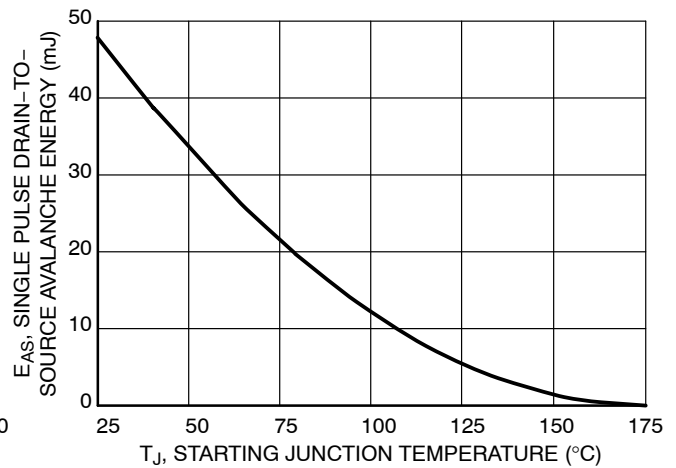


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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## TYPICAL CHARACTERISTICS

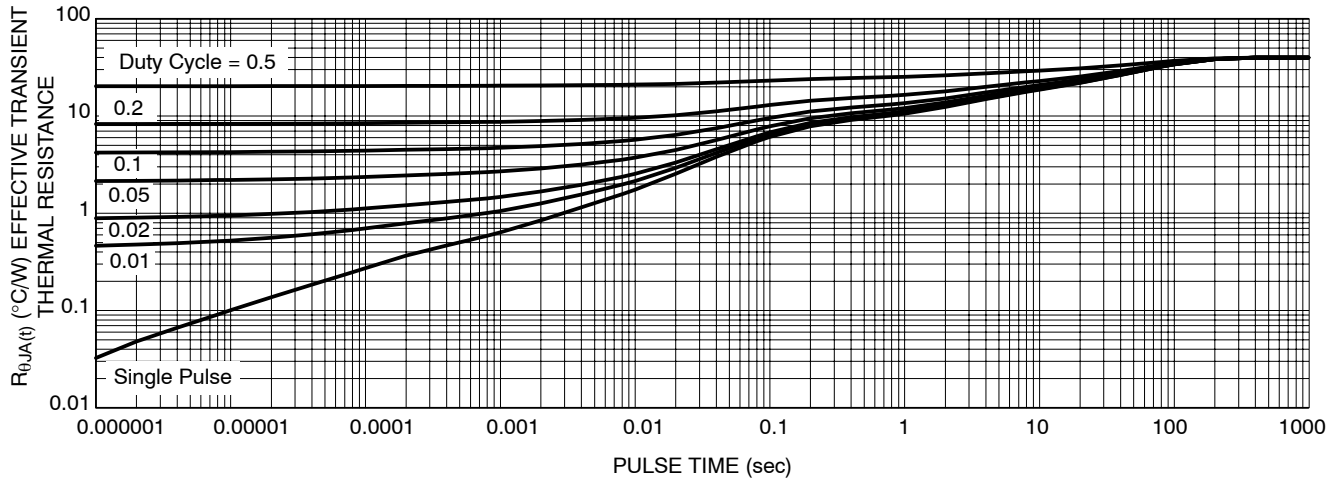
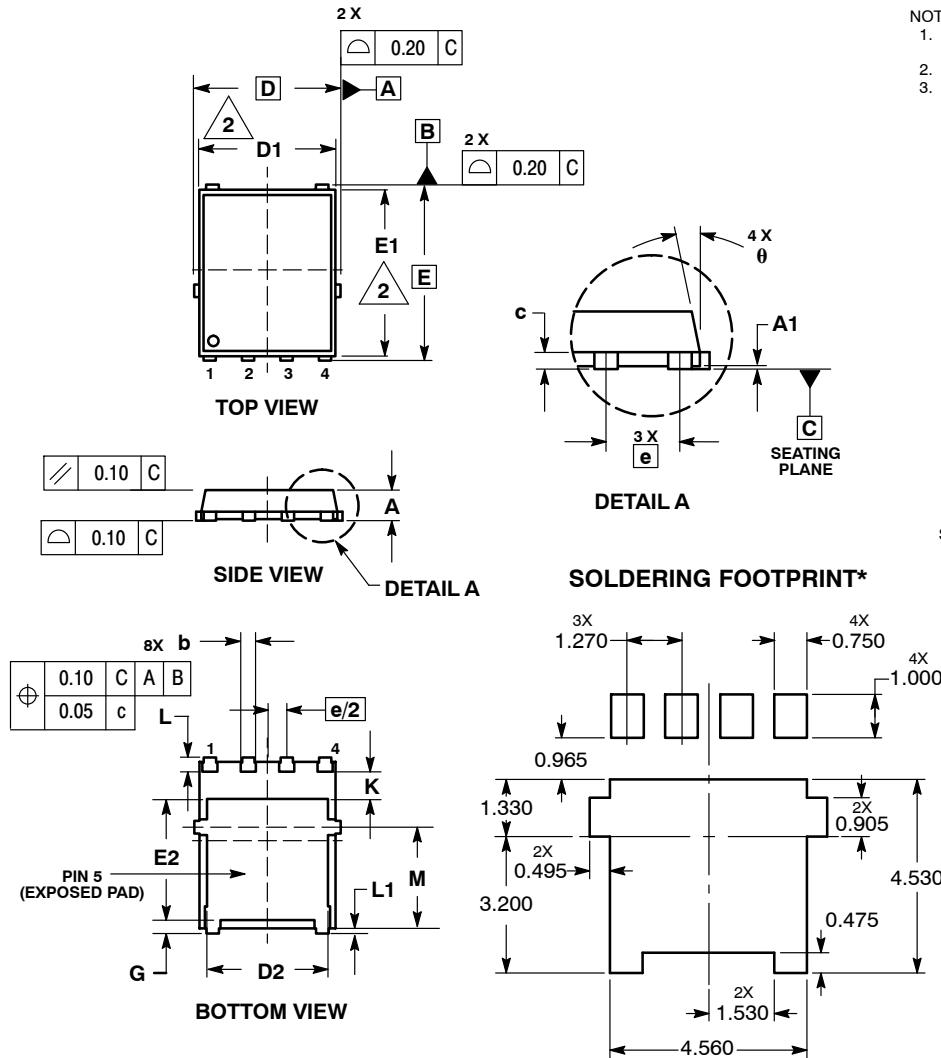


Figure 13. Thermal Response

# NTMFS5834NL, NVMFS5834NL

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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